

Embedded Systems

CS 397

TRIMESTER 3, AY 2021/22

Introduction to the Nucleo-F767ZI Microcontroller Board

- [Ref_02-1] DS11532, STM32F767xx Datasheet, ARM-based Cortex-M7 32-bit MCU+FPU, 462 DMIPS, up to 2MB Flash / 512+16+4KB RAM, USB OTG HS/FS, ..., Rev 7, February 2021. <https://www.st.com/en/microcontrollers-microprocessors/stm32f767zi.html>
- [Ref_02-2] ES0334, STM32F76xxx Errata Sheet, Device Limitations, Rev 8, February 2022.
- [Ref_05-1] UM1974, User Manual, STM32 Nucleo-144 boards (Nucleo-F767ZI, MB1137), Rev 8, August 2020. <https://www.st.com/en/evaluation-tools/nucleo-f767zi.html>

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Nucleo-F767ZI

Overview

- The **STM32 Nucleo-144** development board (**Nucleo-F767ZI**) with **STM32F767ZIT6** MCU provides an affordable and flexible way for users to try out new concepts and build prototypes with the STM32 microcontroller.
- This board provides access to more peripherals via its **ST Zio connector**, which is an extension of **Arduino Uno**, and **ST morpho headers**. These make it easy to expand the functionality of the Nucleo open development platform with a wide choice of specialized shields.
- This board does not require any separate probe for debugging/programming, as it integrates the **ST-LINK/V2-1 debugger/programmer**.
- Comprehensive software packages and various device examples are provided for the ease of software development.

<https://sg.element14.com/stmicroelectronics/nucleo-f767zi/dev-board-nucleo-32-mcu/dp/2546569>

STM32F767ZIT6

STM32F767ZIT6

Ordering Information

STM32 F 76x V G T 6 xxx

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

765= STM32F765xx, USB OTG FS/HS, camera interface, Ethernet

767= STM32F767xx, USB OTG FS/HS, camera interface, Ethernet, LCD-TFT

768 = STM32F768Ax, USB OTG FS/HS, camera interface, DSI host, WLCSP with internal regulator OFF

769= STM32F769xx, USB OTG FS/HS, camera interface, Ethernet, DSI host

Pin count

V = 100 pins

Z = 144 pins

I = 176 pins

A = 180 pins

B = 208 pins

N = 216 pins

Flash memory size

G = 1024 Kbytes of Flash memory

I = 2048 Kbytes of Flash memory

Package

T = LQFP

K = UFBGA

H = TFBGA

Y = WLCSP

Options

xxx = programmed parts

TR = tape and reel

Temperature range

6 = Industrial temperature range, -40 to 85 °C.

7 = Industrial temperature range, -40 to 105 °C.

Microcontroller Features

System	Chrom-ART Accelerator™ JPEG Codec Acceleration ART Accelerator™	2-Mbyte dual bank Flash 512-Kbyte SRAM + 16-Kbyte ITCM RAM FMC/SRAM/NOR/NAND/SDRAM Dual Quad-SPI 94-byte + 4-Kbyte backup SRAM 1024-byte OTP
	Cache I/D 16+16 Kbytes	
	ARM Cortex-M7 216 MHz	
Control	Floating point unit (FPU) Nested vector interrupt controller (NVIC) JTAG/SW debug/ETM Memory Protection Unit (MPU)	
	AXI and Multi-AHB bus matrix 16-channel DMA True random number generator (RNG)	
		Connectivity
		TFT LCD controller HDMI-CEC 6x SPI, 3x I ² S, 4x I ² C Camera interface Ethernet MAC 10/100 with IEEE 1588 MDIO slave 3x CAN 2.0B 1x USB 2.0 OTG FS/HS 1x USB 2.0 OTG FS 2x SDMMC 4x USART + 4 UART LIN, smartcard, IrDA, modem control 2x SAI (Serial audio interface) SPDIF input x4 DFSDM
		Analog
		2x 12-bit, 2-channel DACs 3x 12-bit ADC 24 channels / 2.4 MSPS Temperature sensor

STM32F767ZIT6

Microcontroller Features

- STM32F767ZIT6 in LQFP144 package

for graphic computing
- ARM 32-bit Cortex-M7 + DPFPUs + Chrom-ART (Adaptive Real-Time) Accelerator
- **216 MHz max CPU frequency**
- **VDD from 1.7 V to 3.6 V**
- **2 MB Flash**
- **512 KB SRAM**
- GPIOs (114) with external interrupt capability
- 12-bit ADCs with 24 channels (3)
- 12-bit DAC channels (2)
- USART (4) / UART (4)
- I2C (4)
- SPI (6)
- General Purpose Timers (10)
- Advanced-control Timers (2)
- Basic Timers (2)
- Low-power Timer (1)
- Watchdog Timers (2)
- **CAN (Controller Area Network, bxCAN) 2.0B active (3)**
- SAI (2), SPDIFRX (4 inputs), SDMMC (2), Camera Interface, LCD-TFT,
- RNG (Random Number Generator)
- USB 2.0 OTG HS/FS (High Speed 480 Mb/s, Full Speed 12 Mb/s)
- **Ethernet MAC (Media Access Controller) interface with dedicated DMA**

LQPF = Low-profile Quad Flat Package

DPFPUs = double-precision floating point unit

USB OTG (On-The-Go) is a specification allows a USB device to act as a host for the attachment of other USB devices such as a USB flash drive, mouse or keyboard.

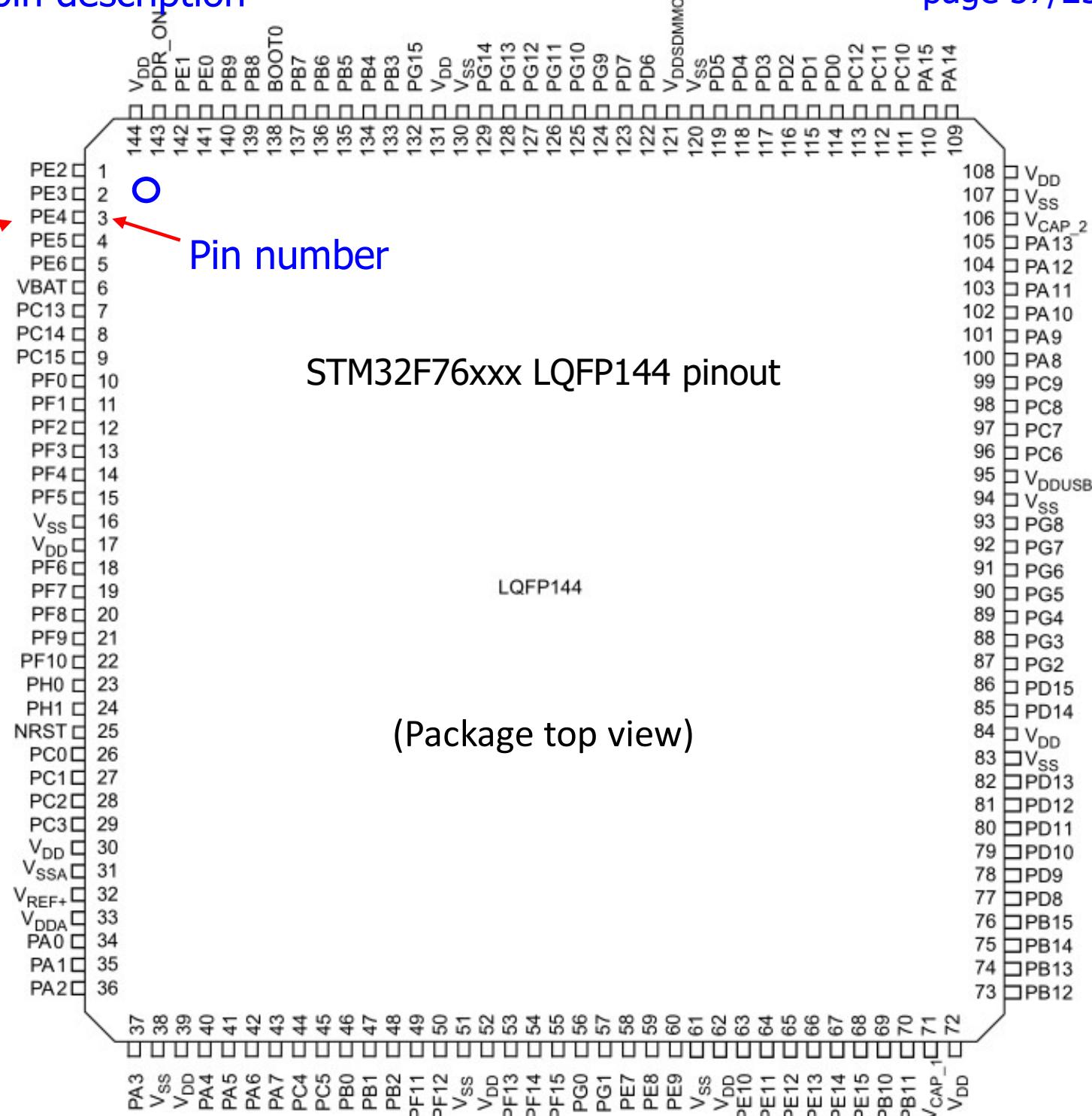


Table 11. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

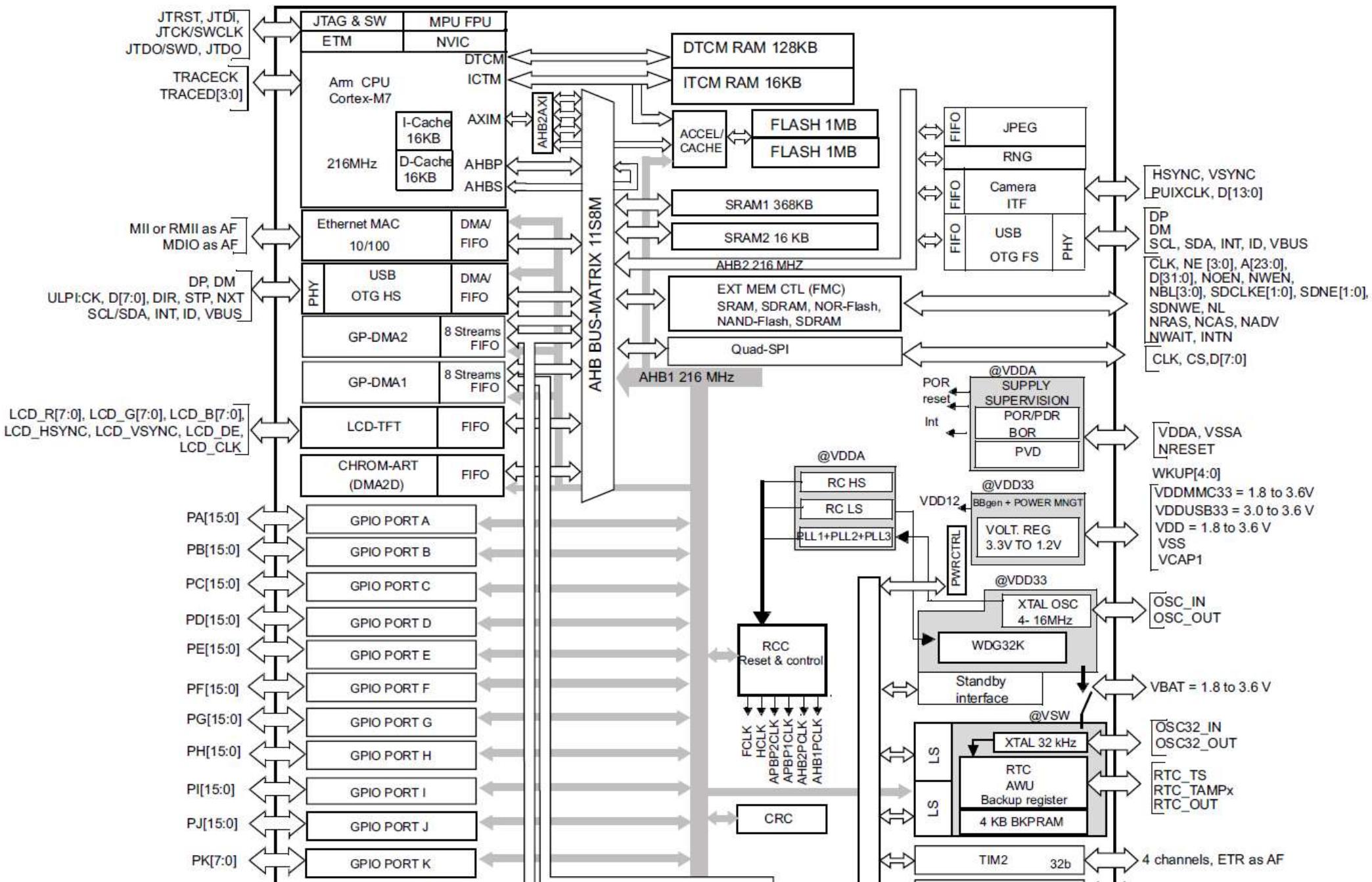
Pin Number												Notes	Alternate functions	Additional functions	
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
TFBGA100	LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180 ⁽¹⁾	LQFP176	LQFP208	TFBGA216	Pin name (function after reset)	Pin type	I/O structure		
C3	3	3	B1	3	3	A1	C12	3	3	A1	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, DFSDM1_DATIN3, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT
D3	4	4	B2	4	4	B1	D12	4	4	B1	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, DFSDM1_CKIN3, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT
E3	5	5	B3	5	5	B2	E11	5	5	B2	PE6	I/O	FT	-	TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCLK_B, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT

Table 10. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

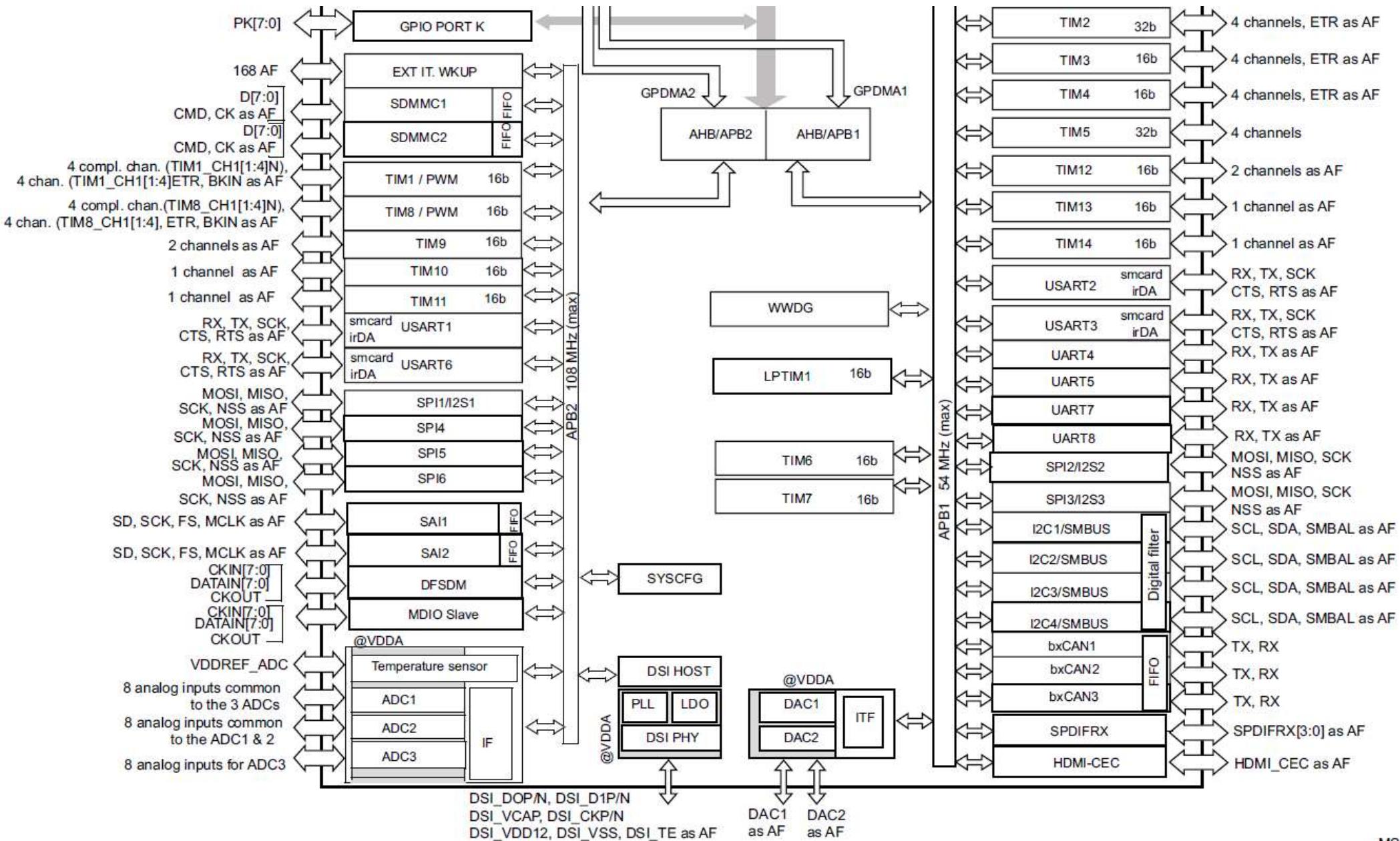
STM32F767ZIT6 Block Diagram (1/2)

page 20/252 [Ref_02-1]



STM32F767ZIT6 Block Diagram (2/2)

page 20/252 [Ref_02-1]



Nucleo-F767ZI

The STM32 Nucleo-F767ZI board offers the following features:

- STM32 microcontroller in LQFP144 package
- Ethernet compliant with IEEE-802.3-2002
- USB OTG or USB full-speed device user connectivity
- 3 user LEDs and 2 push-buttons: USER and RESET
- LSE (low speed external clock) crystal: 32.768 kHz crystal oscillator
- Board connectors:
 - [USB with Micro-B \(ST-LINK\)](#) <https://www.st.com/en/evaluation-tools/nucleo-f767Zi.html>
 - USB with Micro-AB
 - Ethernet RJ45 <https://os.mbed.com/platforms/ST-Nucleo-F767ZI/>
- Expansion connectors:
 - [ST Zio including Arduino Uno V3 \(CN7, CN8, CN9, CN10\)](#)
 - [ST morpho \(CN11, CN12\)](#)
- Flexible power supply options: ST-LINK USB VBUS, or external sources
- On-board ST-LINK/V2-1 debugger/programmer with SWD connector:
 - ST-LINK/V2-1 standalone kit capability
 - USB re-enumeration capability: virtual COM port, mass storage, debug port
- Free software libraries and examples available with the **STM32Cube package**
- Supported by Integrated Development Environments (IDEs): IAR, Keil, GCC-based IDEs, [STM32CubeMX + Atollic TrueSTUDIO](#)
- ARM Mbed Enabled (see <https://www.mbed.com/en/>) [STM32CubeIDE](#)

The ST Zio connectors

		CN7		CN8		CN9		CN10	
PC6	D16	1	2	D43	PC8	D51	PD7	GND	D7
PB15	D17	3	4	D44	PC9	D52	PD6	GND	PF13
PB13	D18	5	6	D45	PC10	D53	PD5	AGND	D6
PB12	D19	7	8	D46	PC11	D54	PD4	AVDD	PE9
PA15	D20	9	10	D47	PC12	D55	PD3	AGND	PE11
PC7	D21	11	12	D48	PD2	GND	PD2	AVDD	D5
PB5	D22	13	14	D49	PG2	GND	PD1	AGND	PE14
PB3	D23	15	16	D50	PG3	PD6	PG14	PA5	D3
PA4	D24	17	18			PD26	D1	PA6	PE13
PB4	D25	19	20			PD27	D0	PA7	PE15
AVDD						PB2		PF12	PG9
AGND						D27			D4
GND						PD28			PE11
GND						PD13			D41
GND						PD12			PE7
GND						PD11			GND
GND						D30			D40
GND						PE2			PE10
GND						D31			D39
GND						PE3			PE12
GND						D61			PE14
GND						PF8			D38
GND						D62			PE15
GND						PF7			D37
GND						D63			PB10
GND						PF9			D36
GND						D64			PB11
PE0	D34	27	28			PG1			
PE0	D35	29	30						

Nucleo-F767ZI Board Pinout

- Arduino subset of Zio = A0 to A5 and D0 to D15
- Zio extension = A6 to A8 and D16 to D72

Pins Legend

Labels usable in code

PX_Y MCU pin without conflict

PX_Y MCU pin connected to other components

XXX Arduino connector names (A0, D1, ...)

XXX LEDs and Buttons (LED_1, USER_BUTTON, ...)

Labels not usable in code (for information only)

XXX Serial pins (USART/UART)

XXX SPI pins

XXX I2C pins

XXX PWMOut pins (TIMER n/c[N])
n = Timer number c = Channel
N = Inverted channel

XXX AnalogIn (ADC) and AnalogOut pins (DAC)

XXX CAN pins

XXX Power and control pins (3V3, GND, RESET, ...)

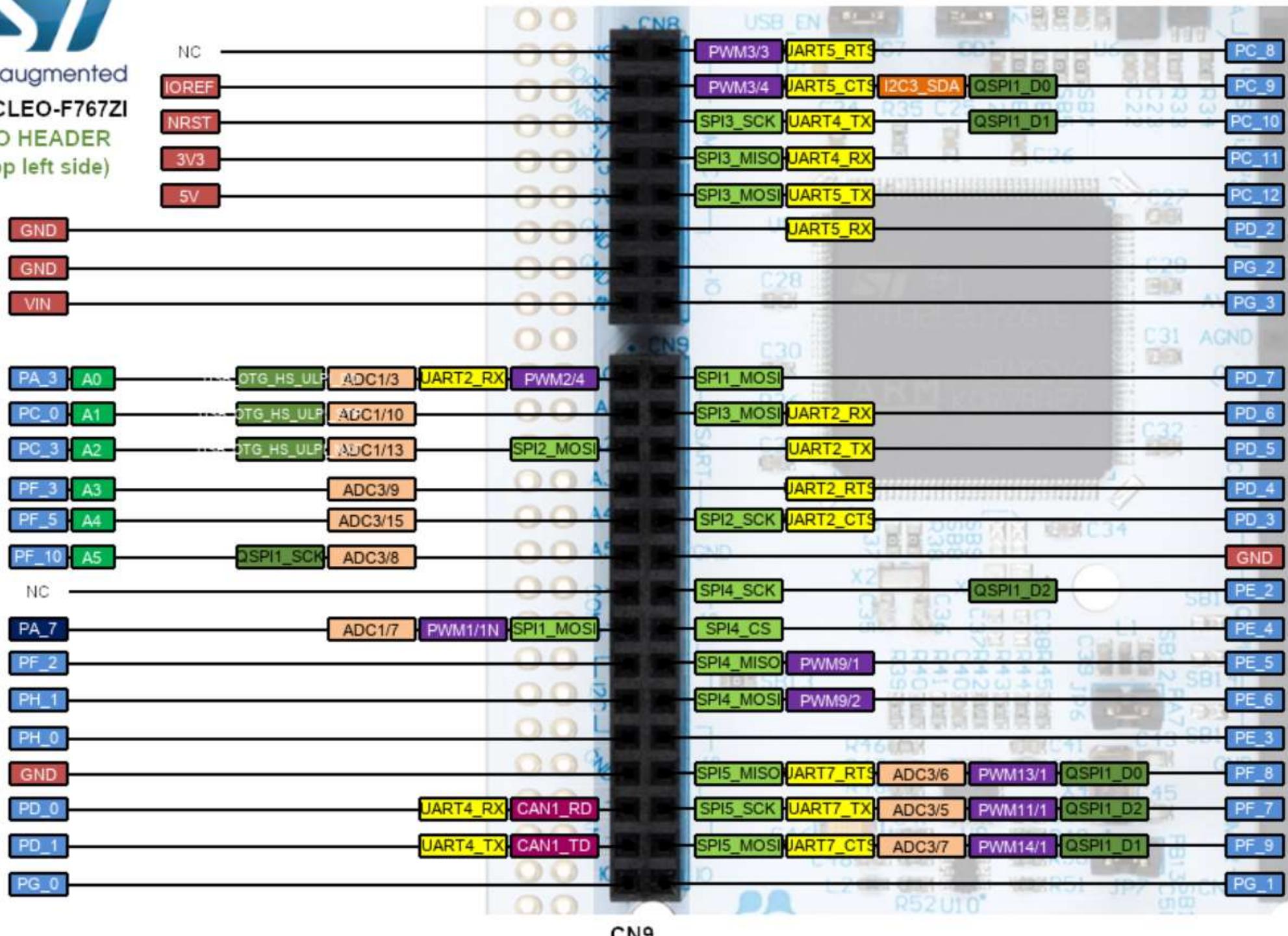


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NUCLEO-F767ZI

ZIO HEADER
(top left side)

ST Zio Header CN8



CN9



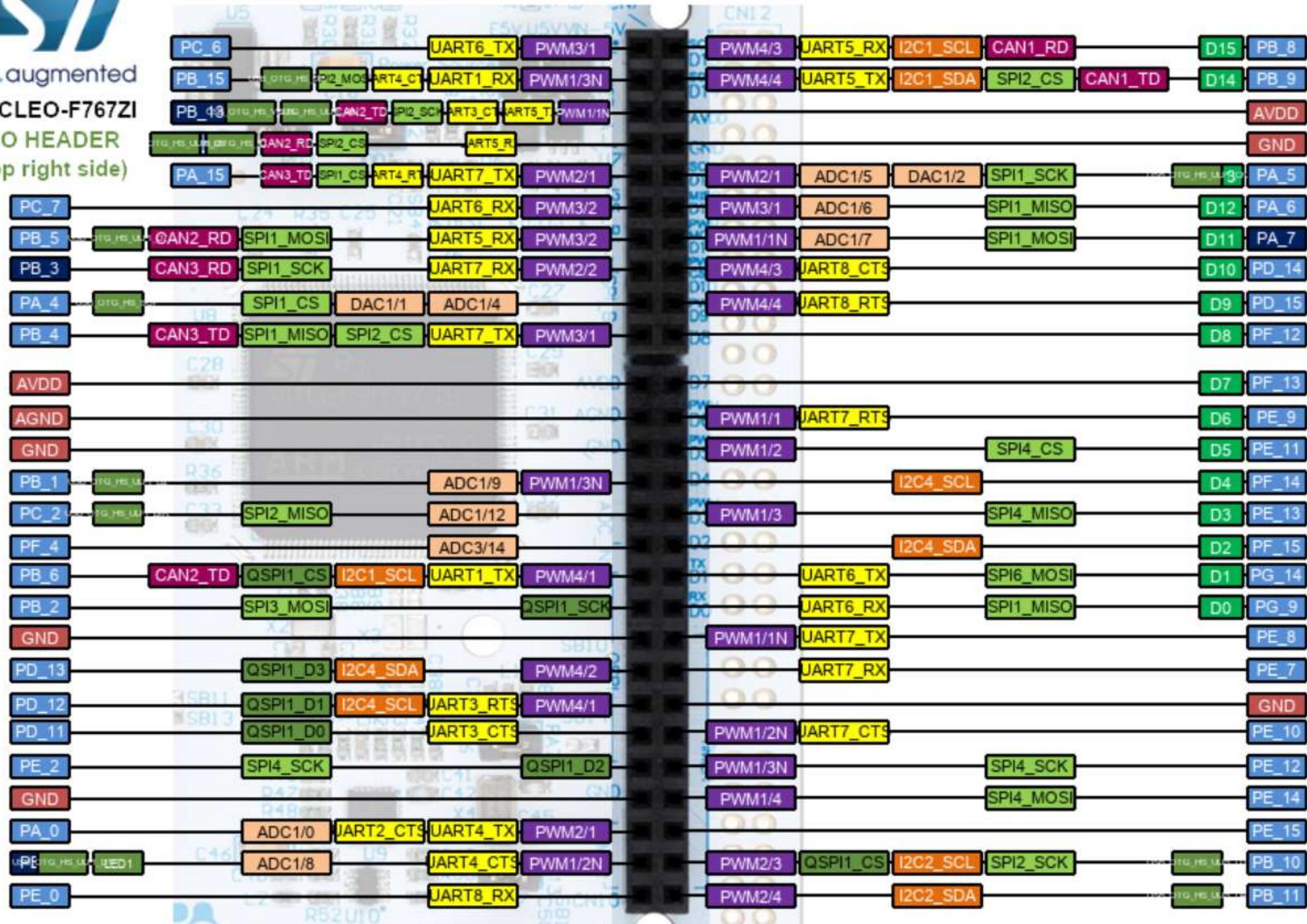
ST Zio Header CN7

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NUCLEO-F767ZI

ZIO HEADER

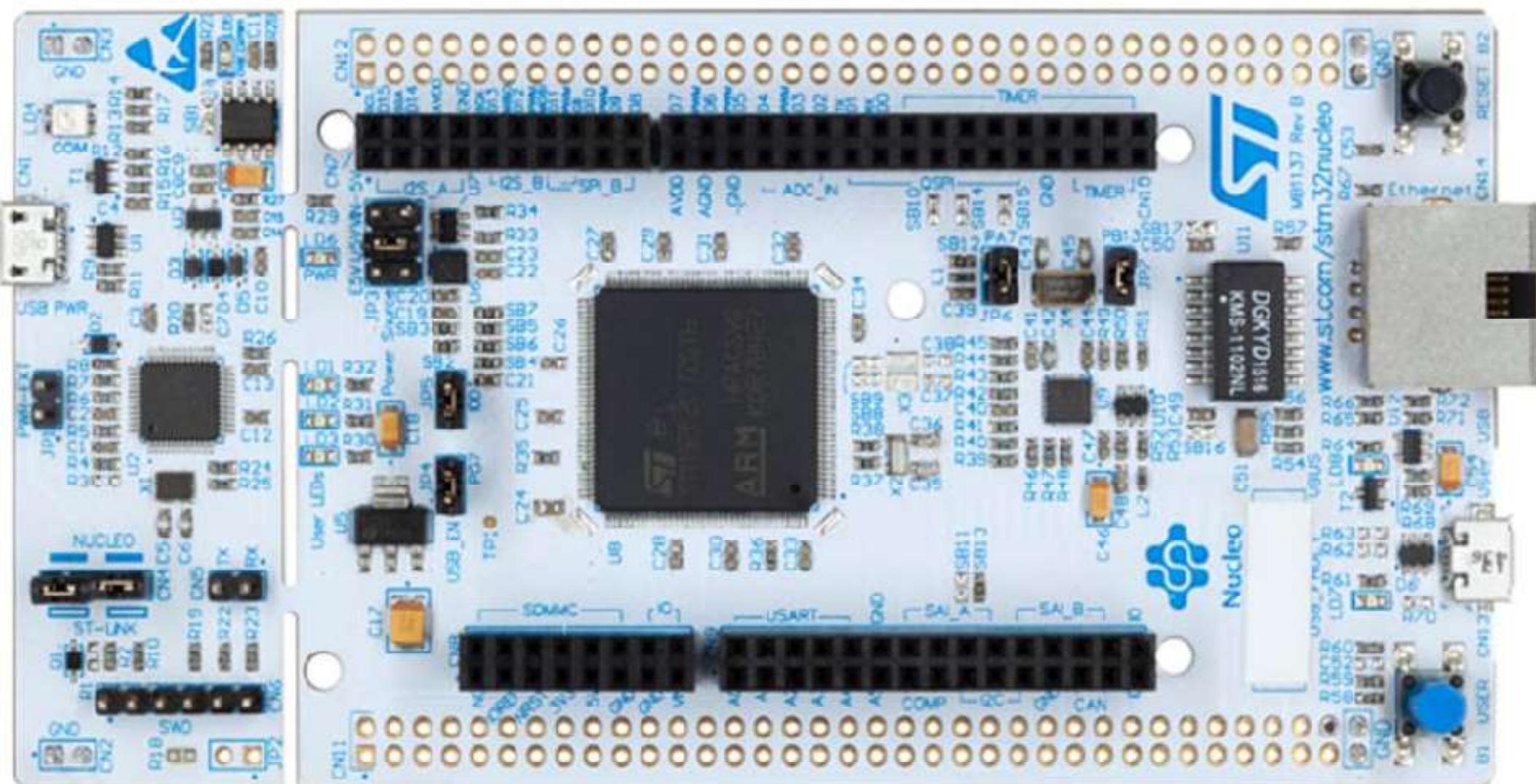
(top right side)



CN10

Nucleo-F767ZI

CN12

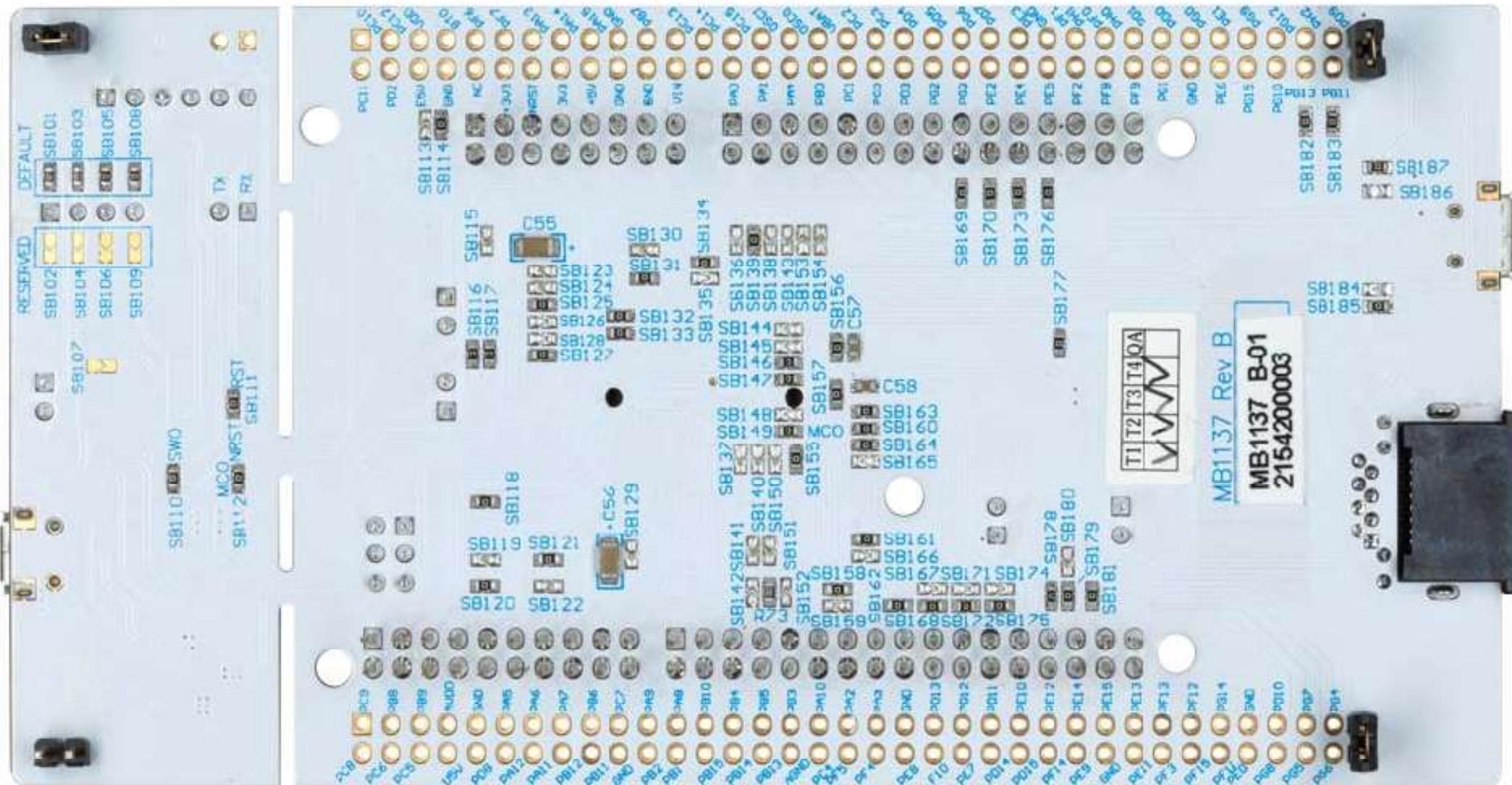


CN11

Nucleo-144 board (top view)

Nucleo-F767ZI

CN11

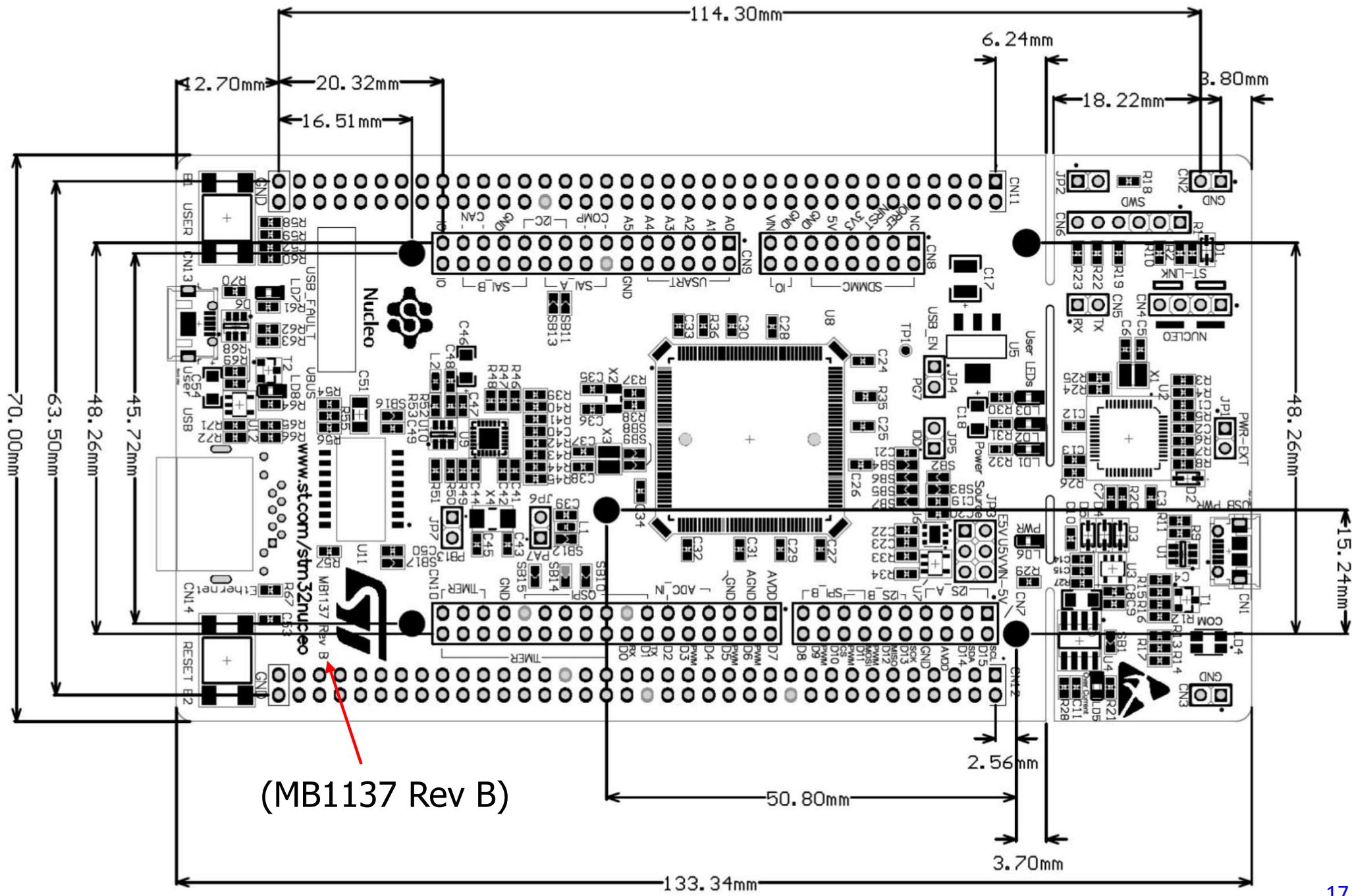


CN12

Nucleo-144 board (bottom view)

Nucleo-F767ZI

Dimensions of Nucleo-F767ZI Board



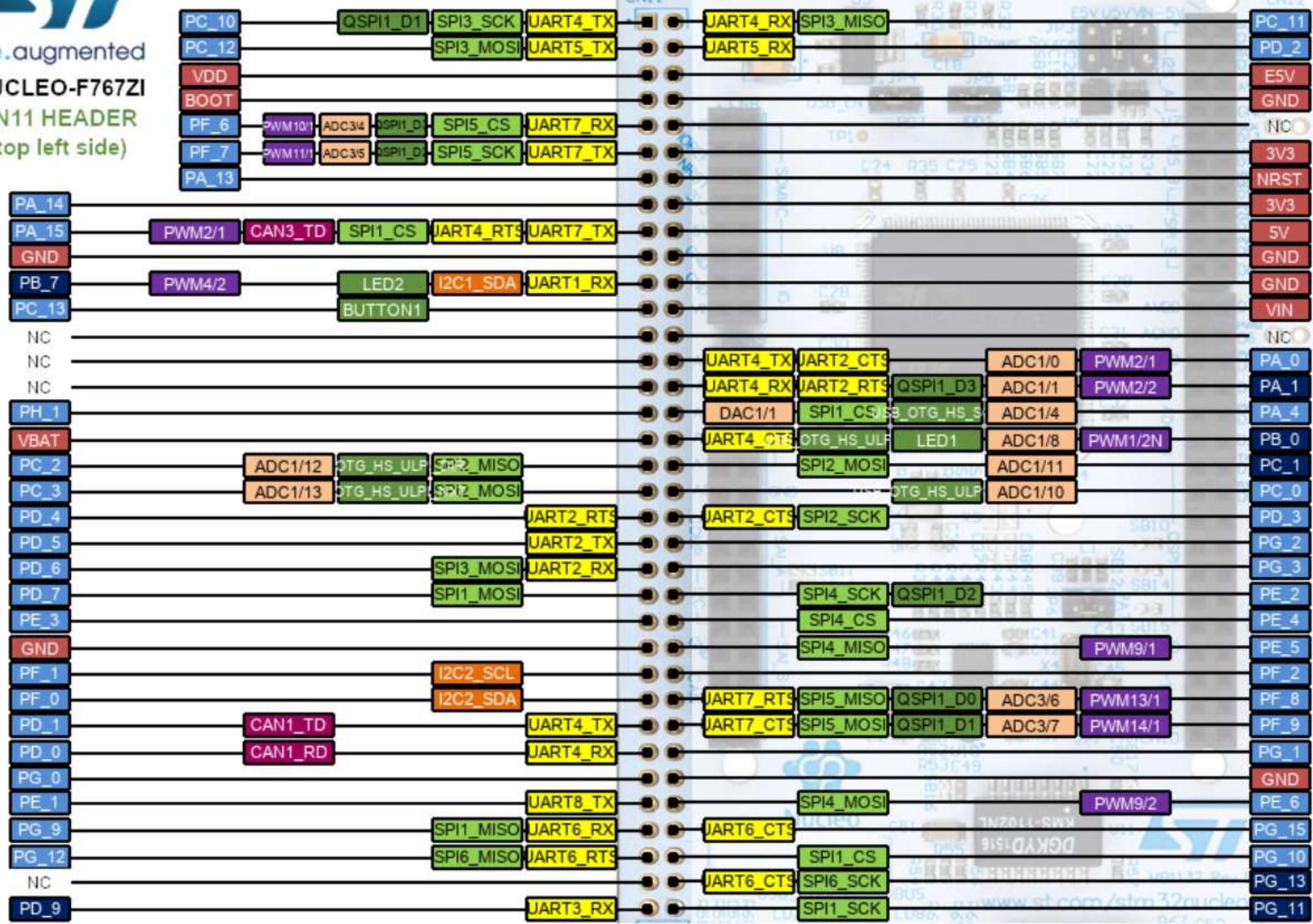


ST Morpho Header (CN11)

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NUCLEO-F767ZI

CN11 HEADER
(top left side)



CN11



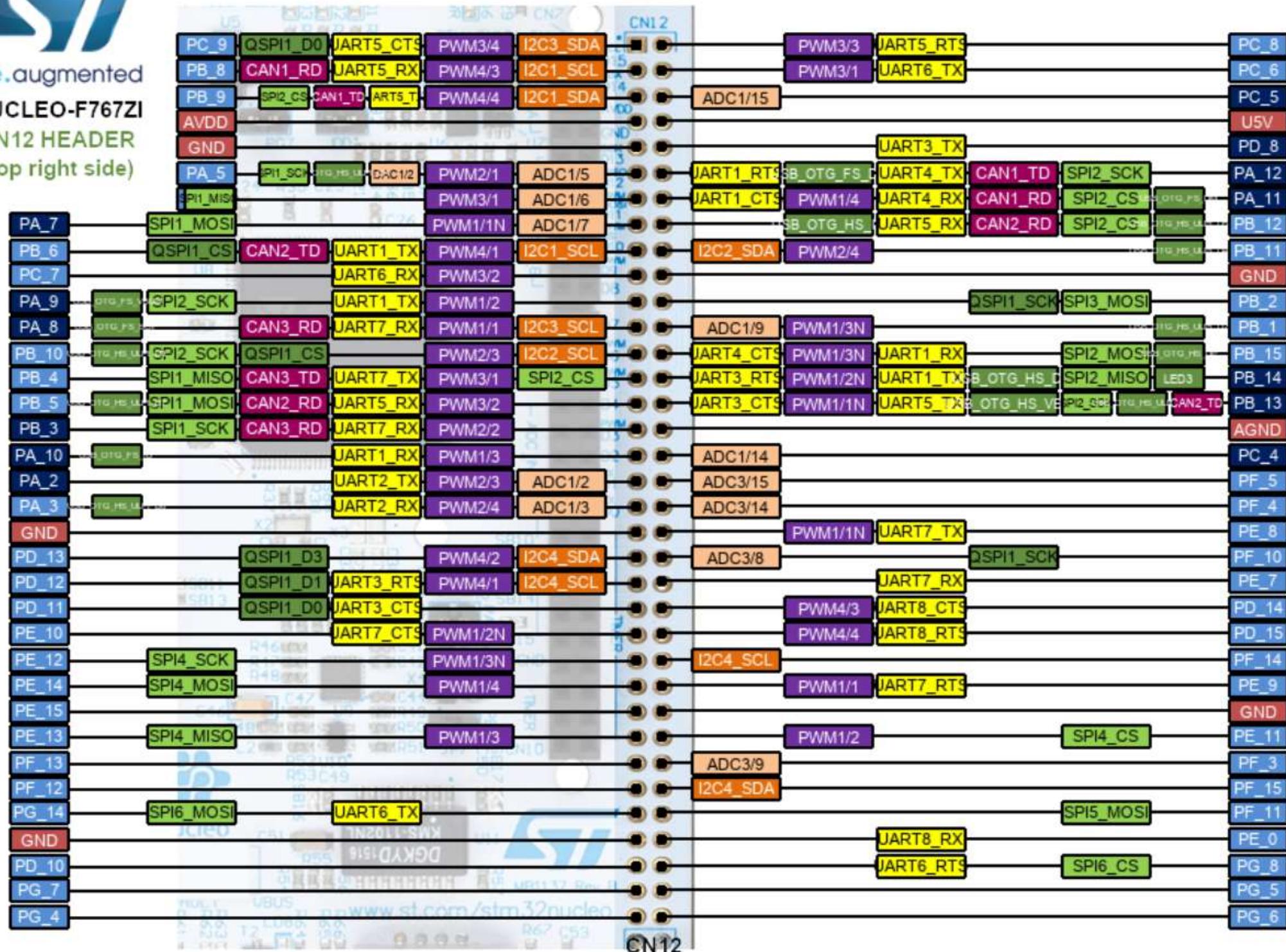
ST Morpho Header (CN12)

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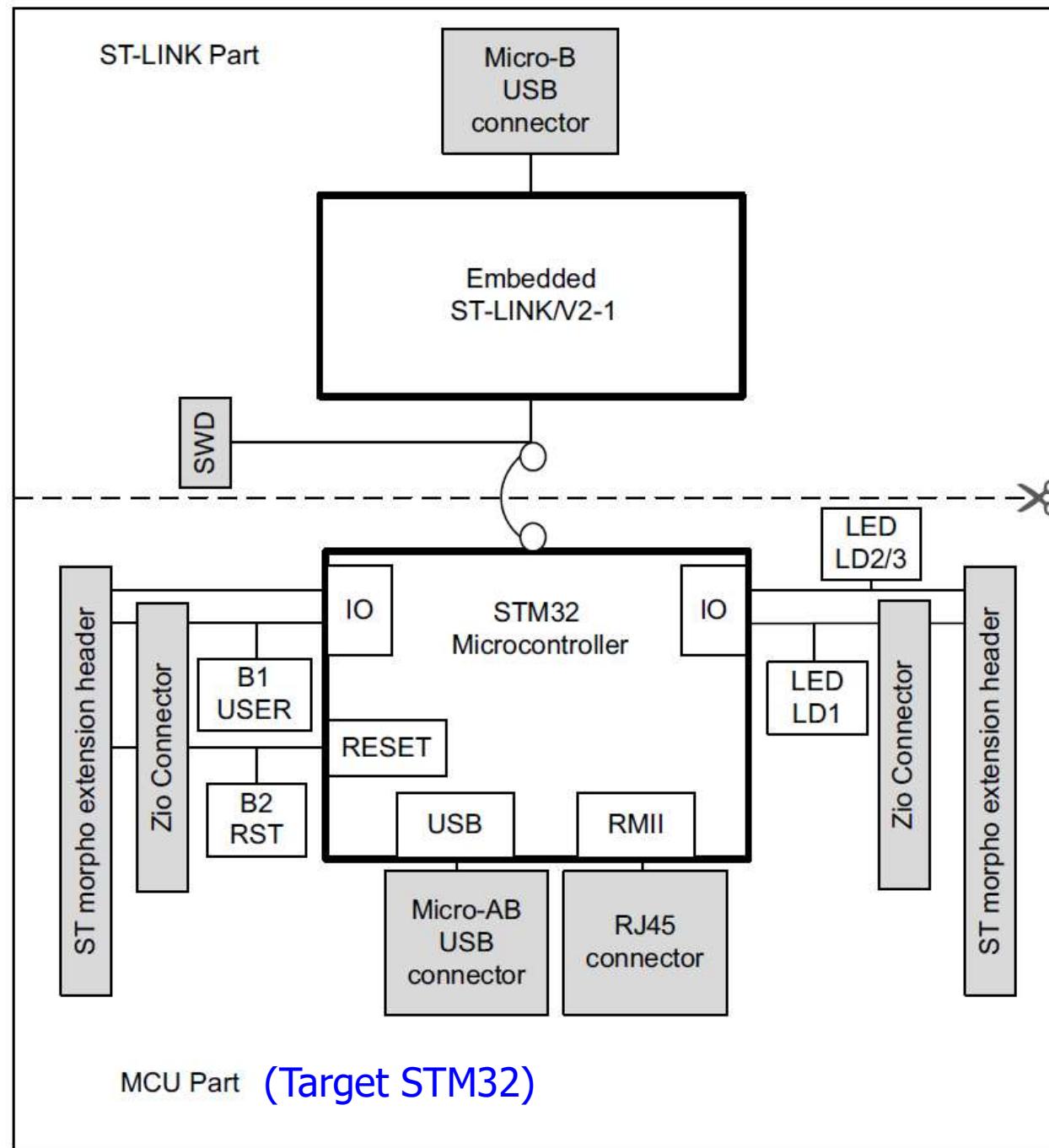
CN12 HEADER

(top right side)



Nucleo-F767ZI

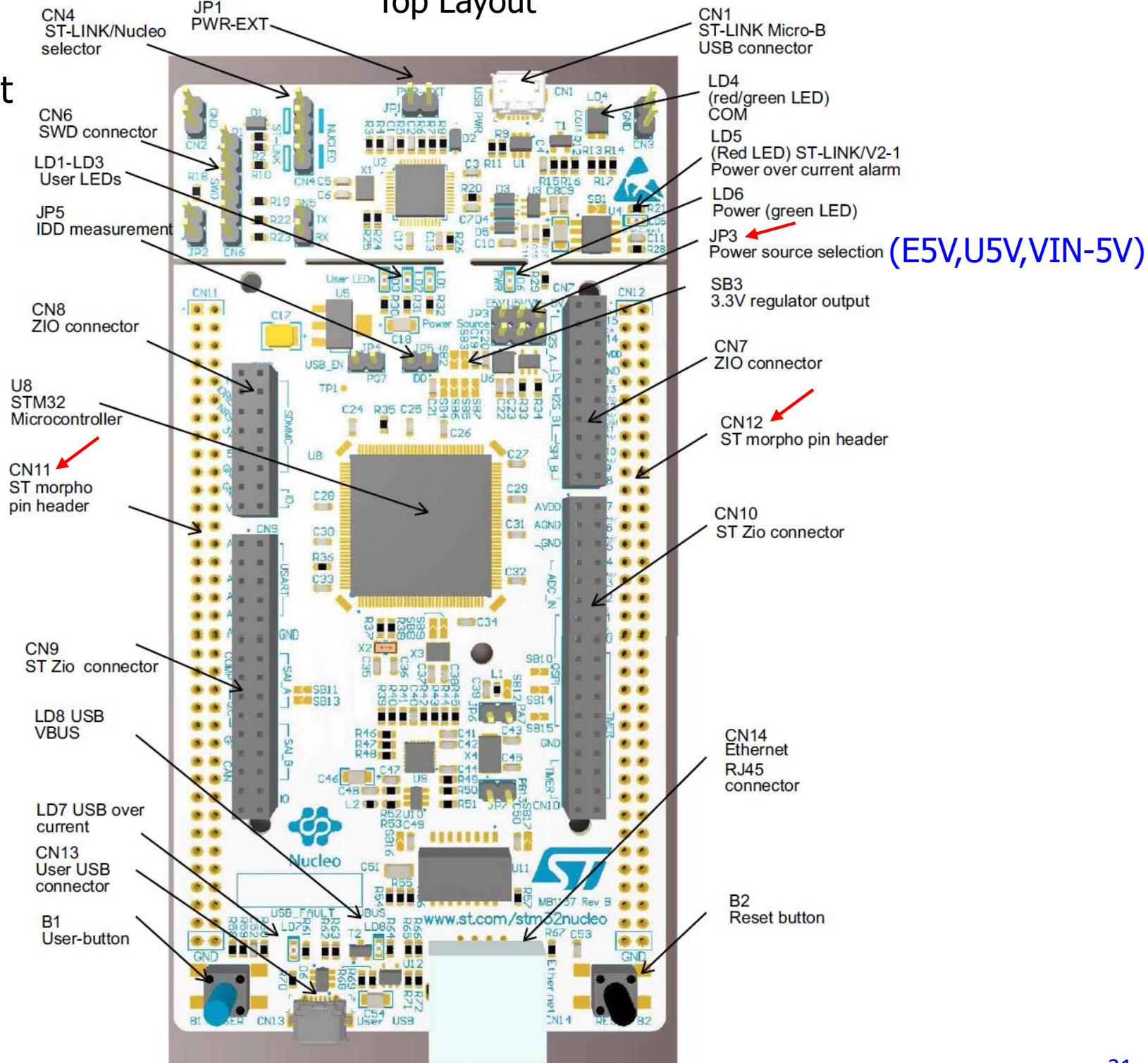
Hardware Layout



Hardware Block Diagram (various connectors)

Top Layout

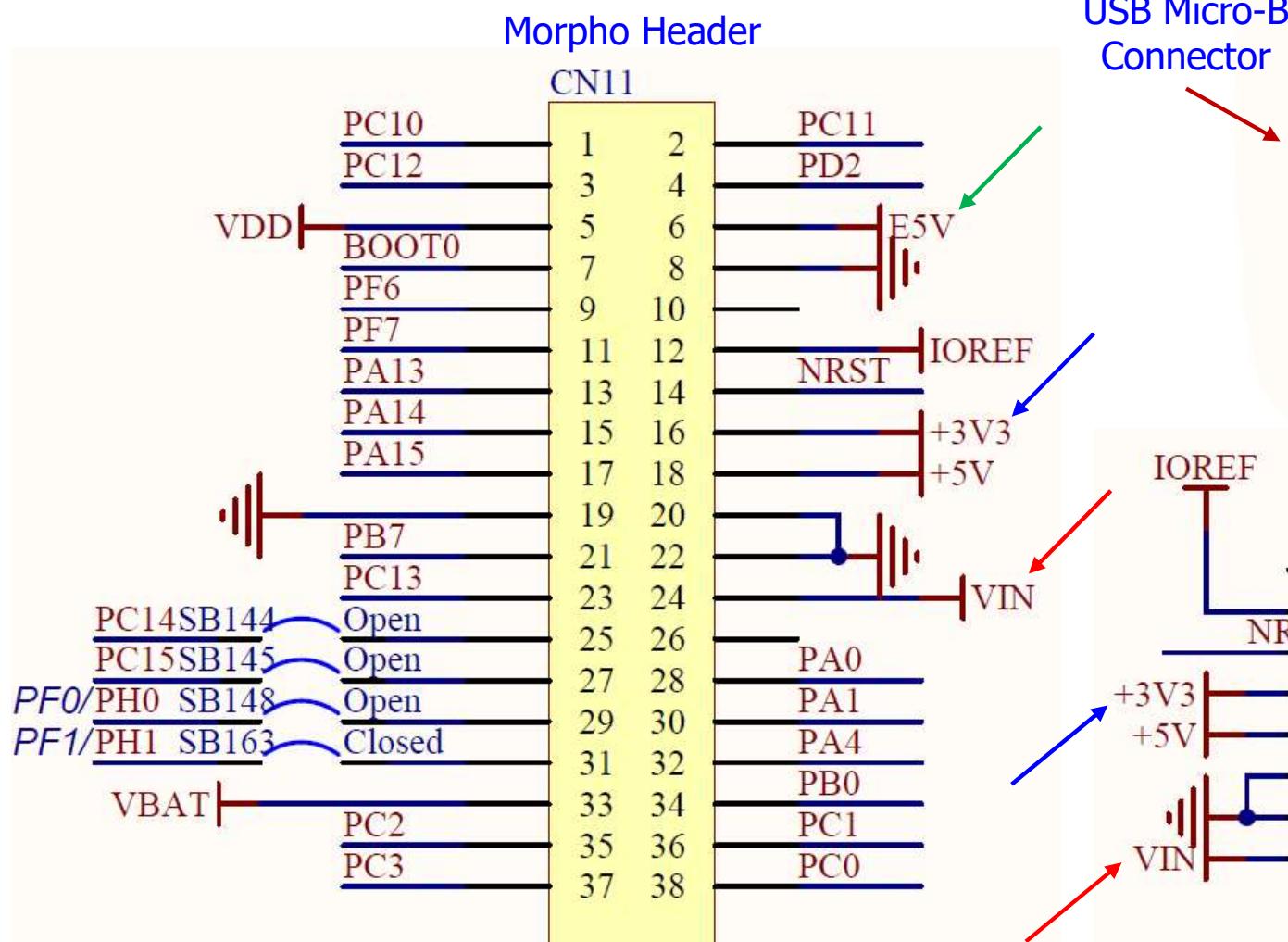
Hardware Layout



Power Supply

The electrical supply can be from one of the following inputs:

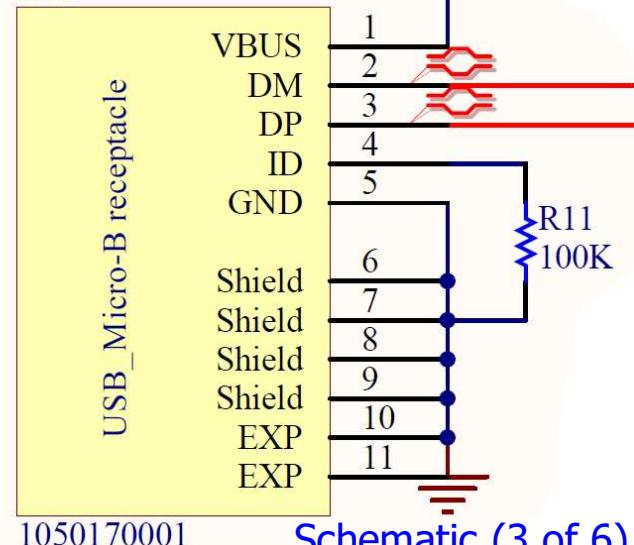
U5V (5 V), **VIN** (7 – 12 V), **E5V** (4.75 – 5.25 V, 0.5 A max),
and **+3V3** (3.0 – 3.6 V)



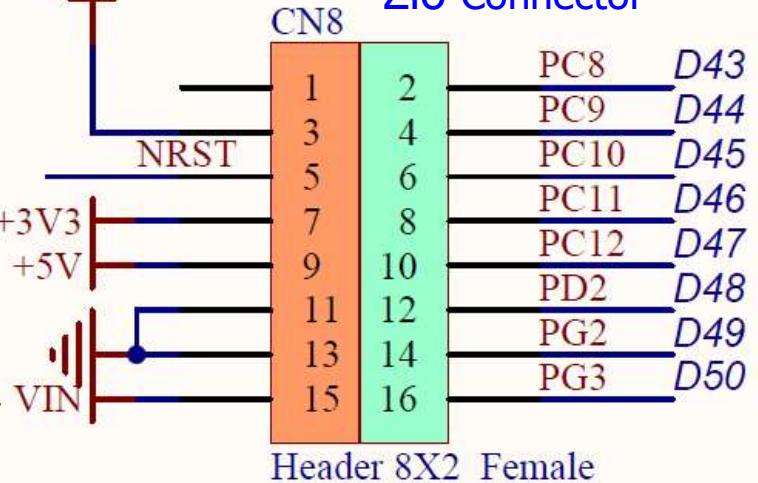
VIN: 7 V, 0.8A max,
7 – 9 V, 0.45 A max,
9 – 12 V, 0.25A max.

USB ST-LINK

CN1



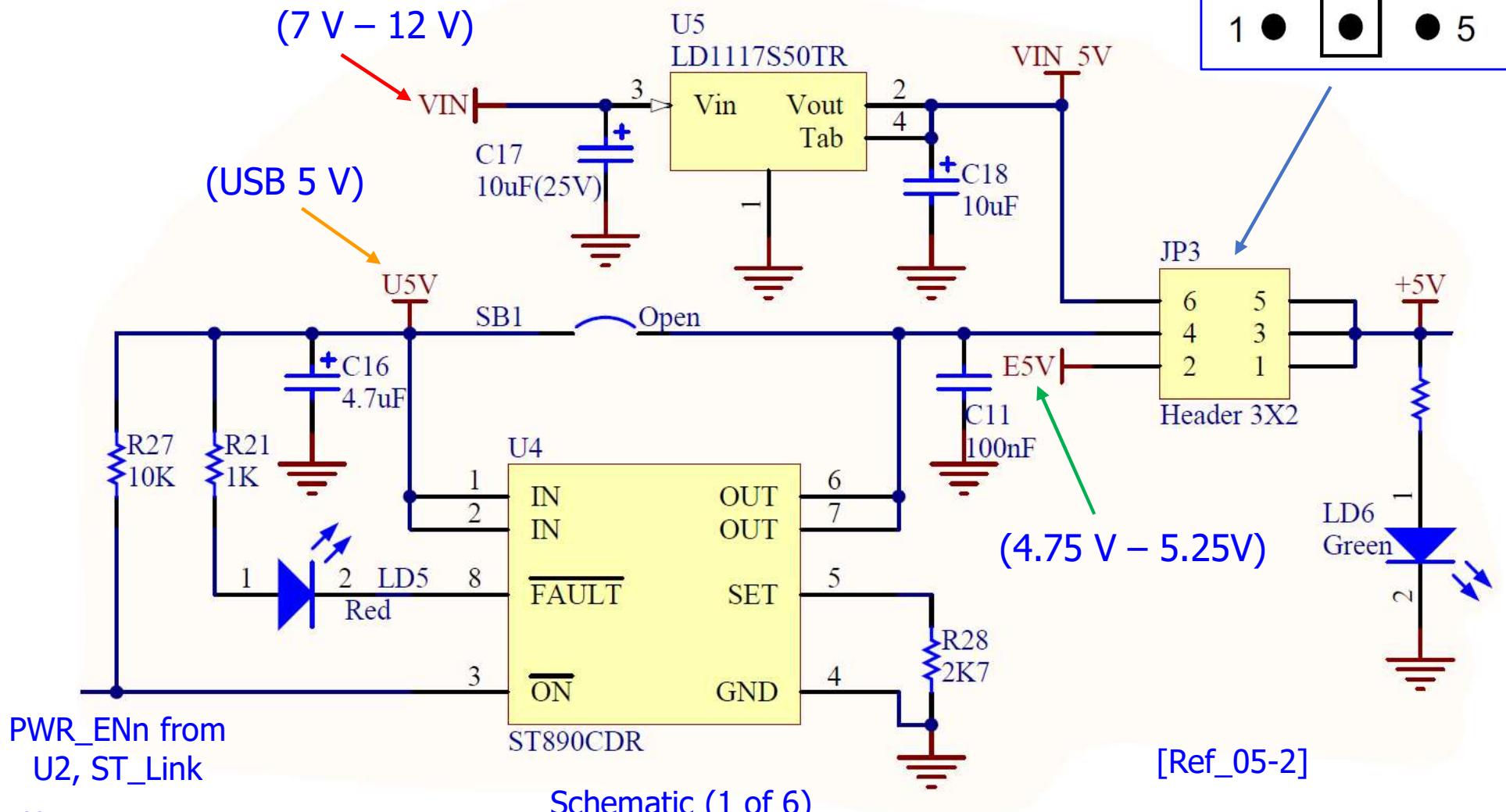
Zio Connector



Nucleo-F767ZI

Power Supply Via ST-Link USB Connector CN1 (U5V)

JP1 is configured according to the maximum current consumption of the board when powered by USB (U5V), (JP1 OFF: 0.3A max, and JP1 ON: 0.1 A max). Keep **JP1 OFF**, **JP5 ON**, **CN4 ON**, and **JP3** is at pins **3 & 4**. LED LD6 (green, PWR) and LD4 (red, COM) light up.

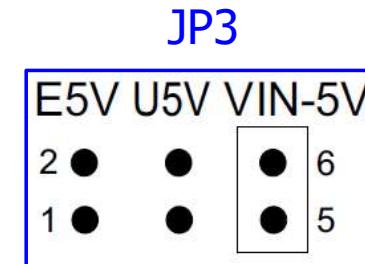


PWR_ENn from
U2, ST_Link

Power Supply Via External Inputs (VIN or E5V)

When board is supplied by **VIN** or **E5V**, the jumper configuration must be

- Jumper **JP3** on pins **1 & 2** for **E5V** or
jumper **JP3** on pins **5 & 6** for **VIN**
- Jumper **JP1 OFF**, Jumper **JP5 ON**, and **CN4 ON**



Note: Power supply to the board by VIN or E5V must always be maintained before and after connecting the USB cable for programming or debugging.

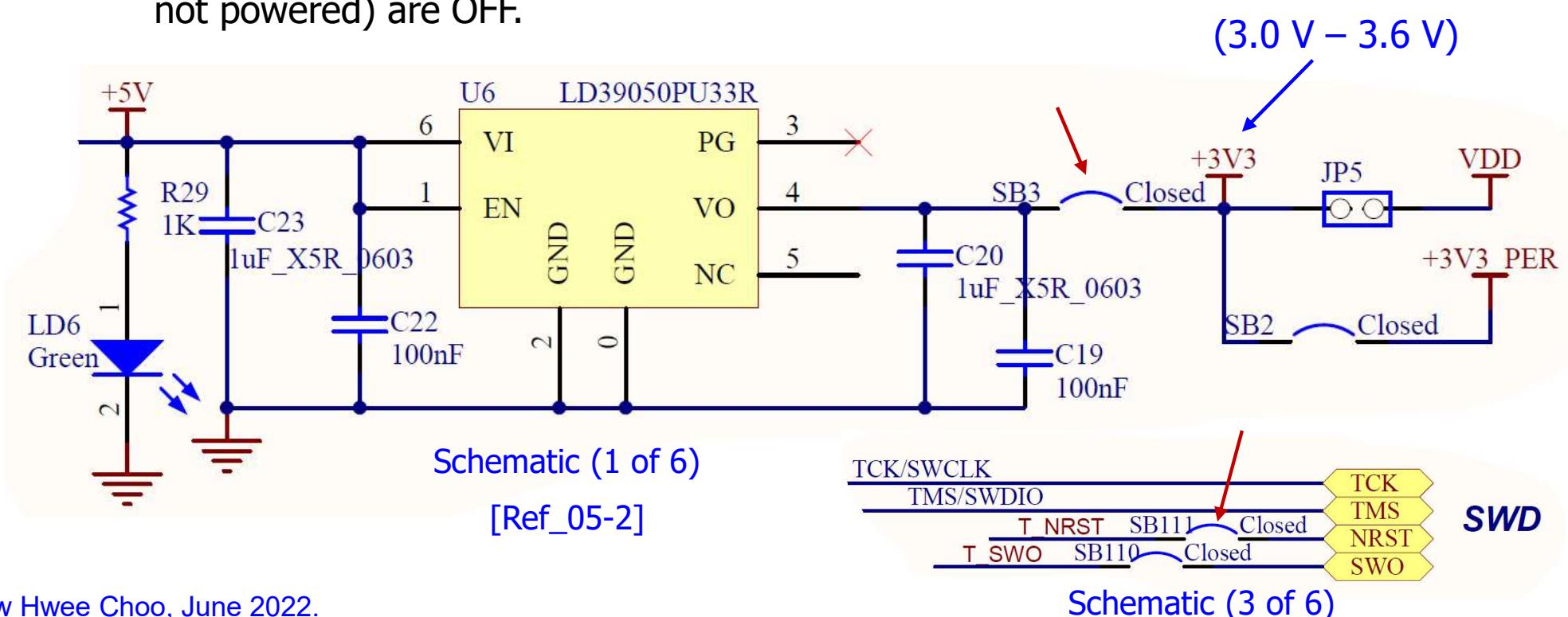
CN4: It is used to enable the on-board program/debug (Jumpers On: Nucleo selected).

Power Supply Output with U5V (USB) or VIN or E5V Input

- When powered by USB, VIN or E5V, the **+5 V** (CN8 pin 9 or CN11 pin 18) can be used as output power supply for an ST Zio shield or an extension board.
- In this case, the maximum current of the power source must be respected.
- The **+3.3 V** (CN8 pin 7 or CN11 pin 16) can be used also as power supply output. The current is limited by the maximum current capability of the regulator U6 (500mA max).

Power Supply Via External +3V3 Input

- When only +3.3 V is supplied to the board (via CN8 pin 7 or CN11 pin 16), the programming and debugging features are not available, since the ST-LINK is not powered.
- When the board is powered by only +3.3 V, two different configurations are possible:
 - ST-LINK is removed (PCB cut) and SB3 (U6 3.3 V regulator output) is OFF.
 - SB3 and SB111 (NRST, note that ST-LINK U2 will short the MCU NRST line when it is not powered) are OFF.



LEDs

User LD1: a green user LED is connected to the pin **PB0** (default: SB120 ON and SB119 OFF) or **PA5** (SB119 ON and SB120 OFF).

User LD2: a blue user LED is connected to **PB7**.

User LD3: a red user LED is connected to **PB14**.

LD4 COM: the tricolor LED LD4 (green, orange, red) provides information about ST-LINK communication status. LD4 default color is **red**. LD4 turns to **green** to indicate that communication is in progress between the PC and the ST-LINK, with the following setup:

- Slow blinking red/off: at power-on before USB initialization
- Fast blinking red/off: after the first correct communication between PC and ST-LINK
- Red on: when the initialization between the PC and ST-LINK is complete
- Green on: after a successful target communication initialization
- Blinking red/green: during communication with target
- Green on: communication finished and successful
- Orange on: communication failure

LD5 USB power fault: LD5 indicates that the power consumption on USB exceeds **500 mA**.

LD6 PWR: the green LED indicates that the STM32 part is powered, and +5 V is available.

LD7 and LD8 USB FS: A red LED LD7 and a green LED LD8 used for indications of USB OTG or device-full-speed communication.

Push-buttons

B1 USER: the user button is connected to the pin **PC13** by default (Tamper support, SB173 ON and SB180 OFF) or **PA0** (Wakeup support, SB180 ON and SB173 OFF) of the STM32 microcontroller.

B2 RESET: this push-button is connected to **NRST** and is used to RESET the STM32 microcontroller.

JP5 (IDD)

Jumper JP5, labeled IDD, is used to measure the current consumption of the STM32 microcontroller by removing the jumper and connecting an ammeter.

To get a correct current consumption, the Ethernet PHY should be set in power-down mode or SB13 (connect pin PA1 to RMII_REF_CLK) should be removed.

- JP5 ON: STM32 is powered (default)
- JP5 OFF: an ammeter must be connected to measure the STM32 current

USART Communication

- The **USART3** interface available on **PD8** and **PD9** of the STM32 can be connected either to ST-LINK or to ST morpho connector.
- The choice is changed by setting the related solder bridges (SB4, SB5, SB6, and SB7).
- By default, the USART3 communication between the target STM32 and the ST-LINK is enabled, to support the **virtual COM port**.

Pin name	Function	Virtual COM port	ST morpho connection
PD8	USART3 TX	SB5 ON and SB7 OFF	SB5 OFF and SB7 ON
PD9	USART3 RX	SB6 ON and SB4 OFF	SB6 OFF and SB4 ON

The Settings of USART3 pins
(Default: SB4, SB5, SB6, & SB7 are ON)

Controller Area Network (bxCAN)

- The three CANs (**bxCANs**) are compliant with the **2.0A and B (active)** specifications with a bitrate up to **1 Mbit/s**.
- They can receive and transmit standard frames with **11-bit identifiers** as well as extended frames with **29-bit identifiers**.
- Each CAN has **three transmit mailboxes, two receive FIFOs** with 3 stages each, and 28 shared scalable filter banks (all of them can be used even if one CAN is used).
- 256 bytes of SRAM are allocated for each CAN.

Nucleo-F767ZI

Pinout for Controller Area Network (CAN)

No Pinout:

PH_13 : CAN1_TX

PH_14 : CAN1_RX

PI_9 : CAN1_RX

PA_15 : CAN3_TX

PB_3 : CAN3_RX

PD_0 : CAN1_RX

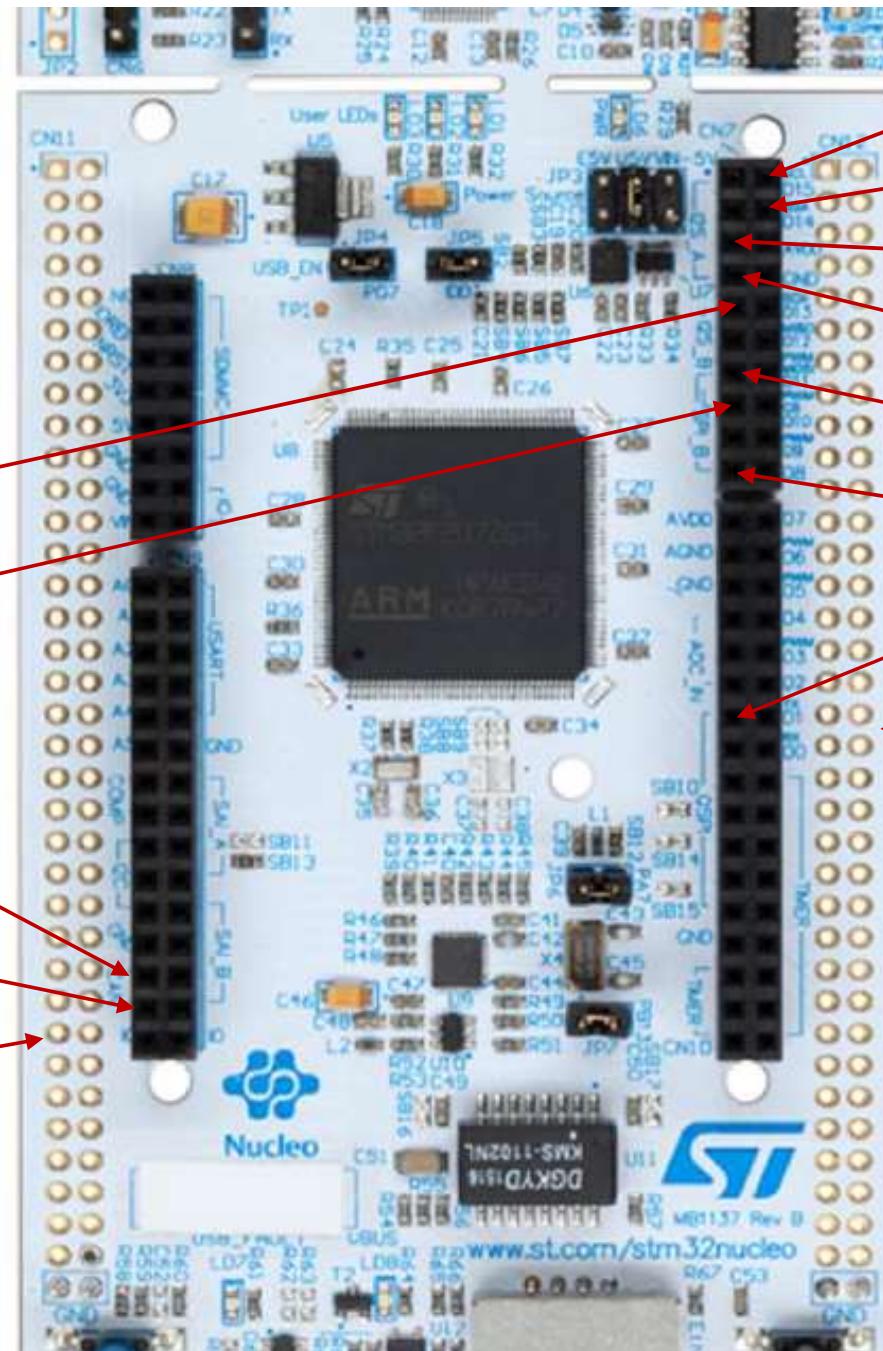
PD_1 : CAN1_TX

On CN11:

PD_0 : CAN1_RX

PD_1 : CAN1_TX

PA_15 : CAN3_TX



PB_8 : CAN1_RX

PB_9 : CAN1_TX

PB_13 : CAN2_TX

PB_12 : CAN2_RX

PB_5 : CAN2_RX

PB_4 : CAN3_TX

PB_6 : CAN2_TX

On CN12:

PB_8 : CAN1_RX

PB_9 : CAN1_TX

PA_11 : CAN1_RX

PA_12 : CAN1_TX

PB_12 : CAN2_RX

PB_13 : CAN2_TX

PB_5 : CAN2_RX

PB_6 : CAN2_TX

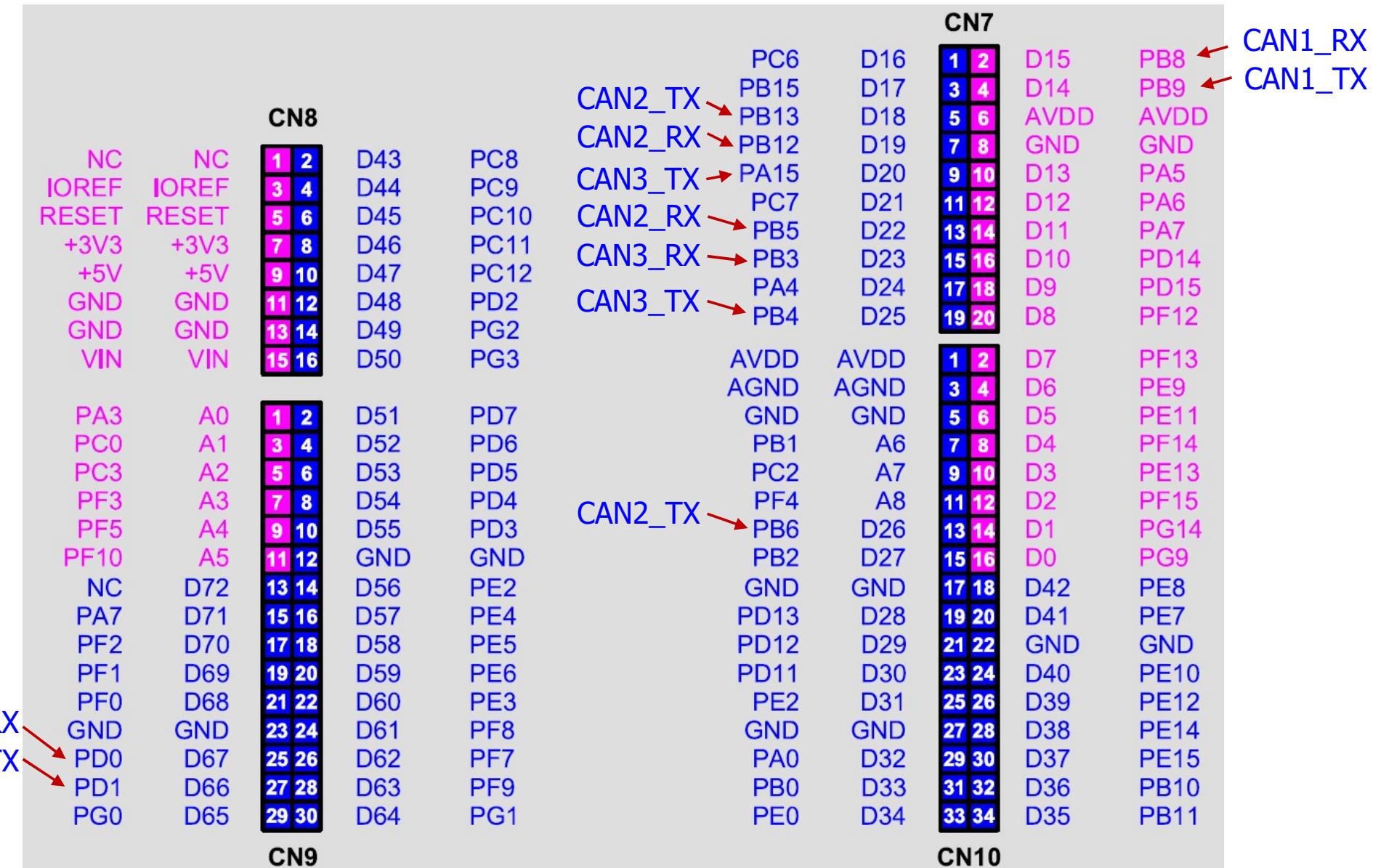
PA_8 : CAN3_RX

PB_3 : CAN3_RX

PB_4 : CAN3_TX

Nucleo-F767ZI

Pinout for Controller Area Network (CAN)



The ST Zio connectors

Ethernet MAC 10/100 with IEEE 1588

- The microcontroller provides an **IEEE-802.3-2002-compliant media access controller (MAC)** for Ethernet LAN communications through an industry-standard **medium-independent interface (MII)** or a **reduced medium-independent interface (RMII)**.
- The microcontroller requires an external **physical interface device (PHY)** to connect to the physical LAN bus (twisted-pair, fiber, etc.).
- The **PHY** is connected to the device **MII** or **RMII** port; **17 signals for MII** or **9 signals for RMII**, and it can be clocked using the **25 MHz** (MII) from the microcontroller.
- The devices include the following features:
 - Support of **10** and **100 Mbit/s** rates
 - Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
 - Tagged MAC frame support (VLAN support)
 - Half-duplex (CSMA/CD) and full-duplex operation

A virtual LAN (VLAN) is a logical overlay network that groups together a subset of devices that share a physical LAN, isolating the traffic for each group.

Ethernet MAC 10/100 with IEEE 1588

- The devices include the following features (continued):
 - MAC control sublayer (control frames) support
 - 32-bit CRC generation and removal
 - Several address filtering modes for physical and multicast address (multicast and group addresses)
 - 32-bit status code for each transmitted or received frame
 - Internal **FIFOs** to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both **2 Kbytes**.
 - Support hardware **PTP (precision time protocol)** in accordance with **IEEE 1588 2008** (PTP V2) with the time stamp comparator connected to the **TIM2** input
 - Triggers interrupt when system time becomes greater than target time

Ethernet Connection

- The board supports **10/100 Ethernet** communication by a **PHY LAN8742A-CZ-TR (U9)** and **RJ45** connector (**CN14**).
- **Ethernet PHY** is connected to the STM32 microcontroller via the **RMII interface**.
- **50MHz clock** for the STM32 microcontroller is generated by the **PHY RMII_REF_CLK**.
- On the board, **JP6** and **JP7** must be **closed** when using Ethernet.
- **Ethernet PHY LAN8742A** should be set in **power-down mode** (in this mode Ethernet PHY reference clock turns off) to achieve the expected **low-power mode current**.
- This is done by configuring Ethernet PHY LAN8742A **Basic Control Register** (at address 0x00) **Bit 11** (Power Down) to “**1**”.
- On the board, **SB13** can also be removed to get the same effect.

Nucleo-F767ZI

Ethernet Connection

Pin name	Function	Conflict with ST Zio connector signal	Configuration when using Ethernet	Configuration when using ST Zio or ST morpho connector
PA1	RMII Reference Clock	-	SB13 ON	SB13 OFF
PA2	RMII MDIO	-	SB160 ON	SB160 OFF
PC1	RMII MDC	-	SB164 ON	SB164 OFF
PA7	RMII RX Data Valid	D11	JP6 ON	JP6 OFF
PC4	RMII RXD0	-	SB178 ON	SB178 OFF
PC5	RMII RXD1	-	SB181 ON	SB181 OFF
PG11	RMII TX Enable	-	SB183 ON	SB183 OFF
PG13	RXII TXD0	-	SB182 ON	SB182 OFF
PB13	RMII TXD1	I2S_A_CK	JP7 ON	JP7 OFF

DMA: Direct Memory Access

MAC: Media Access Control

PTP: Precision Time Protocol

PMT: Power Management

MMC: MAC Management Counters

MII: Media Independent Interface

RMII: Reduced Media Independent Interface

MDC: Management Data Clock

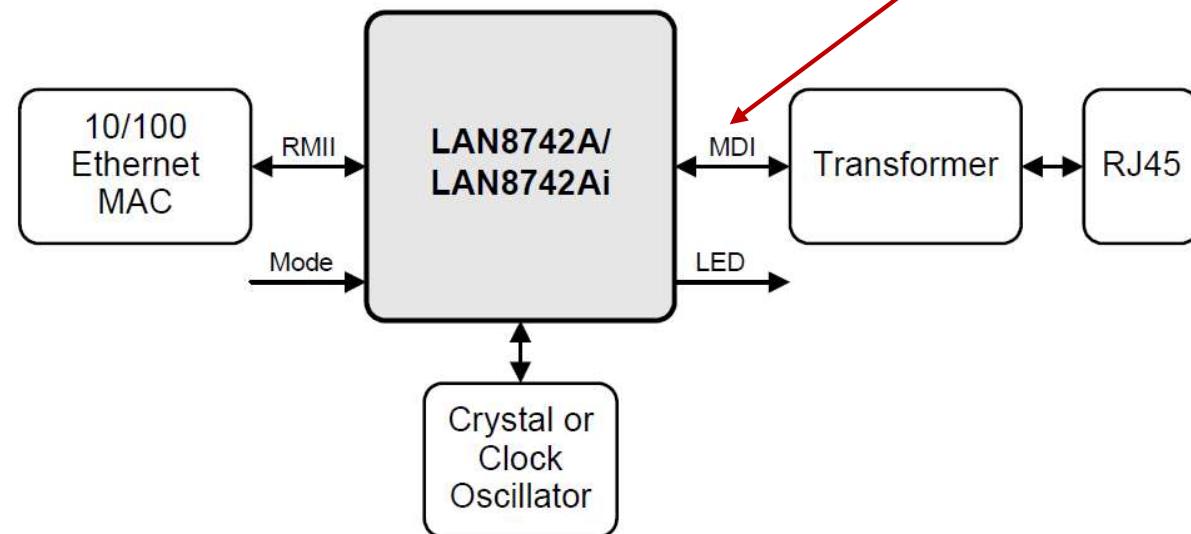
MDIO: Management Data Input/Output

PHY: Physical Layer

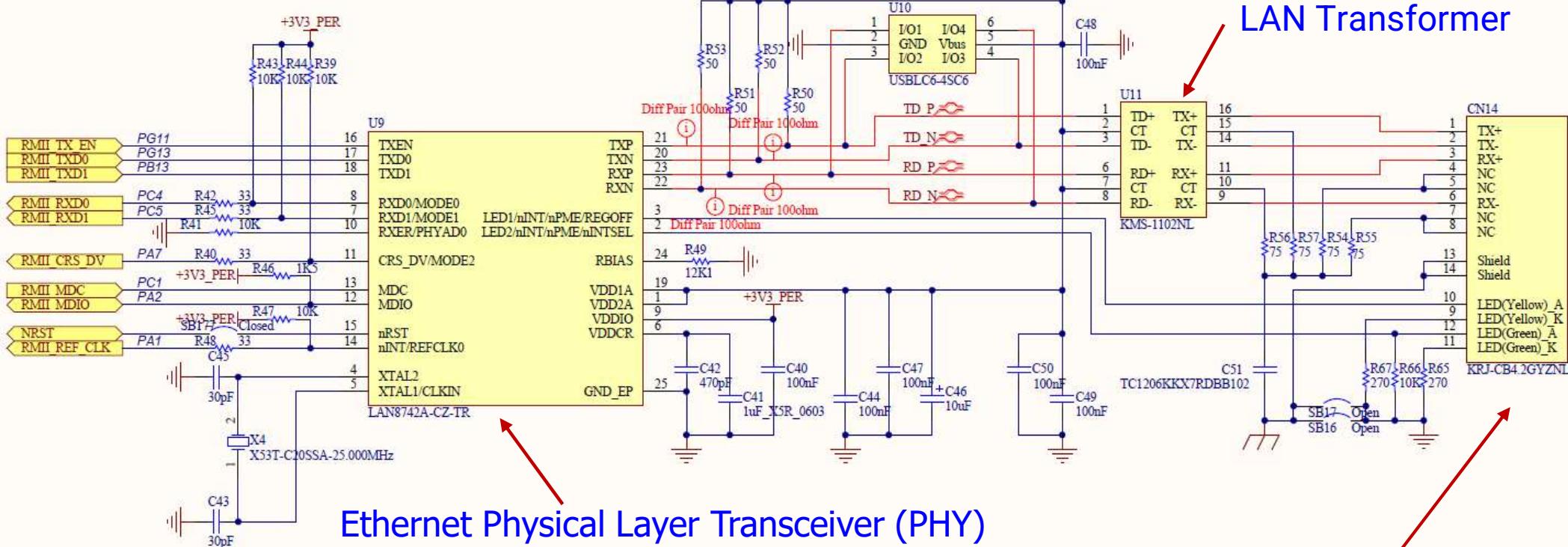
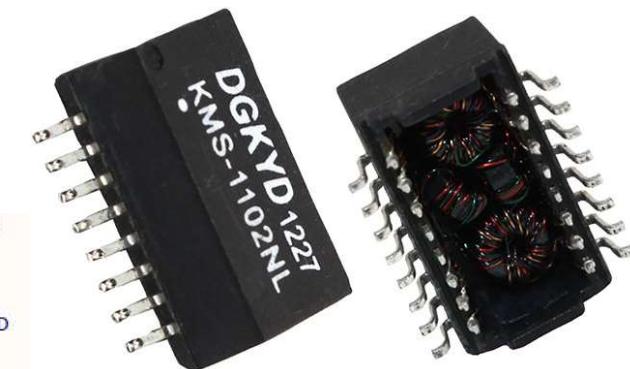
FIFO: First-In-First-Out

Ethernet PHY Connection

medium dependent interface



ESD (Electrostatic discharge)
protection of high-speed interfaces



CRS_DA = Carrier Sense /
Receive Data Valid

Liau Hwee Choo, June 2022.

The Ethernet PHY to RJ45 Connection [Ref_05-2]

Nucleo-F767ZI

Ethernet MCU Connection

SB13, removed for power-down mode

