

Efficient DAC client tests to prevent counterfeited electronics
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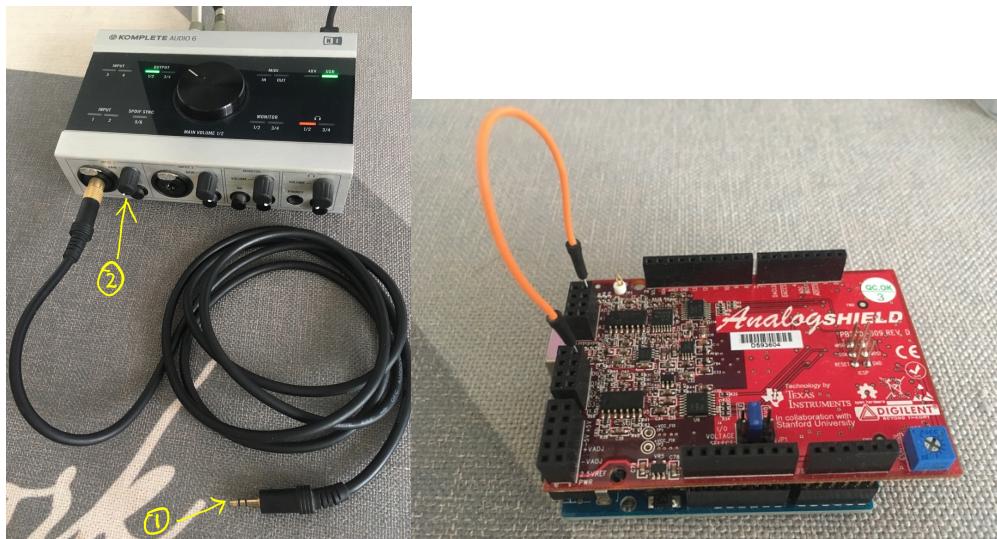
Background:

Electronics production is a collaborative effort. Manufacturers rely on suppliers for parts. Inevitably, counterfeited parts are received by the manufacturer, compromising the quality and safety of their products. The use of DAC variables widely among users and manufacturers. For example, for audio application, the customer may want high SNR, SFDR and low and a balanced output across the audio frequency spectrum. For uses in a SAR ADC, reading the input from a sensor, the user may want monotonicity to ensure safety of feedback control. Thus, an efficient testing method has to be developed for the manufacturer and their customers in order to prevent counterfeit parts, addressing a wide array of applications.

Introduction:

I developed a suite of tools with my professor Dr. Bibyk to verify the monotonicity, linearity, SNR(signal to noise ratio), and flatness of the DAC across the frequency spectrum. The testing only requires low cost hardware that can be purchased at around 100\$. This way, the user will be able to easily test their DAC, preventing counterfeited parts. The testing will take less than 5 minutes on a single DAC. Therefore, the manufacturers will also be able to rule out counterfeited parts to improve their quality control on a mass scale. However, this testing tool is not intended for characterization of the DAC. Thus, instead of printing out precise data, scattered plot is used as the output of the testing tool, to ensure intuitive and fast interpretation. Due to the limitation of the testing hardware, the testing tool is designed to test 16 bit 44.1kHz DAC.

Testing Hardware and software:



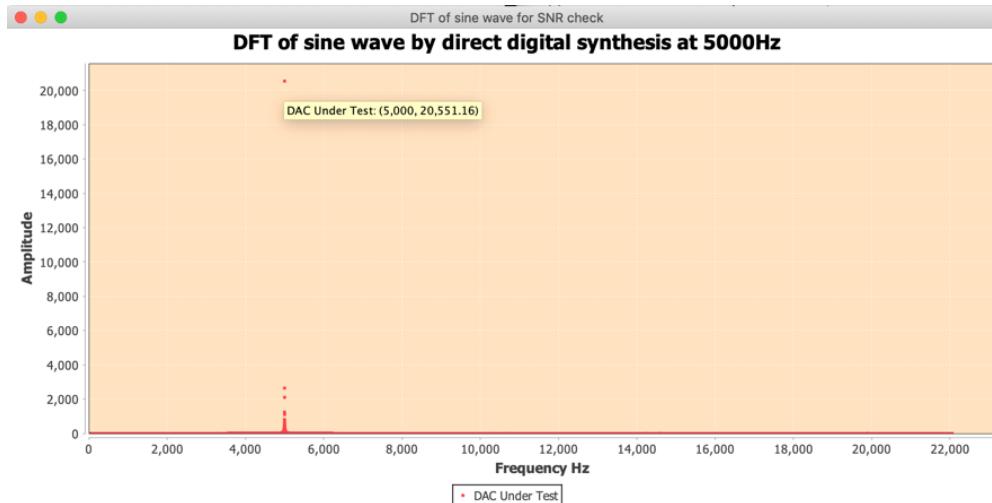
Hardware list:

1. One USB audio interface with a built-in pre-amp and analog gain control②, and 24bit, 44.1kHz sampling rate Delta-sigma ADC.
2. One cable and the necessary adapter to connect the DAC under test①.
3. Arduino UNO and Analog shield.
4. Cable and the necessary adapter to connect the DAC under test.

SNR Testing theory and testing procedure:



Software interface for SNR and frequency response flatness test



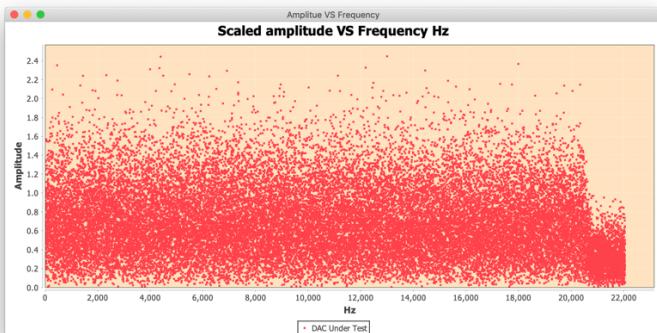
DFT plot for SNR test

To test the SNR of a DAC, cable① is connected to the ADC on the audio interface, a pure wave at 5000Hz generated by direct digital synthesis at 16bit 44.1kHz is output from the DAC under test. Adjusting the gain on the pre-amp, the sine wave output from the DAC so that the signal can hit most full range of the 24bit ADC with clipping.

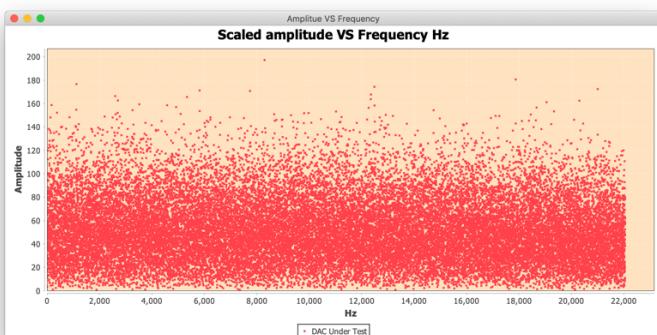
Then the program records the reading from the ADC. The DFT, discrete Fourier transform, is performed based on the recorded data from the ADC. The result of the DFT is shown on a plot. Ideally, there will be only a single point at 5000Hz, however, if the DAC has low SNR caused by non-linearity, spurs will show up at frequency other than 5000Hz, the DFT plot will also contain a high noise floor.

An FFT version of SNR test is also provided by the tool which allows the user to obtain the plot in under 10 seconds. It can be useful if testing speed is important to the user. However, the plot will not be as accurate because of frequency leakage. Because FFT can only take 2^n number of samples as input, however 44.1kHz is not power of two. Therefore, 5000Hz will not exactly fit into a single frequency bin of the FFT output, thus inducing frequency bin leakage. The plot will become falsely more noisy.

Output Flatness and frequency response Testing theory and procedure:



Frequency response of the built-in DAC from a 2017 27inch iMac



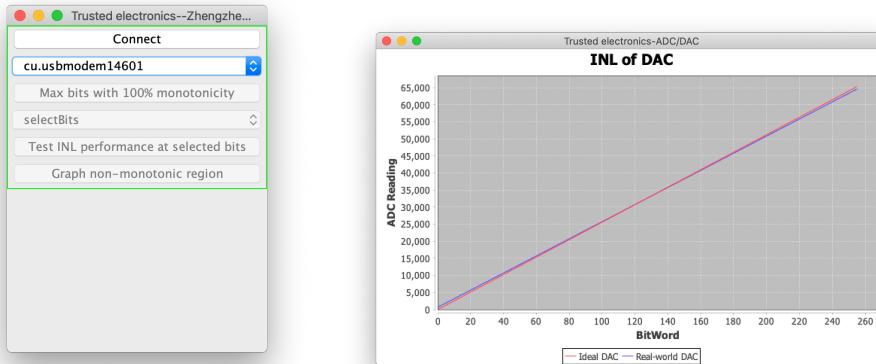
Frequency response of the professional level DAC provided by Texas instrument

White noise is the type of noise that has constant amplitude across the entire frequency spectrum. Thus, white noise is chosen to be the output of the DAC under test. First, the white noise is generated through direct signal synthesis. A random number generator algorithm is used to generate all the sample value to feed into the output of the DAC. The ADC records the white noise, and the FFT is performed to produce the plot on the frequency spectrum.

For audio application, ideally the perfectly flat frequency response is preferred. Looking at the result of the testing tool, for example, the built-in DAC on the iMac has attenuated frequency response from 20500Hz upwards. Whereas the professional level DAC by Texas instrument has a near flat response from 0–22000Hz.

Monotonicity fast testing (under development).....

Monotonicity and static INL testing (Brute force method, necessary but slow)



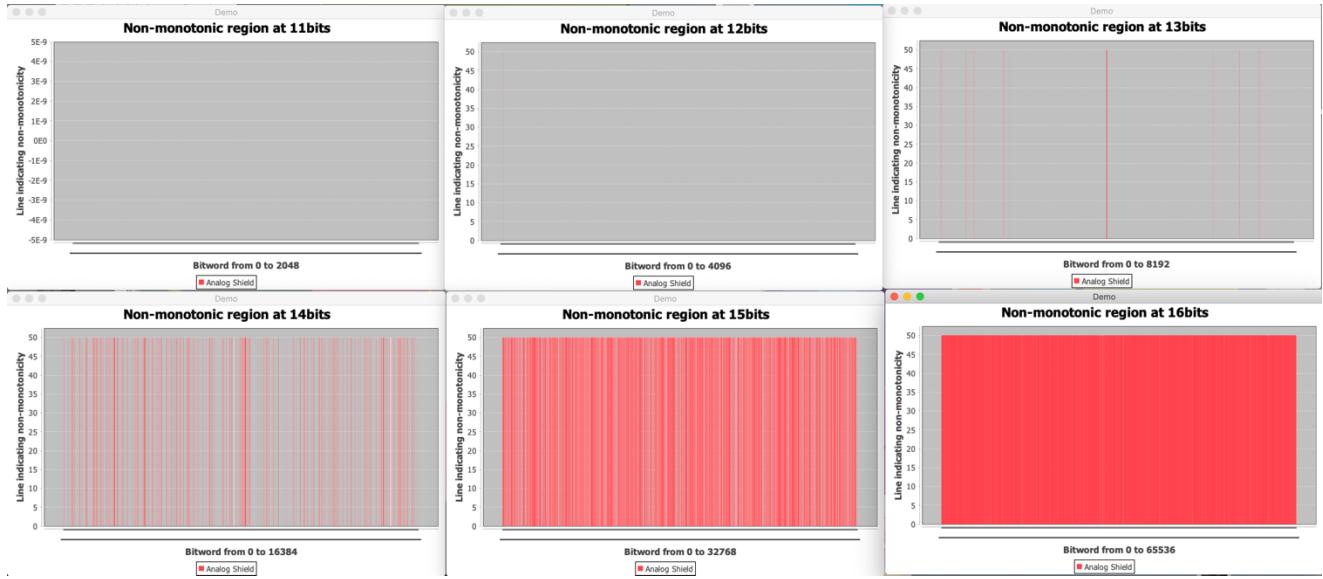
Software interface

Static INL test plot

Brute force testing requires direct access to the DAC. Therefore, the Arduino microcontroller is used, driving the analog shield, and communicating back to the computer running the testing software. For each level of precision, a different step size is used. For example, a 16bit DAC has 65536 incremental output voltage level. If the user opts to test the monotonicity at 16bit precision, the step size will be 1, the firmware on the Arduino would sweep the input to the DAC from 0 to 65536. If the user opts for 15bit, then the step size will be 2, effectively reducing the number of output voltage level to 32768. The software then marks the non-monotonic region if the ADC reading the output from DAC finds that the output voltage decreases rather than increases.

Why Brute force Monotonicity testing? Theory and procedure:

For application with feedback control, maintaining monotonicity is essential. However, it is often difficult for the user know to what extent is the DAC monotonic since such specification is often not disclosed on the data sheet. In addition, most algorithm would tell the user that the DAC under test is monotonic to N number of bits. However, often times, only certain LSB is non-monotonic, the rest of the output value is monotonic. If the non-monotonic region appears within the range unlikely to be used by the user, the DAC can still be treated as monotonic for the specific application, improve yield rate for the manufacturer, in most case, double the precision for the user while retaining monotonicity.



For instance, the DAC under test built-in to the analog shield is completely monotonic as a 11bit DAC. However, when tested as 12bit DAC, one non-monotonic region appears. However, the non-monotonic region appears at a relatively low voltage level. Thus, if application permits, the user can comfortably use the DAC under test as a 12bit DAC.

Work cited

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