EE214: Combinational Circuits-1

Wadhwani Electronics Lab, IIT Bombay

Thursday 28th January, 2021

1 Part-1: 4-bit adder (Simulation should have been attempted as homework. Results to be demonstrated in the lab today)

1. You have been given a full adder description in the reference design during the tutorial session. Using this full adder as a component, describe a 4-bit ripple carry adder in VHDL. You may ignore input carry of LSB full adder.

   Note that it is a simple binary adder that can be implemented by cascading four 1-bit full adders such that the the carry generated by the addition of lower significant bits forms the incoming carry for addition of the next significant bits.

2. Simulate the adder using the generic testbench to confirm the correctness of your description. To do this, note that you need to generate the tracefile for all 256 combinations and modify the testbench given to you appropriately.

3. *Map your logic circuit to the Krypton board. You will use the on-board 8 switches to input the bits to your circuit, and 5 on-board LED's to observe the outputs of your circuit. Confirm that the post-synthesis gate level netlist functions correctly.

4. *Program the Krypton board and demonstrate to the TA the working of the 4-bit adder.

* To be attempted after the tutorial on "Using Krypton".

2 Part-2: A simple combinational circuit

You are given the following specification of a combinational circuit: the circuit has 8 inputs $x_7, x_6, x_5, x_4, \ldots x_0$ and two outputs y_1, y_0. The output bit y_1 is 1 if and only if the number of input bits that are 1 is greater than the number of input bits that are 0. The output bit y_0 is the complement of y_1.

1. Design a logic circuit and draw a schematic which meets the specification. You are allowed to use AND, OR, NOT, XOR gates, or Full Adder to implement your design. (3)

2. Confirm your design with your TA.

3. Describe the logic circuit in VHDL and construct a tracefile which tries all 256 input combinations. (3+3)
   The format for tracefile should be
   $< x_7x_6x_5x_4x_3x_2x_1x_0 >< space >< y_1y_0 >< space >< mask - bits >$.

4. Simulate the circuit with the generic test-bench and confirm that your circuit functions correctly.

5. *Map your logic circuit to the Krypton board. You will use the on-board switches to input the bits to your circuit, and the on-board LED's to observe the outputs of your circuit. Confirm that the post-synthesis gate level netlist functions correctly. (3)

6. *Program the Krypton board and demonstrate to the TA that your implementation works correctly. (3)

7. Submit the report that includes the logic circuit designed, the screenshot of RTL viewer, waveforms, VHDL code **(well commented)**, python script/ C program for trace file, trace file, and the post synthesis report for **both the parts**. The report is to be submitted on moodle and it is mandatory. (10)

* To be attempted after the tutorial on "Using Krypton".