

CHANGE NOTICE: SUPER ELF PC BOARD V1.0

1. The following changes must be made prior to the first application of power. On the back of the board--

- A. Add a jumper between U13 pin 8 and U6 pin 20. (Use the No. 26 wire supplied).
- B. Cut the trace between U10 pin 4 and U10 pin 10.
- C. Add a jumper between U10 pin 4 and U11 pin 10.

2. The following changes are associated with the expansion bus and are optional.

A. The data lines going to the expansion bus connector are incorrectly wired. Cut the traces (on the back of the board) between the 50 pin connector and the display drivers. The pins affected are 22, 23, 24, 25, 47, 48, 49, 50. Connect 8 jumpers per this table:

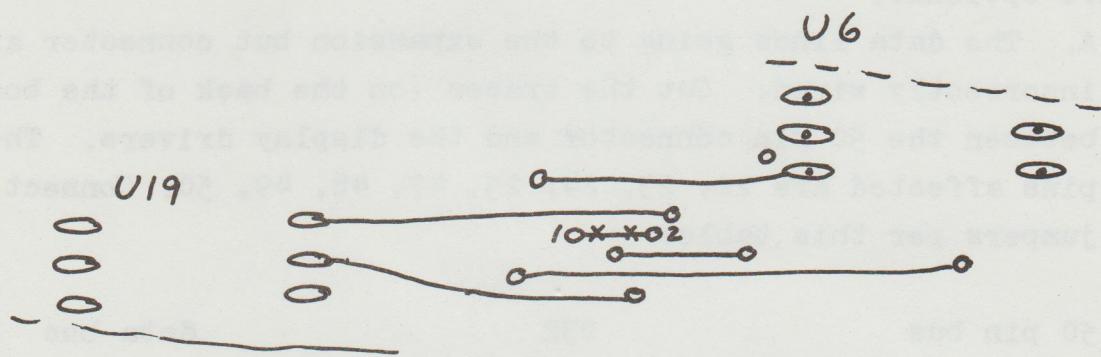
50 pin bus <u>PIN NO.</u>	U32 <u>PIN NO.</u>	data bus <u>ID</u>
22	9	D7
23	7	D6
24	6	D5
25	5	D4
47	4	D3
48	3	D2
49	2	D1
50	1	D0

B. The DMAIN function cannot be used without providing circuit isolation. This requires the following changes:

- ✓ (1) Cut the trace on the back of the board between holes No. 1 and No. 2 as shown on the sketch.
- ✓ (2) Solder a 1N914 Diode in the two above holes with the cathode (banded) end in hole No. 1.
- ✓ (3) Connect a 47 K OHM resistor between U6 pin 38 and U6 pin 40.

3. PARTS LIST

- | | |
|-----------------------------------------|-----------------|
| (1) 1N914 | Diode |
| (1) 47K OHM | ½ watt resistor |
| (2 ft) No. 26 solid wire (twisted pair) | |



SKETCH (Back of Board)

4. Memory Saver Option modification.

A. On the front of the board, cut the trace between
U6 Pin 40 and R1.

B. Connect this end of R1 to the + end of C1.

5. Some brands of 4093 do not 'debounce' as well as others.
Replacing C18 with a 1.0 mfd capacitor will cure double input
pulses. The plus side of C18 is nearest the letters C18.
Replacing C17 with a 1.0 mfd capacitor will cure double stepping
in the single step mode. The plus side of C17 is nearest the
letters C17.



OPTIONS

The following options are avialble and the SUPER ELF circuit board has been designed so all you have to do is add the parts to the board in the provided holes, solder and RUN !

1. Memory Saver \$4.95

This option is a NI-CAD Battery pack which is automatically charged by the ELF power supply. It keeps the memory powered for up to 20 hours without being plugged into the 110V 60 cycle outlet. Now you can load a program and unplug your SUPER ELF and take it to work, a friends house etc., and plug it in and still have your program loaded.

PLEASE NOTE: Memory may be retained for minimum of 4 weeks typically, using the battery backup option with P5101L CMIS low power RAM's in place of the 2101 RAM's. If you have already purchased the option with 2102's we will exchange them for 2 - P5101L at an additional cost of \$18.90. The price of the battery option kit with P5101L RAM's is \$23.85.

2. LOW Address Display (lower 2 Digits) \$9.95

This option allows you to display the Lower 8 Bit Address BUS. Now you no longer need to have any doubt about the current Address.

3. HI Address Latch and Display (higher 2 Digits) \$8.95

This option latches the HI Address and provides Buffered outputs to the expansion connectors. In addition the HI Address is displayed. The LO Address Display option must also be installed.

4. EXPANSION BUS Connectors Price available at a later date

The SUPER ELF Board has provisions for one P C Card connector (Standard 44 Pin) for expansion and also a flat cable connector for expansion to our own SUPER ELF Expander card. This card is in development and will fit inside the available custom Hardwood Case and provide 16 times the memory plus a super 1K monitor and other features to be announced.

5. Custom Case \$19.75

A Hardwood Walnut Finish Case with Plastic Front is completely finished. Our expander board is designed to fit in this case also. Case size approx. 9" X 11" X 2".



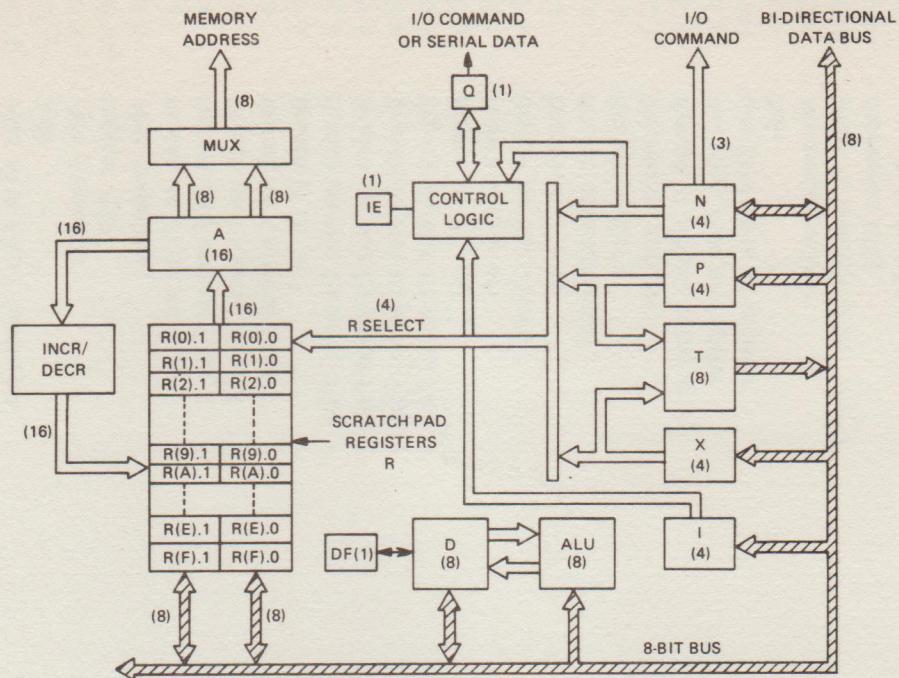
TO: QUEST Super Elf Customers

The data enclosed is incomplete but should be adequate for assembly and operation. The section on logic and troubleshooting and Appendix B will be mailed to you as soon as final revision is completed.

Thank you for your patience. We are very sorry for the long delay in shipping your Super Elf kit. We thought you would like to have the kit itself now, rather than wait for the final revision of the manual. The final pages will be mailed shortly.

A handwritten signature in cursive ink that reads "Roger P. Pitkin".

Roger P. Pitkin
President



- Internal structure of the CDP 1802 Microprocessor.

.. PROGRAM 2.1 -- MEMORY CLEAR

```

0000 90 CLEAR GHI 0 .. REGISTER 0 HAS 0001
0001 AE PLO 14 .. MAKE RE=0000
0002 BE PHI 14
0003 EE LOOP SEX 14 .. EACH TIME, R14 IS -1
0004 73 STXD .. D STILL HAS 00
0005 30 BR LOOP .. GO BACK FOR ANOTHER
0006 03

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.. PROGRAM 2.2 -- MEMORY SEQUENCER

```

0000 90 SEQ GHI 0 .. THIS PART IS
0001 AE PLO 14 .. JUST LIKE CLEAR
0002 BE PHI 14
0003 EE LOOP SEX 14
0004 8E GLO 14 .. THIS IS ADDRESS VALUE
0005 73 STXD .. SO DATA=ADDRESS
0006 30 BR LOOP .. REPEAT UNTIL DONE
0007 03

```

.. PROGRAM 2.3 -- SLOW BLINK

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0000 91 BLINK GHI 1 .. LOOK AT TIMER IN 1
0001 CE LSZ .. IS ZERO ONLY 1/256
0002 7A REQ .. IF NOT 00, Q OFF
0003 38 SKP
0004 7B SEQ .. WHILE ZERO, Q ON
0005 11 INC 1 .. BUMP COUNTER
0006 30 BR BLINK .. THEN REPEAT.
0007 00

```



NETRONICS RESEARCH AND DEVELOPMENT LIMITED
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APPENDIX A

INSTRUCTION SUMMARY

MNEM	NAME	OPCODE	PAGE				F8	bb	31
ADC —	ADD with Carry	74	42	LDI b	Load D Immediate		Or	35	
ADCI b	ADD with Carry Immediate	7C bb	42	LDN r	Load D via N $1 \leq r \leq F$		F0	35	
ADD —	Add	F4	41	LDX —	Load D via R(X)		72	35	
ADI b	ADD Immediate	FC bb	42	LDXA —	Load D via R(X)Advance		CF	42	
AND —	Logical AND	F2	39	LSDF —	Long Skip if DF is 1		CC	53	
ANI b	ANd Immediate	FA bb	40	LSIE —	Long Skip if Interrupts are Enabled		C8	22	
B1 a	Branch on External Flag 1	34 aa	16	LSKP —	Long Skip		C7	42	
B2 a	Branch on External Flag 2	35 aa	16	LSNF —	Long Skip if DF is 0		C5	25	
B3 a	Branch on External Flag 3	36 aa	16	LSNQ —	Long Skip if Q is off		C6	24	
B4 a	Branch on External Flag 4	37 aa	16	LSNZ —	Long Skip if Not Zero		CD	25	
BDF a	Branch if DF is 1	33 aa	41	LSQ —	Long Skip if Q is on		CE	24	
BN1 a	Branch on Not External Flag 1	3C a7	17	LSZ —	Long Skip if Zero		C4	22	
BN2 a	Branch on Not External Flag 2	3D aa	17	MARK —	Save X & P		F1	38	
BN3 a	Branch on Not External Flag 3	3E aa	17	NOP —	No Operation		F9 bb	39	
BN4 a	Branch on Not External Flag 4	3F aa	17	OR —	Logical OR		6p	20	
BNF a	Branch if DF is 0	3B aa	42	ORI b	OR Immediate		Br	29	
BNQ a	Branch if Q is off	39 aa	25	OUT p	Output from memory; $1 \leq p \leq 7$		Ar	29	
BNZ a	Branch on Not Zero	3A aa	23	PHI r	Put D into Hlgh byte of register		7A	15	
BQ a	Branch if Q is on	31 aa	25	PLO r	Put into LOw byte of register		70	53	
BR a	Branch unconditionally	30 aa	18	REQ —	Reset Q		78	56	
BZ a	Branch on Zero	32 aa	23	RET —	RETurn		F5	43	
DEC r	Decrement register	2r	27	SAV —	SAVE T		75	46	
DIS —	Return & DISable interrupts	71	53	SD —	Subtract D from memory		7D bb	46	
GHI r	Get Hlgh byte of register	9r	29	SDB —	Subtract D from memory with Borrow		FD bb	44	
GLO r	Get LOw byte of register	8r	29	SDBI b	Subtract D from Immediate byte with Borrow		Dr	52	
IDL —	Idle	00	14	SDI b	Subtract D from Immediate byte		7B	14	
INC r	Increment register	1r	27	SEP r	SEt P		FE	47	
INP p	Input to memory & D; $9 \leq p \leq F$	6p	20	SEQ —	Set Q		7E	47	
IRX —	Increment R(X)	60	35	SHL —	SHift D Left		F6	48	
LBDF aa	Long Branch if DF is 1	C3 aaaa	42	SHLC —	SHift D Left with Carry		76	48	
LBNF aa	Long Branch if DF is 0	CB aaaa	42	SHR —	SHift D Right		38	22	
LBNQ aa	Long Branch if Q is off	C9 aaaa	24	SHRC —	SHift D Right with Carry		F7	46	
LBNZ aa	Long Branch if Not Zero	CA aaaa	23	SKP —	Skip one byte		77	46	
LBQ aa	Long Branch if Q is on	C1 aaaa	24	SM —	Subtract Memory byte from D		7F bb	46	
LBR aa	Long Branch unconditionally	C0 aaaa	18	SMB —	Subtract Memory byte from d with Borrow		FF bb	46	
LBZ aa	Long Branch if Zero	C2 aaaa	23	SMBI b	Subtract Immediate Memory from D with Borrow		5r	32	
LDA r	Load D & Advance	4r	34	SM I b	Subtract Immediate Memory from D		73	33	
				STR r	SToRe D into memory		F3	39	
				STXD —	STore D via R(X) & Decrement		FB bb	40	
				XOR —	EXclusive OR				
				XRI b	EXclusive OR Immediate				

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wired & tested	\$89.95				
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QUANTITY ORDERED	QUANTITY SHIPPED	QUANTITY BACK ORDERED	ITEM/DESCRIPTION	UNIT PRICE	AMOUNT
1	1		4K ELF EXP KIT	PB 9.9.	79.95
1	1		1K SUPER ROM MON	11-9.	19.95
1	1		PARALLEL I O PORT	PB 12.8	7.95
1	1		S 100 MEMORY IO	MAIL	4.50
1	1		QUESTDATA CATALOG	9/15	12.00
					NC

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1	1	+	catalog		N/C
1	1	+	Super Elf kit	106.95	106.95
1	1	+	cabinet for Elf Super	15.00	15.00
			B/C TILL OCT 20. SCR FOR THE DELAY		
			QUEST		
			SHIPPED MANUAL SPEAKER		
					DEC 15 1977

Note: We cannot ship UPS to P.O. Boxes
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 2-3 WEEKS

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1	1		4K EXP.		
1	1		1K SUP. Rom		

P.B.

 B. of A.
 & DATE:
 MC
 & DATE:

No.Q

FREIGHT	
INSURANCE	

SALES TAX	
CHECK	MONEY ORDER
CASH	C.O.D.
TOTAL	

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Oct. 30, 1978

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YOUR INDUCE # 42202. (THE QUESTDAYA
IS BEING RECEIVED BUT NO PART) BACK ORDERED
I HAVE NOT RECEIVED ANY OF THE PARTS. ~~YET~~
CAN YOU ^{GIVE ME} INDICATE A SHIPPING DATE FOR
THESE PARTS?

THANK YOU.

SINCERELY YOURS

R. HEPPEL

CODING FORM

Program Name _____ Date _____ Page ____ of ____

<u>LOCATION</u>	<u>CODE</u>	<u>LABEL</u>	<u>MNEMONIC</u>	<u>OPERAND</u>	<u>COMMENTS</u>
0					
1					
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