

## CHANGE NOTICE: SUPER ELF PC BOARD V1.0

1. The following changes must be made prior to the first application of power. On the back of the board--

- A. Add a jumper between U13 pin 8 and U6 pin 20. (Use the No. 26 wire supplied).
- B. Cut the trace between U10 pin 4 and U10 pin 10.
- C. Add a jumper between U10 pin 4 and U11 pin 10.

2. The following changes are associated with the expansion bus and are optional.

A. The data lines going to the expansion bus connector are incorrectly wired. Cut the traces (on the back of the board) between the 50 pin connector and the display drivers. The pins affected are 22, 23, 24, 25, 47, 48, 49, 50. Connect 8 jumpers per this table:

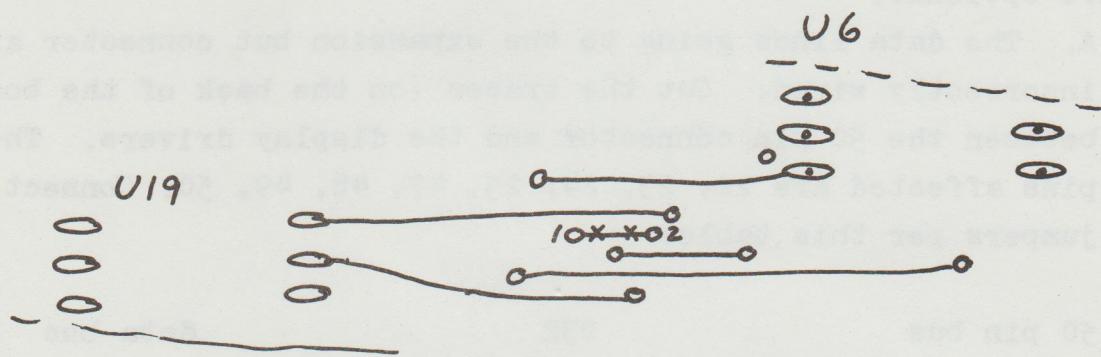
50 pin bus <u>PIN NO.</u>	U32 <u>PIN NO.</u>	data bus <u>ID</u>
22	9	D7
23	7	D6
24	6	D5
25	5	D4
47	4	D3
48	3	D2
49	2	D1
50	1	D0

B. The DMAIN function cannot be used without providing circuit isolation. This requires the following changes:

- ✓ (1) Cut the trace on the back of the board between holes No. 1 and No. 2 as shown on the sketch.
- ✓ (2) Solder a 1N914 Diode in the two above holes with the cathode (banded) end in hole No. 1.
- ✓ (3) Connect a 47 K OHM resistor between U6 pin 38 and U6 pin 40.

## 3. PARTS LIST

- |   |                 |
|---|-----------------|
| (1) 1N914                               | Diode           |
| (1) 47K OHM                             | ½ watt resistor |
| (2 ft) No. 26 solid wire (twisted pair) |                 |



SKETCH (Back of Board)

## 4. Memory Saver Option modification.

A. On the front of the board, cut the trace between U6 Pin 40 and R1.

B. Connect this end of R1 to the + end of C1.

## 5. Some brands of 4093 do not 'debounce' as well as others.

Replacing C18 with a 1.0 mfd capacitor will cure double input pulses. The plus side of C18 is nearest the letters C18. Replacing C17 with a 1.0 mfd capacitor will cure double stepping in the single step mode. The plus side of C17 is nearest the letters C17.



## OPTIONS

The following options are avialble and the SUPER ELF circuit board has been designed so all you have to do is add the parts to the board in the provided holes, solder and RUN !

1. Memory Saver \$4.95

This option is a NI-CAD Battery pack which is automatically charged by the ELF power supply. It keeps the memory powered for up to 20 hours without being plugged into the 110V 60 cycle outlet. Now you can load a program and unplug your SUPER ELF and take it to work, a friends house etc., and plug it in and still have your program loaded.

**PLEASE NOTE:** Memory may be retained for minimum of 4 weeks typically, using the battery backup option with P5101L CMIS low power RAM's in place of the 2101 RAM's. If you have already purchased the option with 2102's we will exchange them for 2 - P5101L at an additional cost of \$18.90. The price of the battery option kit with P5101L RAM's is \$23.85.

2. LOW Address Display (lower 2 Digits) \$9.95

This option allows you to display the Lower 8 Bit Address BUS. Now you no longer need to have any doubt about the current Address.

3. HI Address Latch and Display (higher 2 Digits) \$8.95

This option latches the HI Address and provides Buffered outputs to the expansion connectors. In addition the HI Address is displayed. The LO Address Display option must also be installed.

4. EXPANSION BUS Connectors Price available at a later date

The SUPER ELF Board has provisions for one P C Card connector (Standard 44 Pin) for expansion and also a flat cable connector for expansion to our own SUPER ELF Expander card. This card is in development and will fit inside the available custom Hardwood Case and provide 16 times the memory plus a super 1K monitor and other features to be announced.

5. Custom Case \$19.75

A Hardwood Walnut Finish Case with Plastic Front is completely finished. Our expander board is designed to fit in this case also. Case size approx. 9" X 11" X 2".



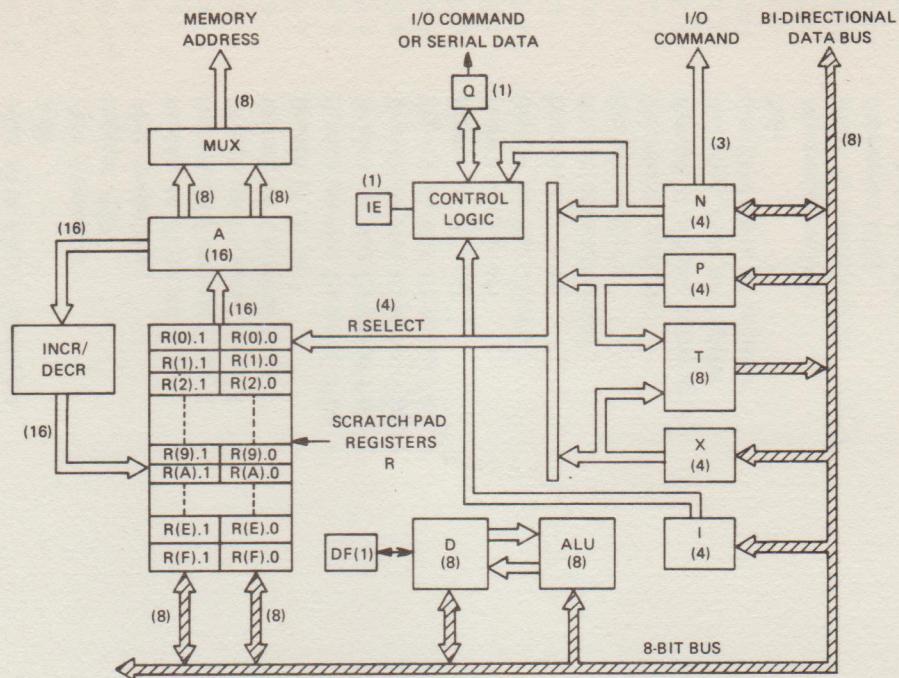
TO: QUEST Super Elf Customers

The data enclosed is incomplete but should be adequate for assembly and operation. The section on logic and troubleshooting and Appendix B will be mailed to you as soon as final revision is completed.

Thank you for your patience. We are very sorry for the long delay in shipping your Super Elf kit. We thought you would like to have the kit itself now, rather than wait for the final revision of the manual. The final pages will be mailed shortly.

A handwritten signature in cursive ink that reads "Roger P. Pitkin".

Roger P. Pitkin  
President



- Internal structure of the CDP 1802 Microprocessor.

.. PROGRAM 2.1 -- MEMORY CLEAR

```

0000 90 CLEAR GHI 0 .. REGISTER 0 HAS 0001
0001 AE PLO 14 .. MAKE RE=0000
0002 BE PHI 14
0003 EE LOOP SEX 14 .. EACH TIME, R14 IS -1
0004 73 STXD .. D STILL HAS 00
0005 30 BR LOOP .. GO BACK FOR ANOTHER
0006 03

```

.. PROGRAM 2.2 -- MEMORY SEQUENCER

```

0000 90 SEQ GHI 0 .. THIS PART IS
0001 AE PLO 14 .. JUST LIKE CLEAR
0002 BE PHI 14
0003 EE LOOP SEX 14
0004 8E GLO 14 .. THIS IS ADDRESS VALUE
0005 73 STXD .. SO DATA=ADDRESS
0006 30 BR LOOP .. REPEAT UNTIL DONE
0007 03

```

.. PROGRAM 2.3 -- SLOW BLINK

```

0000 91 BLINK GHI 1 .. LOOK AT TIMER IN 1
0001 CE LSZ .. IS ZERO ONLY 1/256
0002 7A REQ .. IF NOT 00, Q OFF
0003 38 SKP
0004 7B SEQ .. WHILE ZERO, Q ON
0005 11 INC 1 .. BUMP COUNTER
0006 30 BR BLINK .. THEN REPEAT.
0007 00

```



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## APPENDIX A

### INSTRUCTION SUMMARY

MNEM	NAME	OPCODE PAGE	LDI b	Load D Immediate
ADC —	ADD with Carry	74	42	LDN r
ADCI b	ADD with Carry Immediate	7C bb	42	Load D via N $1 \leq r \leq F$
ADD —	Add	F4	41	LDX —
ADI b	ADD Immediate	FC bb	42	Load D via R(X)Advance
AND —	Logical AND	F2	39	LSDF —
ANI b	AND Immediate	FA bb	40	LSIE —
B1 a	Branch on External Flag 1	34 aa	16	LSKP —
B2 a	Branch on External Flag 2	35 aa	16	LSNF —
B3 a	Branch on External Flag 3	36 aa	16	LSNQ —
B4 a	Branch on External Flag 4	37 aa	16	LSNZ —
BDF a	Branch if DF is 1	33 aa	41	LSQ —
BN1 a	Branch on Not External Flag 1	3C a7	17	LSZ —
BN2 a	Branch on Not External Flag 2	3D aa	17	MARK —
BN3 a	Branch on Not External Flag 3	3E aa	17	NOP —
BN4 a	Branch on Not External Flag 4	3F aa	17	OR —
BNF a	Branch if DF is 0	3B aa	42	ORI b
BNQ a	Branch if Q is off	39 aa	25	OUT p
BNZ a	Branch on Not Zero	3A aa	23	PHI r
BQ a	Branch if Q is on	31 aa	25	PLO r
BR a	Branch unconditionally	30 aa	18	Put D into HIgh byte of register
BZ a	Branch on Zero	32 aa	23	Put into LOW byte of register
DEC r	Decrement register	2r	27	Reset Q
DIS —	Return & DISable interrupts	71	53	RET —
GHI r	Get HIgh byte of register	9r	29	RETurn
GLO r	Get LOW byte of register	8r	29	SAV —
IDL —	Idle	00	14	SD —
INC r	Increment register	1r	27	SDB —
INP P	Input to memory & D; $9 \leq p \leq F$	6p	20	Subtract D from memory with Borrow
IRX —	Increment R(X)	60	35	Subtract D from Immediate byte with Borrow
LBDF aa	Long Branch if DF is 1	C3 aaaa	42	SET P
LBFI aa	Long Branch if DF is 0	CB aaaa	42	SDBI b
LBHQ aa	Long Branch if Q is off	C9 aaaa	24	SDI b
LBNZ aa	Long Branch if Not Zero	CA aaaa	23	SEP r
LBQ aa	Long Branch if Q is on	C1 aaaa	24	SEQ —
LBQ aa	Long Branch unconditionally	C0 aaaa	18	Set Q
LBZ aa	Long Branch if Zero	C2 aaaa	23	SHL —
LDA r	Load D & Advance	4r	34	SHLC —
				Shift D Left with Carry
				SHR —
				Shift D Right
				SHRC —
				Shift D Right with Carry
				SKP —
				Skip one byte
				SM —
				Subtract Memory byte from D
				SMB —
				Subtract Memory byte from d with Borrow
				Subtract Immediate Memory from D with Borrow
				Subtract Immediate Memory from D
				SToRe D into memory
				SToD via R(X) & Decrement
				Store D via R(X)
				XOR —
				EXclusive OR Immediate

LDI b	31	F8 bb
LDN r	35	0r
LDX —	35	CF
LDXA —	35	FO
LSDF —	35	CC
LSIE —	35	53
Load D via R(X)	35	C8
Load D via N $1 \leq r \leq F$	35	22
Long Skip if DF is 1	35	C7
Long Skip if Interrupts are Enabled	35	42
Long Skip if DF is 0	35	C5
Long Skip if Q is off	35	24
Long Skip if Not Zero	35	CD
Long Skip if Q is on	35	25
Long Skip if Zero	35	CE
Save X & P	35	24
No Operation	35	79
Logical OR	38	C4
OR Immediate	39	F1
Output from memory; $1 \leq p \leq 7$	20	F9 bb
Put D into HIgh byte of register	20	6p
Put into LOW byte of register	20	Br
Reset Q	29	29
RETurn	29	AT
RETurn	15	7A
SAV T	53	15
Subtract D from memory	56	78
Subtract D from memory with Borrow	43	F5
Subtract D from Immediate byte with Borrow	46	75
Subtract D from Immediate byte	46	7D bb
SEt P	46	Dr
SDI b	46	52
SDB —	46	7B
SDBI b	46	44
SDI b	46	FD bb
SEP r	46	52
SEQ —	46	7B
Set Q	46	14
SHL —	47	FE
SHLC —	47	7E
SHR —	47	47
Shift D Right	48	F6
Shift D Left	48	48
Shift D Right with Carry	48	76
Shift D Left with Carry	48	76
Skip one byte	22	38
Subtract Memory byte from D	46	F7
Subtract Memory byte from d with Borrow	46	77
Subtract Immediate Memory from D with Borrow	46	FF bb
Subtract Immediate Memory from D	46	5r
SToRe D into memory	32	32
SToD via R(X) & Decrement	33	73
Store D via R(X)	33	F3
EXclusive OR Immediate	39	FB bb
	40	40

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			<del>B/0 TILL OCT 20.</del> <del>SOCK FOR THE DELAY</del>	<del>SHIPPED</del> <del>MANUAL &amp; SPEAKER</del>	
			<del>QUEST</del>		DEC 15 1971
Note: We cannot ship UPS to P.O. Boxes					
<i>B/0 SPEAKER FOR KIT 2-3 WEEKS</i>					
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1	1		1K SUP. Rom		

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