

# **SUPER ELF**

**AN  
1802 BASED  
MICRO COMPUTER  
BY  
QUEST**

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If you have any questions  
or problems with your SUPER ELF

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CONTENTS

	<u>PAGE</u>
I INTRODUCTION	
1. Manual Contents	5
2. External Connections	5
II OPERATION	
1. Hardware Assignments	6
2. Controls Description	6
3. Indicators and Displays Description	7
4. Operation without the ROM Monitor	8
5. Operation with the ROM Monitor	9
6. Using Single Step/Slow Step	10
III LOGIC DESIGN DESCRIPTION	
1. Hexidecimal Keypad	11
2. Control Circuit G R S W	13
3. Control Circuit M P I L	15
4. Display Control	17
5. ROM/RAM Select	17
6. RAM/ROM Memory	19
7. State/Mode Display	19
8. Output/Data Display	23
9. Address Buffers/Latch	23
10. Address Display	25
11. Power Supply	25
12. Memory Saver	25
13. Video Generator	29
14. I/O Port Select	29
15. Q Circuit	29
16. Clock Generator	30
IV EXPANSION BUS	
1. Capabilities	31
2. Constraints	31
V TROUBLESHOOTING	
1. CPU Mode Control	34
2. Hexidecimal Keypad	34
3. Video Display	35
4. Data/Output Display	35

5. Address Display	35
6. ROM/RAM Select	35
7. Load Mode	35
<b>APPENDIX A. PARTS LIST AND ASSEMBLY INSTRUCTIONS</b>	
1. Parts List - Basic	43
2. Parts List - Optional Low Address Display	46
3. Parts List - Optional High Address Display	47
4. Parts List - Optional Memory Saver	47
5. Parts List - Optional Accessories	48
6. Assembly Instructions - Basic	48
7. Assembly Instructions - Low Address Display	52
8. Assembly Instructions - High Address Display	52
9. Assembly Instructions - Memory Saver	52
10. Initial Checkout	53
<b>APPENDIX B. DATA SHEETS</b>	
1. CDP1802 Microprocessor	57
2. CDP1861 Video Display Controller	78
<b>FIGURES</b>	
1. Hexidecimal Keyboard	12
2. Control Circuit G R S W	14
3. Control Circuit M P I L	16
4. Display Control / ROM/RAM Select	18
5. RAM/ROM Memory	20
6. State/Mode Display	21
7. Output/Data Display	22
8. Address Buffers/Latch	24
9. Address Display	26
10. Power Supply / Memory Saver	27
11. Video Generator / I/O Port Select / Q circuit / Clock	28
12. Expansion Bus Connections	33
13. Component Layout V 1.0	36
14. Component Layout V 2.0	37
15. Board Wiring Pattern V 1.0 Front	38
16. Board Wiring Pattern V 1.0 Back	39
17. Board Wiring Pattern V 2.0 Front	40
18. Board Wiring Pattern V 2.0 Back	41
19. Power and Ground Connections	42
<b>CHANGE NOTICES</b>	89

## I. INTRODUCTION

### 1. MANUAL CONTENTS

This manual consists of 5 major sections and two appendices. These 5 sections cover a) a description of the external connections required, b) detailed descriptions of the operational features and how to use them, c) logic diagrams/schematics and descriptions of how the logic works, d) the expansion buses and how to use them, and e) hints on troubleshooting in case of difficulty. Appendix A contains parts lists and assembly instructions for the basic SUPER ELF and available options. Appendix B contains complete data sheets on both the 1802 CPU and the 1861 video graphics generator.

### 2. EXTERNAL CONNECTIONS

All external connections are located in the upper left hand corner of the printed circuit board. These connections are summarized here and discussed in more detail in both Section III Logic Design and Appendix A Parts List and Assembly Instructions. Starting at the upper lefthand corner and going to the right, the BAT pair of connections are used for the 2.4V standby Ni-Cad battery included in the memory saver option. Next are the SW1 connections used to connect the battery to the Rams (also used in the memory saver option). Next are the SW2 connections used to disable the Rams (also used in the memory saver option). Next are the AC connections which are used to supply power to the board from the supplied plug-in transformer. Going back to the upper lefthand corner and going down the left edge is the SPKR connections. This is the amplified output of the Q line. Normally a speaker is connected here for audio effects. However, these connections can also be used as a serial output port or a relay driver. Next are the VID connections which are an amplified composite (sync and video) video signal of approximately 2 volts peak to peak. This output may drive a video monitor directly or it may be used to drive an RF modulator to allow connections to any TV set's antenna terminals. Some RF modulators available for this use work much better than others. One that has been tested and approved is the VAMP INC. Model RFVM-1 which is available through QUEST.

## II. OPERATION

### 1. HARDWARE ASSIGNMENTS

The SUPER ELF has been designed using the following hardware assignments.

- A. Video Display ON Op Code 61.
- B. Video Display OFF Op Code 62.
- C. HEX Keyboard Input Op Code 6C.
- D. HEX Display Output Op Code 64.
- E. Video Display Status Line EF1.
- F. Input Switch Status Line EF4.

### 2. CONTROLS DESCRIPTION

The following is a description of the 24 key keyboard controls.

R RESET - Puts the CPU in the RESET mode. These additional functions are reset if they were set.

1. Single Step
2. Memory Protect
3. ROM Select

L LOAD - Puts the CPU in the LOAD mode from the RESET mode.

I INPUT - Inputs data from the HEX keypad to the data bus in the LOAD mode. In the RUN mode the EF4 Status Line is LOW while the key is depressed.

P MEMORY PROTECT - Prevents writing into memory. Useful in the LOAD mode to verify the load. Cannot be used in the RUN mode with the basic unexpanded board.

M MONITOR - Selects the on-board monitor. Replaces the first 20 HEX locations in memory with the monitor ROM. Location 20 HEX is used by the monitor, so user programs must not start before location 21 HEX when using the monitor.

S SINGLE STEP - Allows single stepping through the program one machine cycle at a time. The stopping point is the negative edge of the TPA pulse of each machine cycle. This function is used with the RUN switch. When in the SINGLE STEP mode, the DATA/OUTPUT displays display the DATA bus.

- G RUN or GO puts the CPU in the RUN mode from either the WAIT or RESET modes. If single step has been selected, only one machine cycle will be executed at a time with each momentary key depression. Holding the RUN button down will result in slowly stepping through the program one machine cycle at a time.
- W WAIT puts the CPU in the WAIT state if previously in the RUN state. Puts the CPU in the LOAD state from the RESET state. Resets memory protect.
- O through F - HEX keypad stores the last TWO key depressions for input to the 8 bit data bus. The last key depressed is the least significant 4 bits of the 8 bit data word.

### 3. INDICATORS AND DISPLAYS DESCRIPTION

The SUPER ELF has nine LEDS and two HEX displays (4 additional HEX displays are optional).

#### A. The LEDS show:

ID	FUNCTION
Q	Status of Q line
L	CPU in LOAD mode
R	CPU in RESET mode
G	CPU in RUN mode
W	CPU in WAIT mode
0	CPU in state 0
1	CPU in state 1
2	CPU in state 2
3	CPU in state 3

NOTE: LED logic is active high.

B. The two HEX displays are normally an output port. However, in the SINGLE STEP mode, the displays show the contents of the data bus.

C. The 4 optional HEX displays show the contents of the address bus.

#### 4. OPERATION WITHOUT THE ROM MONITOR

A. Loading programs is done in the LOAD mode. If you have purchased the address display option, the address just loaded will be displayed along with the address contents. All loading must start at location 00HEX.

(1.) To load a program.

- a. Push RESET R key.
- b. Push LOAD L key.
- c. Push the 2 HEX keypad keys corresponding to the contents of address 00HEX.
- d. Push the INPUT I switch.
- e. The contents of address 00HEX will be displayed by the data displays.
- f. Push the 2 HEX keypad keys corresponding to the contents of the next address.
- g. Push the INPUT I switch.
- h. The contents of that address will be displayed.
- i. Repeat steps f and g until the entire program is loaded.

(2) To make corrections.

- a. Push RESET R key.
- b. Push LOAD L key.
- c. Push Memory Protect P key.
- d. Push the INPUT I key until the preceding location is reached.
- e. Load the HEX keypad with the corrected data word.
- f. Push the WAIT W key to enable memory writing.
- g. Push the INPUT I key to load the correction data word.

(3) To run programs.

- a. Push the RESET R key.
- b. Push the RUN G key. The program will start executing at address 00HEX.

## 5. OPERATION WITH THE ROM MONITOR

The SUPER ELF monitor allows us to do three things.

A. Loading a program starting at any location.

B. Examine any location in memory (including the monitor itself).

C. Starting a program at any location.

NOTE: This monitor only works with PAGE ZERO (the first 256 words of memory).

A. To use the monitor to load a program.

(1) Push RESET R key.

*MONITOR CONTROL IN* → (2) Push HEX keys 0 and 2 in that order.

*SKIP MEMORY ADDRESS* → (3) Push the MONITOR M select key.

00 → (4) Push the RUN G key and the data display will indicate 02.

02 → (5) Push the two HEX keypad keys corresponding to the starting address.

(6) Push the INPUT I key and the Q light will come on indicating that memory writing is enabled.

(7) Push the two HEX keypad keys corresponding to the data going into the memory.

(8) Push the INPUT I key and the data displays will display the memory data just entered.

(9) Repeat steps 7 and 8 for the remainder of the program.

(10) Push the RESET R key when completed.

B. To use the monitor to read out memory contents.

(1) Push the RESET R key.

*MONITOR CONTROL OUT* → (2) Push HEX keypad keys 0 and 1 in that order.

01 → (3) Push the Monitor M select key.

01 → (4) Push the RUN G key and the data display will indicate 01.

(5) Push the two HEX keypad keys corresponding to the starting address.

(6) Push the INPUT I key.

(7) Push the INPUT I key again and the data display will indicate the contents of the specified memory location.

(8) Continue to push the INPUT I key to step through the memory contents one at a time.

(9) Push the RESET R key when completed.

NOTE: The contents of the monitor may be read out by using memory location 00 in step 5.

C. To use the monitor to start execution of a program at any location.

- (1) Push the RESET R key.
- 00 (2) Push the HEX keypad key 0 twice.
- (3) Push the Monitor M select key.
- (4) Push the RUN G key and the data display will indicate 00.
- (5) Push the two HEX keypad keys corresponding to the starting address.
- (6) Push the INPUT I key and the program will start executing.

## 6. USING SINGLE STEP/SLOW STEP

The SUPER ELF has the ability to step through programs one machine cycle at a time. Execution is halted at the negative edge of the TPA signal in each machine cycle. At this point, the CPU is in the process of executing the current instruction cycle. The instruction set timing diagrams in APPENDIX B should be consulted to determine the hardware state corresponding to the instruction being executed.

The single step/slow step mode may be entered from the RESET state or the WAIT state by pushing the Single Step S key. Program execution may then be started or resumed by pushing the RUN G key. A single push of the RUN G key will advance the program one machine cycle. Holding the RUN G key down will advance the program at a rate of approximately 1 to 2 machine cycles per second. Releasing the RUN G key will stop execution. Pushing the WAIT W key disables the single step mode and then pushing the RUN G key resumes normal speed operation.

### III LOGIC DESIGN DESCRIPTION

#### 1. HEXIDEcimal KEYBOARD (Figure 1)

The 16 push buttons of the HEX keypad are encoded into one HEX character using a CMOS 20 key encoder, 74C923. The keys are arranged in a 4x4 matrix. The encoder uses scanning to determine which key is depressed. The scanning frequency is determined by C7 and is nominally 600 cps. The switch debounce is internally eliminated, with the debounce period set by C9 to nominally 25ms. When a key is depressed, the data available (DA) line goes high after the debounce period. If a second key is depressed before the first key is released, releasing the first key will force the DA line low and then, after the debounce period, DA will go high for the second key. This is called two key roll-over. The DA line will stay high as long as the key is depressed. The output data word is retained until the NEXT key depression causes an another DA pulse. The data word does not change from old to new until AFTER the leading edge of the DA pulse. This feature allows storing the old data word using the DA pulse to latch a special zero input delay latch. This latch, a 74C175, uses the next DA pulse to store the previous data word. This approach allows the generation of a 8 bit data word using the last two HEX keys depressed. The last key depressed is the least significant HEX character of the 2 HEX character word. To the user, sequential HEX key depressions are shifted to the left with the last two retained as the input word. The resulting 8 bit word is gated on to the bi-directional data bus by special CMOS devices called bilateral switches. Two 4016 I/C's are used, each containing 4 switches. Each switch behaves as a very high resistance when off and as a 300 ohm resistor when on. The ON/OFF control is isolated from the "contacts". The switches are wired as one 8 pole single throw switch. The keyboard input signal, KBIN, gates the data word onto the data bus. This results from the execution of the I/O port input command 6C or pushing the input key during the load mode.

Hexidecimal Keyboard

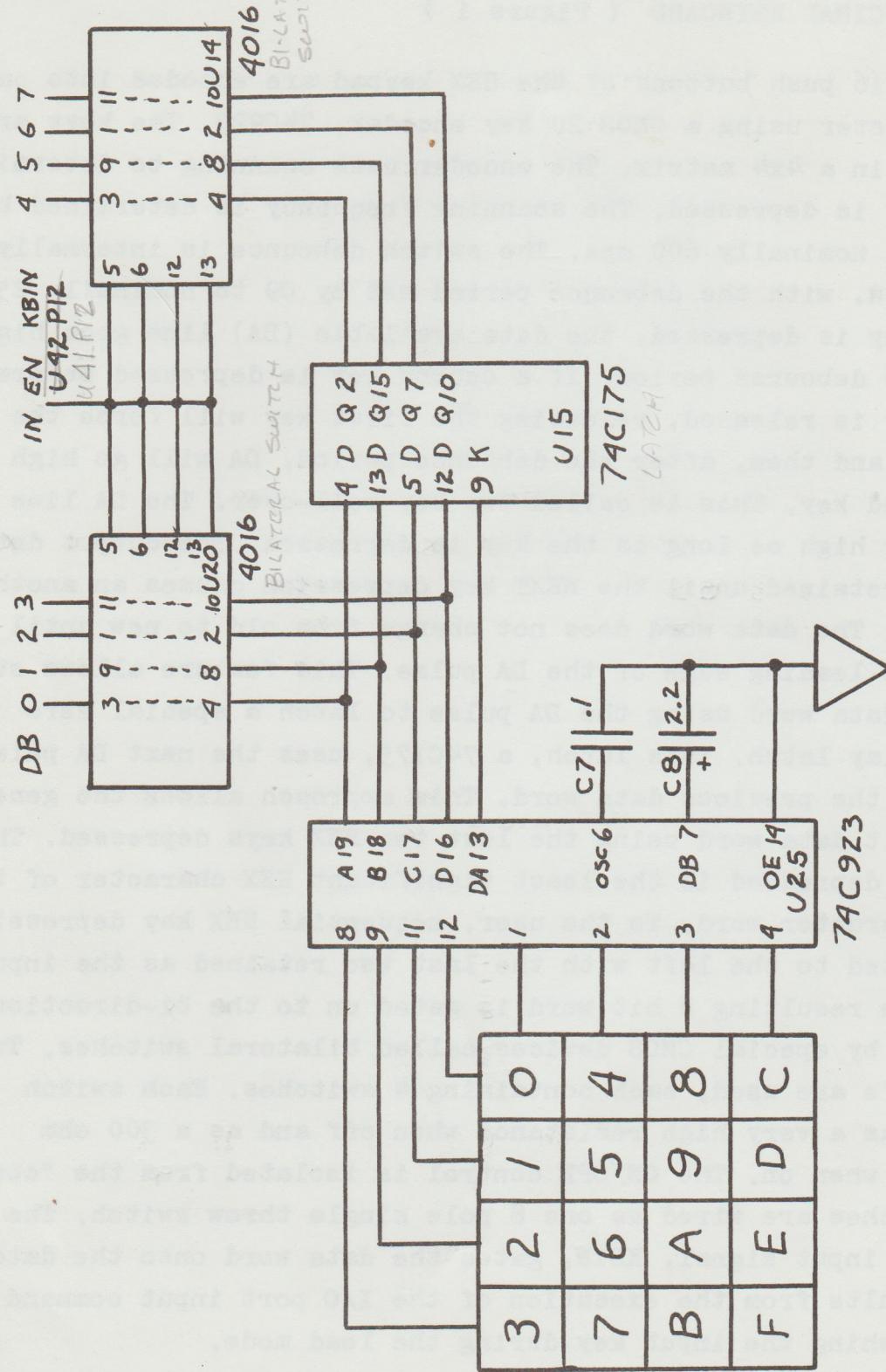


Figure 1

## 2. CONTROL CIRCUITS G R S W (Figure 2)

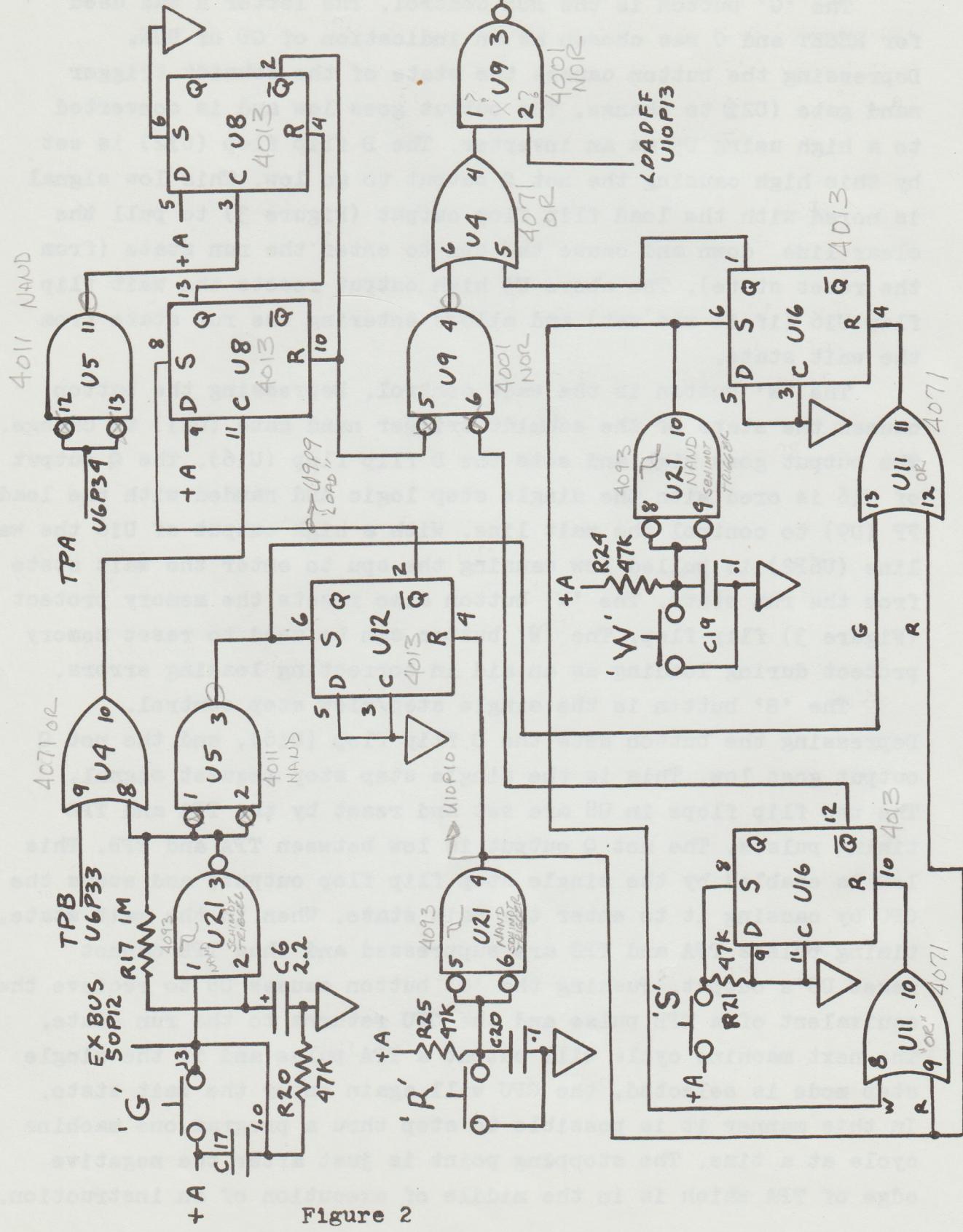
The 'G' button is the RUN control. The letter R was used for RESET and G was chosen as an indication of GO or RUN. Depressing the button causes the state of the schmidt trigger nand gate (U21) to change. The output goes low and is converted to a high using U5 as an inverter. The D flip flop (U12) is set by this high causing the not Q output to go low. This low signal is nored with the load flip flop output (Figure 3) to pull the clear line down and cause the cpu to enter the run state (from the reset state). The above U5 high output resets the wait flip flop U16 (if it was set) and allows entering the run state from the wait state.

The 'W' button is the wait control. Depressing the button causes the state of the schmidt trigger nand gate (U21) to change. The output goes high and sets the D flip flop (U16). The Q output of U16 is ored with the single step logic and nanded with the load FF (U9) to control the wait line. With a high output of U16 the wait line (U6P2) is pulled low causing the cpu to enter the wait stste from the run state. The 'W' button also resets the memory protect (Figure 3) flip flop. The 'W' button can be used to reset memory protect during loading as an aid in correcting loading errors.

The 'S' button is the single step/slow step control. Depressing the button sets the D flip flop (U16), and the not Q output goes low. This is the single step stop request signal. The two flip flops in U8 are set and reset by the TPA and TPB timing pulses. The not Q output is low between TPA and TPB. This low is enabled by the single step flip flop output, and stops the CPU by causing it to enter the wait state. When in the wait state, timing pulses TPA and TPB are suppressed and thus TPB cannot reset U8's output. Pushing the 'G' button causes U8 to recieve the equivalent of a TPB pulse and the CPU returns to the run state. The next machine cycle will output a TPA pulse and if the single step mode is selected, the CPU will again enter the wait stste. In this manner it is possible to step thru a program one machine cycle at a time. The stopping point is just after the negative edge of TPA which is in the middle of execution of an instruction.

## Control Circuit

G R S W



**Figure 2**

The timing diagrams in the appendix should be consulted to determine specifically where the instruction execution has stopped. Note that there are at least two and sometimes three machine cycles per instruction. The 'G' button schmidt trigger has a gated oscillator built into it which provides the slow step feature. When the button is pushed and held, the oscillator is enabled and starts outputting pulses (equivalent to TPB) at approximately Two per second. The same feature could be accomplished simply by repetitively pushing the button. The initial delay for the first pulse is caused by the time it takes to charge C6 up to the schmidt trigger operating point.

The 'R' button is the reset button. Depressing the button causes the state of the schmidt trigger to change putting a high on the reset line. All other functions are reset by this control.

### 3. CONTROL CIRCUITS M P I L (Figure 3)

The 'M' button is the ROM monitor select control. Depressing the button causes the D flip flop (U12) to be set. The not Q output goes low and this signal is used to select the ROM when the first 32 locations are addressed. (see figure 4)

The 'P' button is the memory protect control. Depressing the button causes the D flip flop (U10) to be set. The Q output is ored with the CPU MWR signal. When in the Protect mode, the MWR signal is blocked and memory write is inhibited.

The 'L' button is the load mode select control. Depressing the button causes the D flip flop (U10) to be set. The Q output is nored with the clear and wait CPU controls forcing them low and putting the CPU in the wait state.

The 'I' button is the input control. Depressing the button causes the state of the schmidt trigger (U21) to change to low. This pulls the EF4 CPU sense line low. This signal can be used by a program to detect that input data is available. Also the D flip flop (U7) is clocked causing the DMAIN signal to go low. this signal is used by the CPU in the 'built in' load mode to load data into memory.

## Control Circuit

M P I L

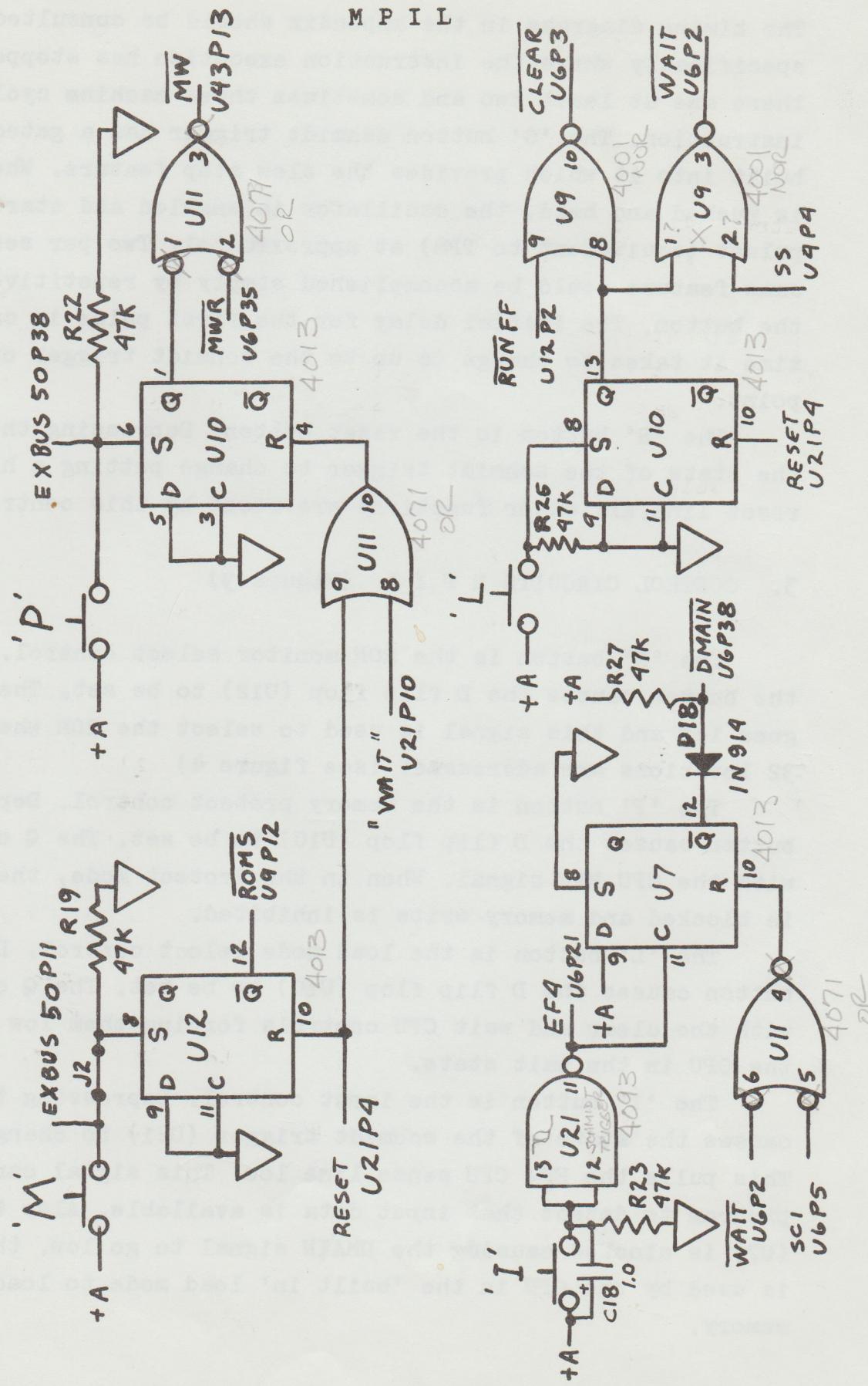


Figure 3

#### 4. DISPLAY CONTROL (Figure 4)

This circuit logically decides when to enable the input latches of the display drivers. TPB and MRD along with either load or N2 are anded together to detect the execution of an output instruction and enable the displays. One additional logic element has been added to switch the displays from an output display to a data bus display. When the single step mode is selected this signal is gated with the display select signal forcing the displays onto the data bus all the time.

The same figure also shows the logic for enabling the input data word. In this case either LOAD or N2 and MRD cause the input to be selected.

#### 5. ROM/RAM SELECT (Figure 4)

The ROM is selected only during memory read cycles of the first 32 locations in memory when in the ROM mode. Address lines A5, A6, and A7 are all zero for the first 32 locations. These signals are anded with the ROM select signal and the result is anded with MRD to enable the ROM during memory reads of the first 32 locations. If the ROM is not selected than the RAM must be selected. This signal is used with either MW or MRD to enable the RAM for a memory read or write.

The dotted lines show the V1.0 wiring. In this version, the rom is selected during either a write or read operation. Therefore any attempt to write into the first 32 locations will cause a momentary data bus conflict. This is not harmful in this application but the design was changed to eliminate this conflict in the V2.0 boards. The inverter used is spare on the V1.0 boards and so this change could be made if desired by trace cutting and jumpers.

SINGLE STEP  
DISPLAY INDICATE  
DATA BUS  
ONLY

MA  
of 32  
for ROM

## ROM/RAM Select

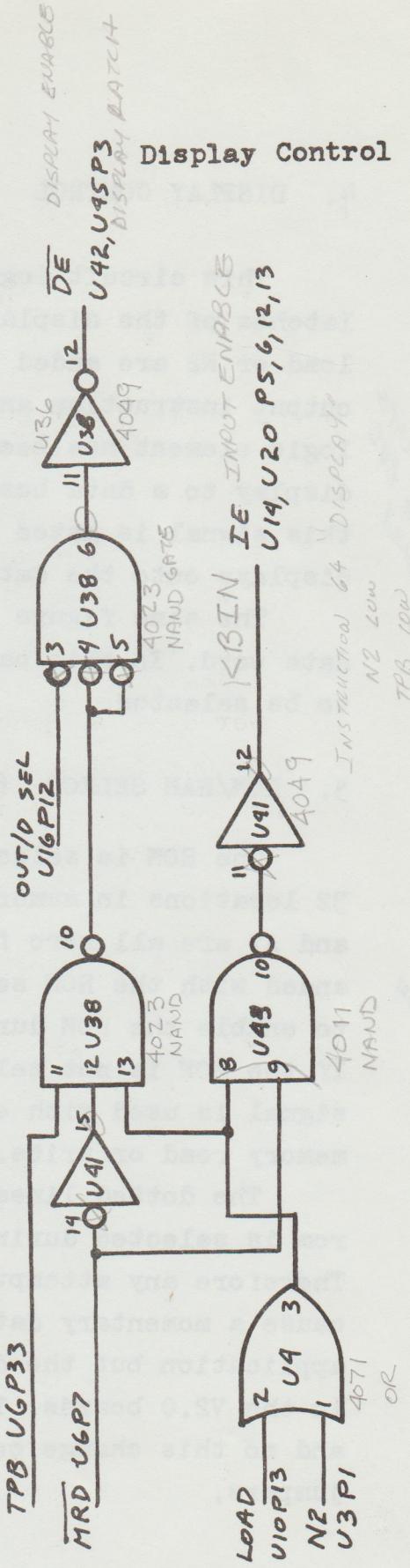
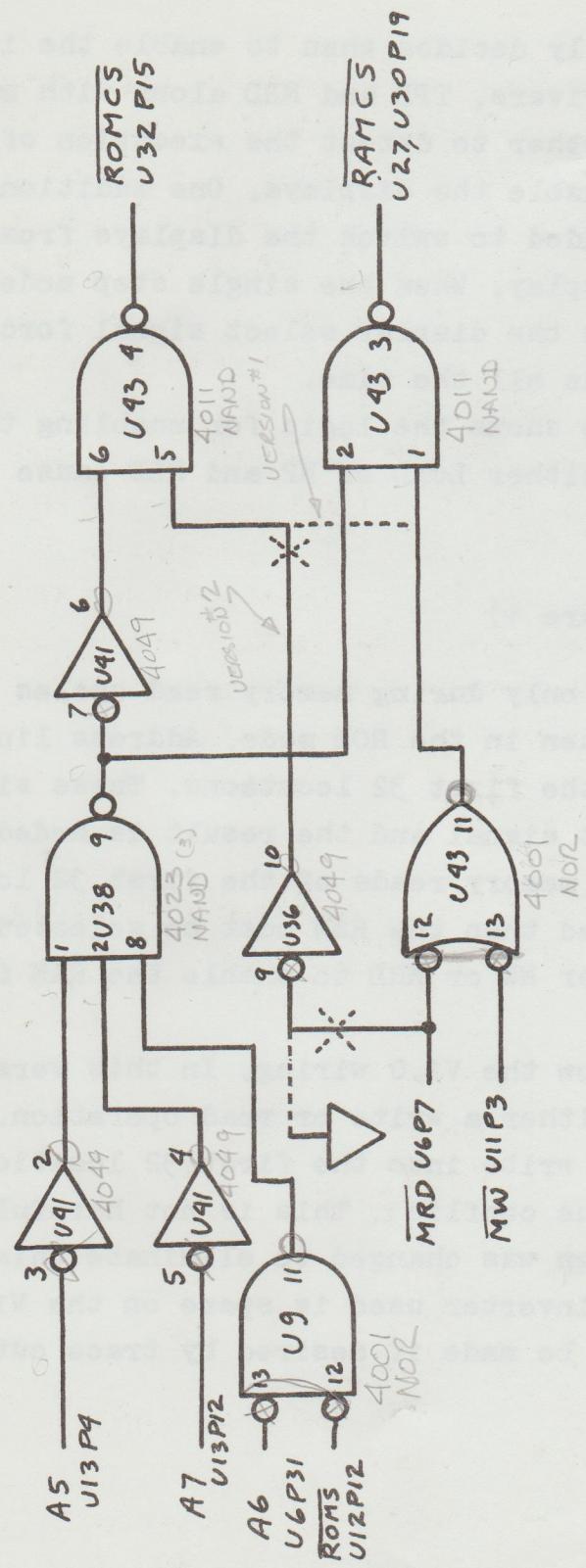


Figure 4

## 6. RAM/ROM MEMORY (Figure 5)

The RAM consists of two 2101 MOS memorys organized as 256 words of 4 bits. Their address lines are in parallel to result in a memory organized as 256x8. The ROM is a TTL fusible link PROM organized as 32x8. Its output data lines are Tri-State so that they are not connected to the data bus unless the ROM is selected (Figure 4). The RAM control is more complex. In addition to the RAM select signal (Figure 4) The output is enabled by MRD and read / write control is by MW. There is an additional RAM select signal which is active high and normally held up by R18. In the memory saver option this line is lowered to disable the RAM prior to power down to prevent random write pulses during up or down.

Note: that the address and data lines are not connected in accordance with the manufacturer's convention for A0,A1---A7, D0----D7. This is done for convenience of circuit board layout and causes no problem in operation.

## 7. STATE/MODE DISPLAY (Figure 6)

The STATE and MODE displays are similar and decode the two input lines into the corresponding LED driver.

<u>MODE</u>	<u>CLEAR</u>	<u>WAIT</u>
LOAD	LOW	LOW
RESET	LOW	HIGH
RUN	HIGH	HIGH
WAIT	HIGH	LOW

<u>STATE</u>	<u>SC1</u>	<u>SCO</u>
S0 (Fetch)	LOW	LOW
S1 (Execute)	LOW	HIGH
S2 (DMA)	HIGH	LOW
S3 (INT)	HIGH	HIGH

The two input lines are inverted and the normal and inverted signals are input to the and gates, only one and gate is true at a time. This output is inverted in the corresponding 4049 driver and provides a current limited sink of approximately

## RAM/ROM Memory

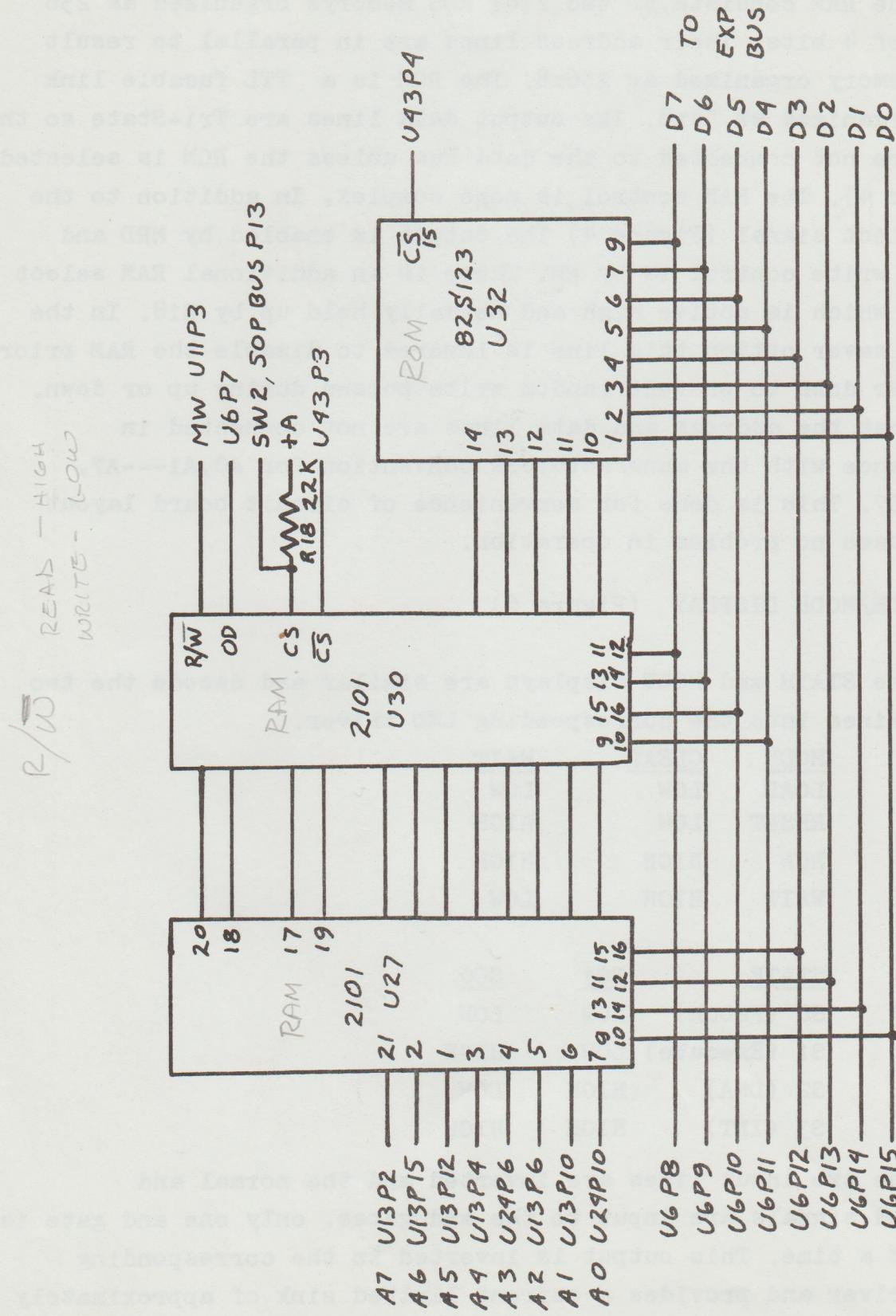


Figure 5

## State/Mode Display

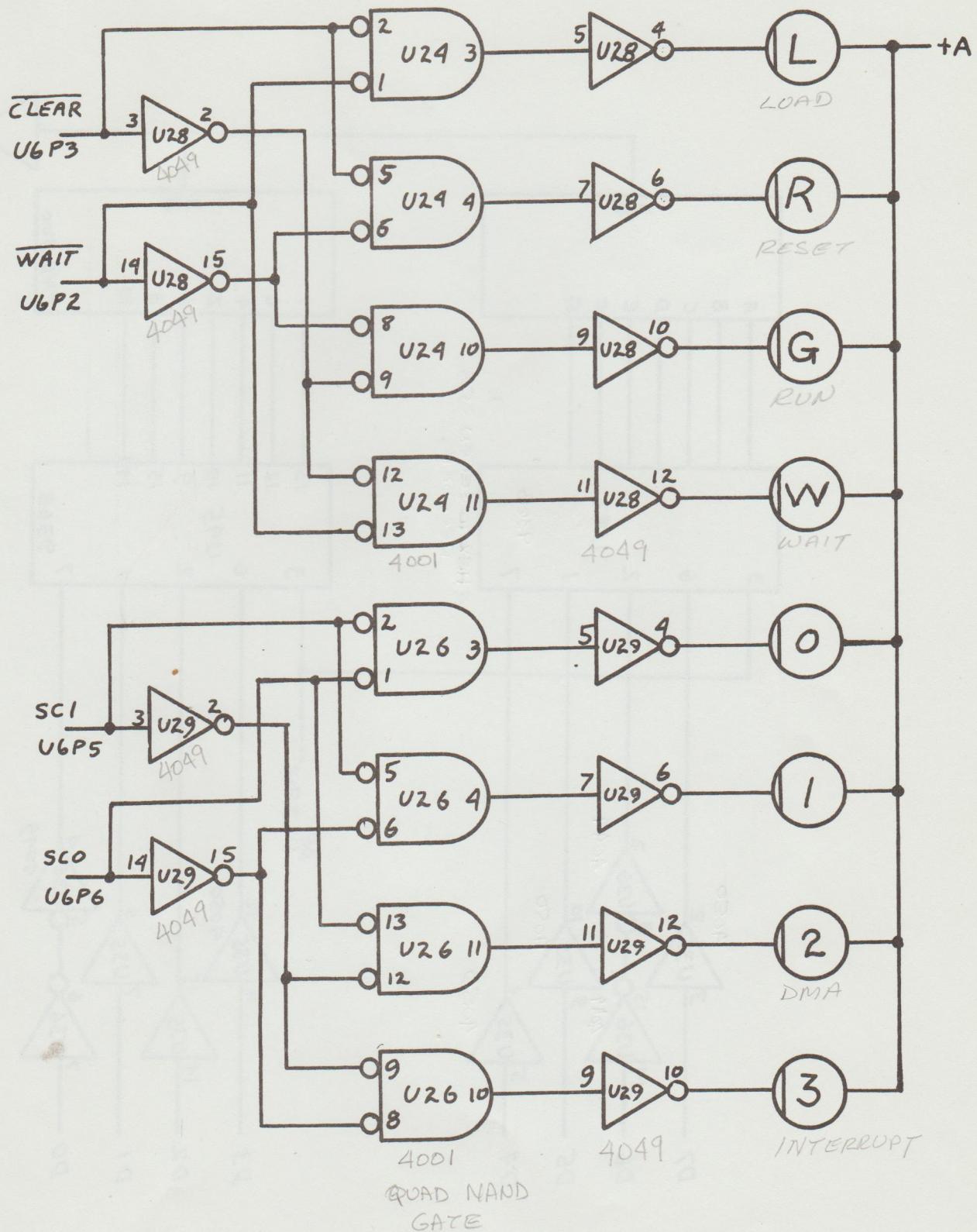


Figure 6

## Output/Data Display

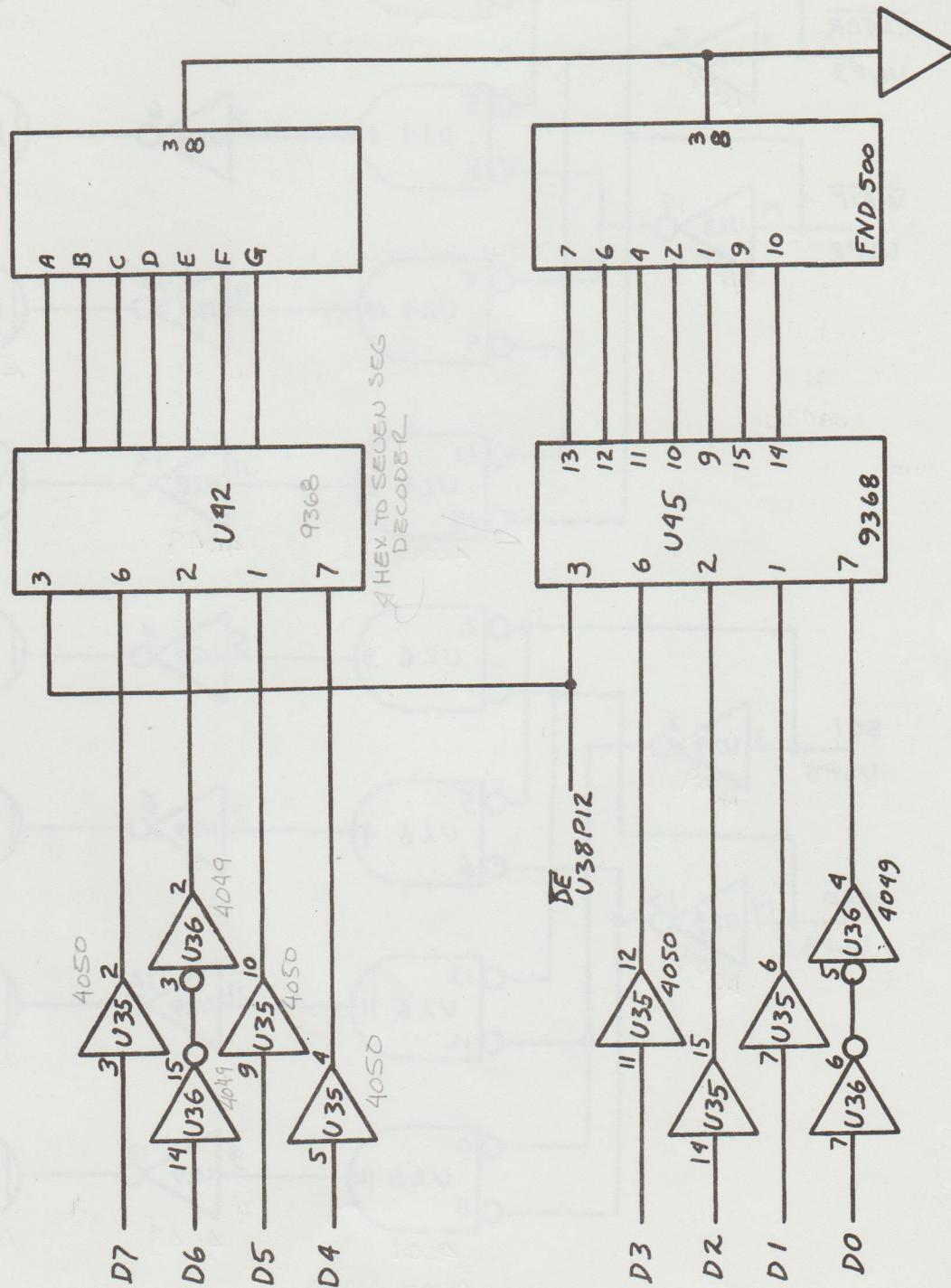


Figure 7

15ma to light the LED. the use of a 4049 eliminates the need for a series resistor since it is internally current limited to a safe value (with a 5v supply).

Only one STATE or MODE led can be on at a time. However due to the persistance of vision, more than one STATE led may appear to be on when the CPU is in the run mode.

#### 8. OUTPUT/DATA DISPLAY (Figure 7)

The displays are seven segment leds which use a combination of upper case and lower case letters to obtain a hex readout. the display drivers are combination decoders, latches, and current limited drivers. Except for loading considerations, they could be connected directly to the data bus. Buffers are used to reduce the loading to a CMOS load. When the display drivers are enabled they latch the content of the data bus and display the stored value. (Figure 4) External current limiting resistors could have been used to reduce the power disipation but this would have reduced the brightness of the displays. Although the display drivers run hot they are working normally as they were designed.

#### 9. ADDRESS BUFFERS/LATCH (Figure 8)

The address lines are buffered for both the display option and the expansion bus. The high address if any is present on the address bus during the TPA timing pulse. This allows latching the high address with the TPA signal. The high address lines are also buffered.

## Address Buffers/Latch

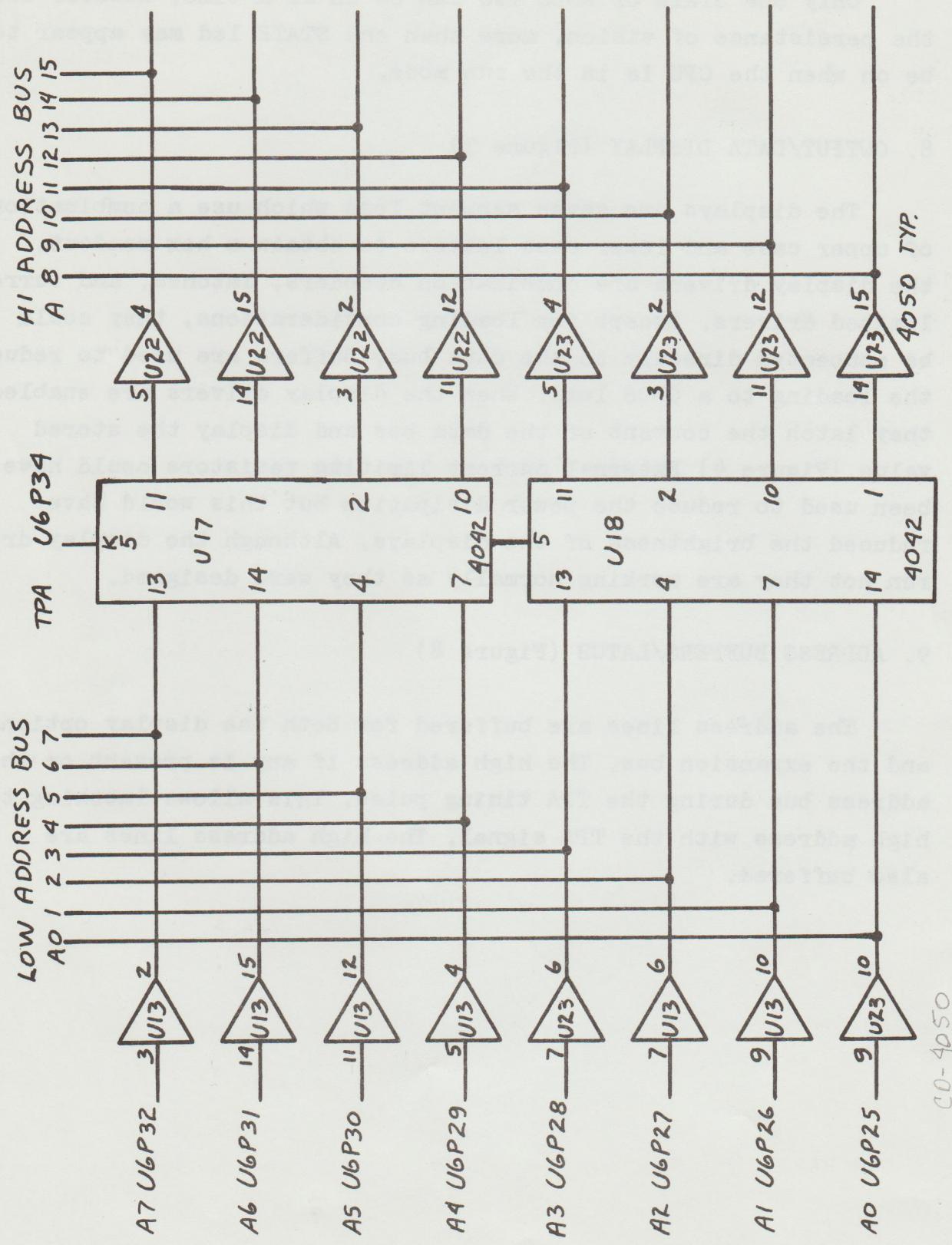


Figure 8

#### 10. ADDRESS DISPLAY (Figure 9)

The address bus contents may be displayed using the optional displays. The displays and drivers are the same as the output/data displays. In this case the displays are always enabled so that they show what is on the address bus at any time. Thus, during program execution in the RUN mode, they usually appear somewhat dim and look like they are displaying eights. In the slow step mode they provide a useful debug tool. During the manual load mode they provide a read out of the location and content just loaded. Note that they are not usable when loading using the monitor. Unless you go to the single step mode and follow the program execution.

#### 11. POWER SUPPLY (Figure 10)

The power supply for the basic kit consists of a wall plug transformer with a 10 volt output which is rectified by the bridge rectifier (D2,D3,D6,D7) and filtered by C1. The resulting voltage is higher than necessary and is dropped by the series diode string (D10,D12,D14,D16) and input to the regulator (this reduces the regulator power dissipation). C15 is used to provide stable regulator operation. The output bus is called +A and the nominal current is 500ma. Noise on the bus is reduced by the bus/ground layout around the edge of the board and by bypass capacitors C3,C5,C9, and C10.

The address displays have their own power supply which is identical in design to the main supply. The load on this supply with all four address displays is almost the same as the basic supply. Almost all the power goes to the LEDs and displays.

#### 12. MEMORY SAVER (Figure 10)

The memory saver consists of a third supply which supplies only the RAM's (by cutting J1). Ni-Cad batteries are used to provide standby power. They are automatically charged when power

## Address Display

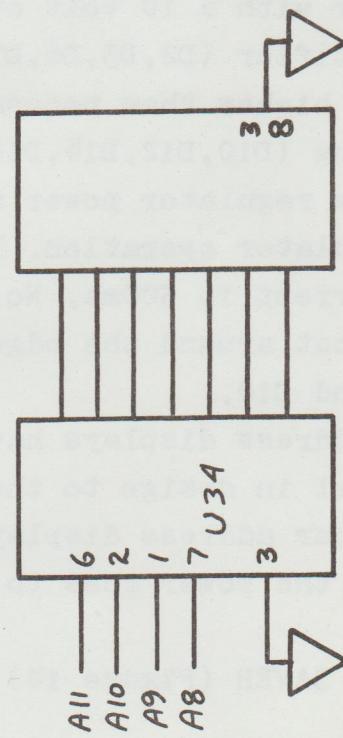
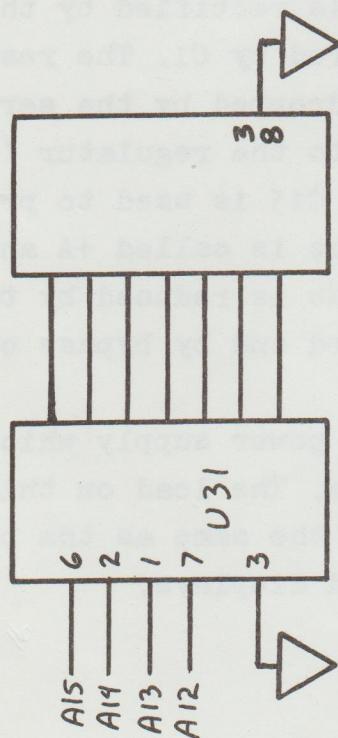
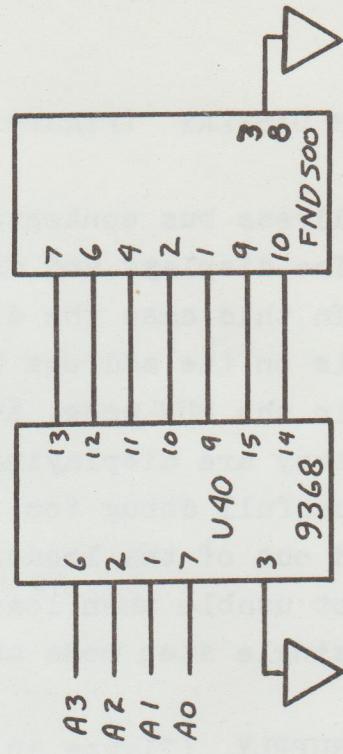
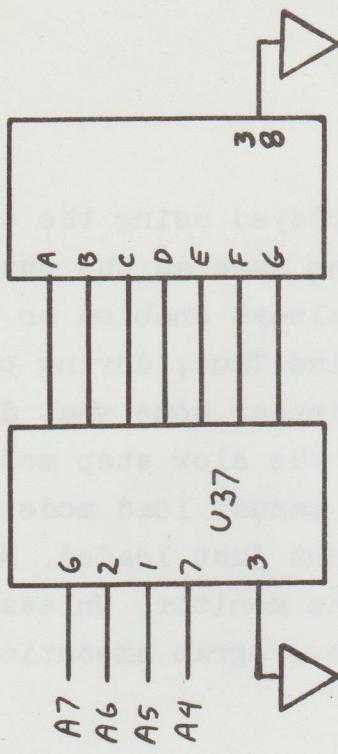


Figure 9

**Power Supply/Memory Saver**

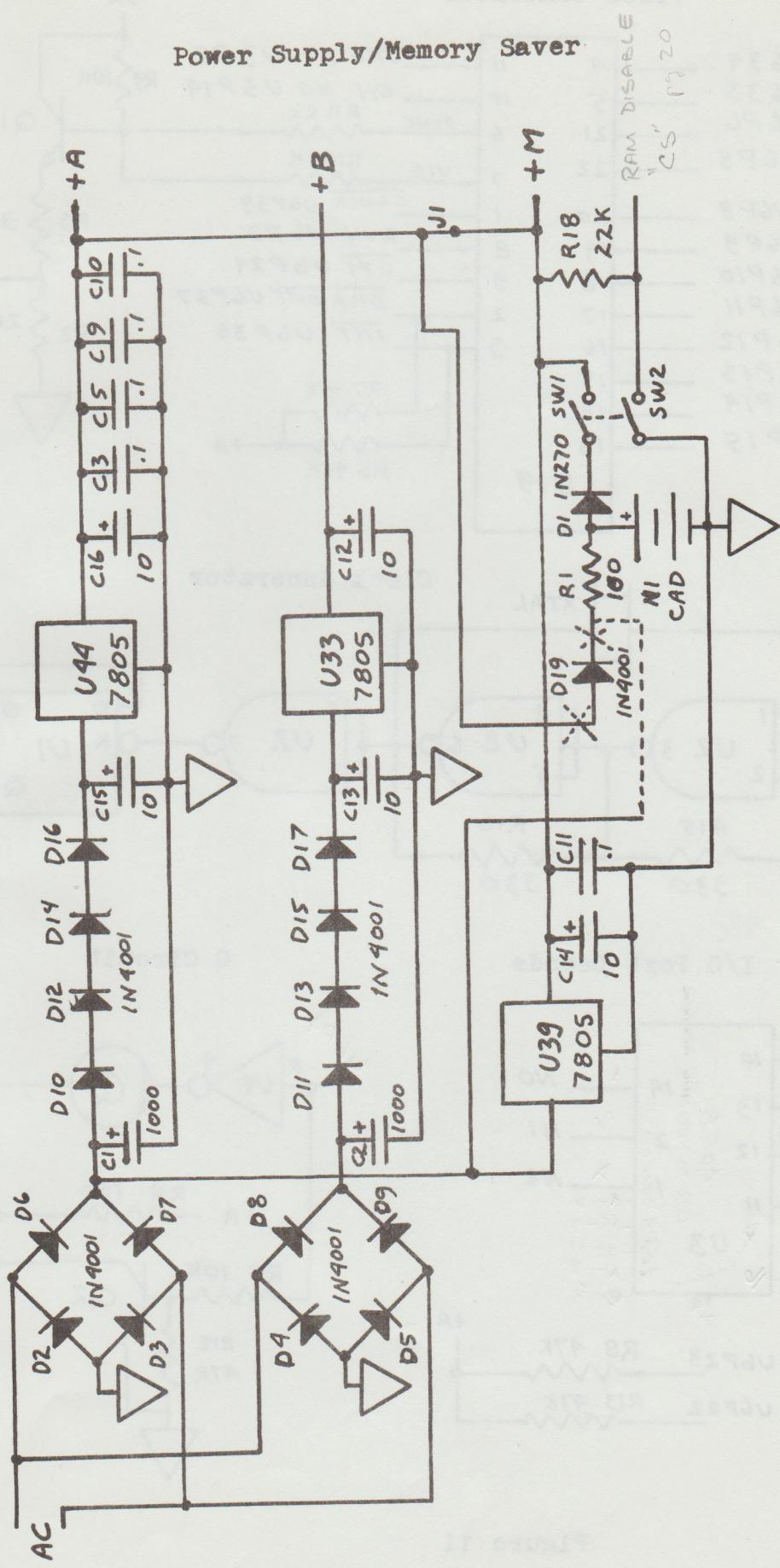


Figure 10

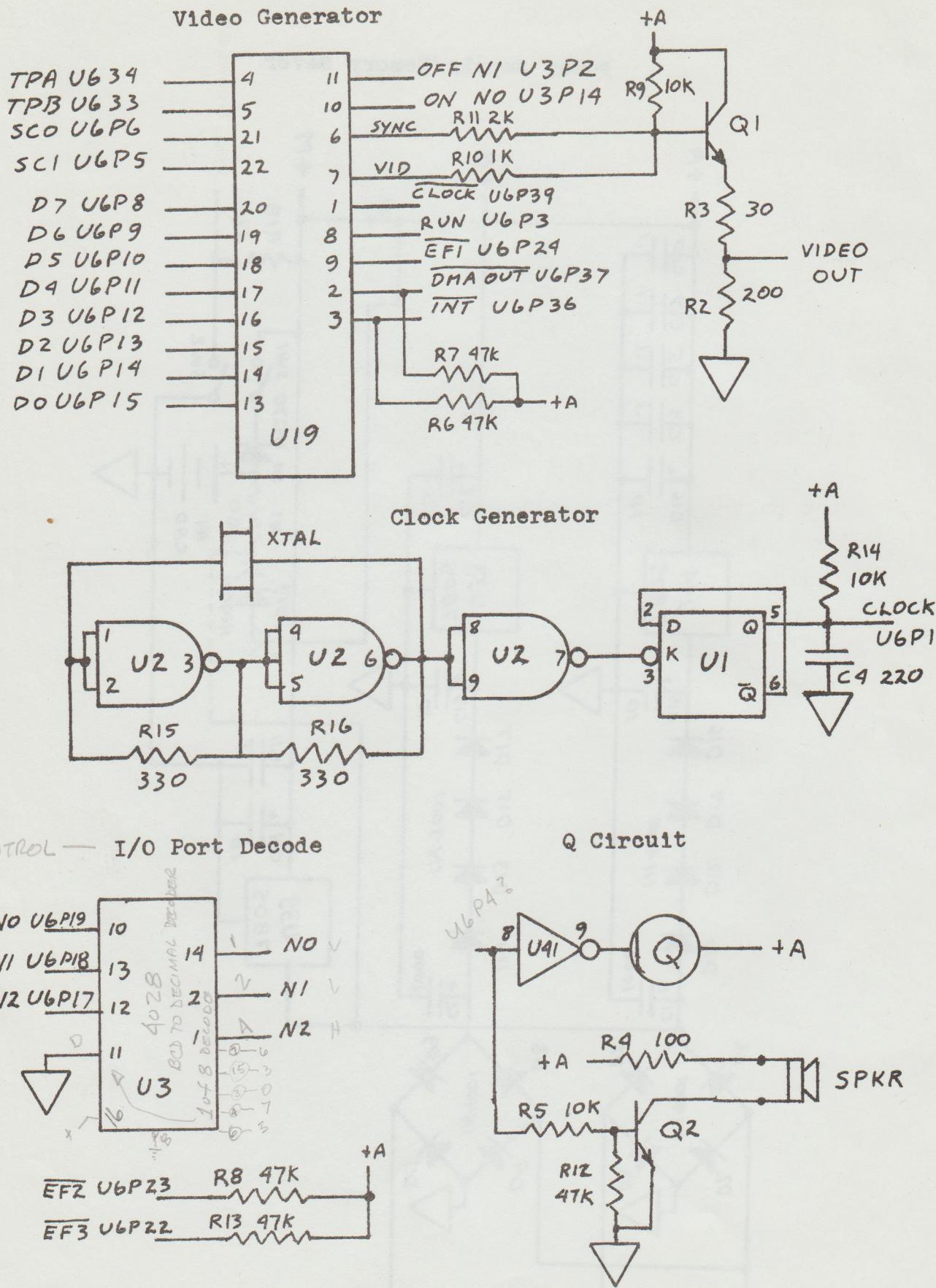


Figure 11

is on. The switch grounds the RAM select to prevent power transients from causing random memory writing during power on/off. The dotted lines show the V1.0 design. The V2.0 change revised the source of the charge current and the charging current was increased, D19 isolates the batteries from the power bus when it is off.

#### 13. VIDEO GENERATOR (Figure 11)

The video generator consists of an 1861 Video Display Controller and a video amplifier. The operation of the 1861 is covered in the appendix data sheets. The video amplifier combines the sync pulses with the video signal and provides a low impedance drive with sufficient power to all tested video monitors and RF modulators.

#### 14. I/O PORT SELECTION (Figure 11)

The I/O port decoder is a BCD to Decimal decoder used as a 3 line to one of eight line decoder. Use of the I/O lines directly from the CPU is Permitted but limits the design to a maximum of 3 input and 3 output ports. By Decoding the lines the number of input and output ports is increased to seven of each.

#### 15. Q CIRCUIT (Figure 11)

The Q LED is driven by a current limited inverter like the STATE/MODE LED's. An audio amplifier and speaker is also connected to the Q line. The Speaker can be replaced with a relay by shorting out R4.

## 16. CLOCK GENERATOR (Figure 11)

The Clock Generator is a TTL and gate used as an inverting amplifier. R15 and R16 bias the TTL logic into the linear region. The third gate is used as a buffer to the divide by 2 flip flop. R14 is a pullup for TTL to CMOS logic shifting and C4 acts as a low pass filter to suppress overshoot. CMOS logic is too slow with a 5v supply to be used at 3.5 MC.

## IV EXPANSION BUS

### 1. CAPABILITIES

The SUPER ELF has two types of expansion buses.

The first is a standard 44-pin connector. This connector and matching plug-in printed circuit cards are readily available locally or may be purchased from QUEST. This 44-pin bus provides all the signals normally required for expanded memory (including all 16 bits of address if address options are incorporated), input/output ports, and other common applications.

The second expansion bus is a 50-pin bus designed to interface with 50-pin flat cable connectors. This bus is specifically designed to interface with the SUPER ELF expansion card containing a 1K super monitor, up to 4K of ram, a cassette interface, and other features. Four additional functions are available on this bus which are used to facilitate the use of the expansion board. For example: the M button becomes a RUN-WITH-MONITOR button. These additional functions require minor (already provided for) modifications to the basic SUPER ELF printed circuit board. Detailed instructions are provided with the expansion board.

### 2. CONSTRAINTS

When using the 44-pin expansion bus, care must be taken to insure that the power and signal interface requirements are met.

Two unregulated power buses are supplied. One (No. 1) is part of the basic SUPER ELF; the other (No. 2) is part of the low address display option. Expansion bus current drain on No. 1 should be limited to less than 300 ma. Current drain on No. 2 should be limited to less than 200 ma. when both high and low address options are installed. In addition, additional filtering may be required on the expansion card. This depends upon

the amount of current being drawn. 500 MFD to 1000 MFD on the input to the regulator is sufficient for the maximum allowable current. If more power is required, or other voltages, an auxiliary power supply is highly recommended.

The signal out lines can drive at least one Low Power TTL or a number of CMOS loads. The address lines are buffered and can drive one Standard TTL load. The input lines may be driven by TTL logic if pull up resistors are used (22K OHMS to 5V). CMOS drivers do not require pull up resistors.

Expansion bus signals which are also used by the main board must be diode isolated ON THE expanded card. For example: DMAIN.

Proper bypassing of power leads and avoidance of long expansion bus leads is necessary to avoid problems.

<u>CONNECTOR</u>	<u>FUNCTION</u>	<u>CONNECTOR</u>	<u>FUNCTION</u>		
<u>50 Pin</u>	<u>44 Pin</u>	<u>50 Pin</u>	<u>44 Pin</u>		
1	1	Ground	26	A	Ground
2	2	+10v Unreg #1	27	B	+10v Unreg #2
3	3	EF3 (22)	28	C	EF2 (23)
4	4	NO (19)	29	D	N1 (18)
5	5	N2 (17)	30	E	Q (4)
6	6	SC1 (5)	31	F	SCO (6)
7	7	MRD (7)	32	H	CLOCK (39)
8	8	DMAIN (38)	33	J	DMAOUT (37)
9	9	MWR (35)	34	K	INT (36)
10	10	TPB (33)	35	L	TPA (34)
11	-	M *	36	-	N/C
12	-	G *	37	-	N/C
13	-	CS *	38	-	MP *
14	11	A15	39	M	A14
15	12	A13	40	N	A12
16	13	A11	41	P	A10
17	14	A9	42	R	A8
18	15	A7	43	S	A6
19	16	A5	44	T	A4
20	17	A3	45	U	A2
21	18	A1	46	V	A0
22	19	D7 (5) D7 (8)	47	W	D3 (12) D6 (9)
23	20	D4 (9) D5 (10)	48	X	D2 (13) D4 (11)
24	21	D5 (10) D3 (12)	49	Y	D1 (14) D2 (13)
25	22	D4 (11) D1 (14)	50	Z	D0 (15) D0 (15)

## NOTES:

1. 1802 pin numbers shown in parenthesis where directly connected.
2. \* Signifies special function for SUPER ELF expansion board.
3. N/C Means no connection.

FIGURE 12 EXPANSION BUS CONNECTIONS

## V TROUBLESHOOTING

In case of trouble, recheck all IC's to be sure that they are in the correct location, are in the correct way and there are no bent under pins. The pin usually bends under so it is hidden and appears ok until the IC is pulled. Recheck for solder bridges using a magnifying glass. Recheck polarity of diodes and capacitors and be sure the values correspond to the parts layout. Next isolate the problem using Section III as a guide. Interchanging IC's when possible can isolate a defective IC. Since most CMOS IC's can stand a shorted output continuously (with a 5 volt supply), it is difficult for a defective IC to damage others. An upside down inserted IC will be immediately shorted out. Static discharges too small to notice will burn out inputs during handling. Difficult problems need a logic probe and scope to troubleshoot. A voltmeter has limited use because readings between 1v and 4v may indicate either pulses are present or a short.

### 1. CPU MODE CONTROL

These circuits are static and can be checked with a voltmeter. Using the schematics, trace the signals thru until the problem is isolated to a valid input to an IC and a bad output. The bad output could be because the IC is bad or the next IC in line has a shorted input. Once the circuit is isolated to this point, replacing the suspect IC usually will fix the problem. It is permissible to CAREFULLY bend out the OUTPUT pin so it does not go into the socket and see if the output is now valid. This usually (but not always) isolates the problem.

### 2. HEXIDECLIMAL KEYPAD

Some of this circuit is static and by checking the output of U25 and U15 using different keys to provide logical '1' and '0' levels.

If loading the high digit in location zero in the load mode is not reliable, the 4016 may be defective. This may be verified

by depressing the reset and load buttons and then measuring the voltages on the output of U25. With F input to the keyboard, all four voltages should be above 3v.

An end to end check from key pad to display is possible by entering the load mode and disabling the RAM. The RAM is disabled by grounding the right pad for SW2, then the key pad input is displayed directly. Pressing a key should result in its being displayed.

### 3. VIDEO DISPLAY

It may be necessary to load 61 in location 00 and 69 in location 01 in step Z of the checkout. If the 3 state lights still do not flicker the 1861 is probably defective.

### 4. DATA/OUTPUT DISPLAY

The end to end check described in 2 above and parts substitution is the best approach here. The 7 segment displays cannot be damaged if they are inserted upsidedown. The ribbed edge should be up.

### 5. ADDRESS DISPLAY

In the load mode the display should follow the input switch closures. If loading is normal but the display reads wrong, try part substitution. The high address can be checked as follows. Load C0,AA,55 in locations 00,01,02. Press reset, single step and then the run button 4 times. The address display should read AA55. Any other displayed numbers should provide a clue to the problem. Again try parts substitution.

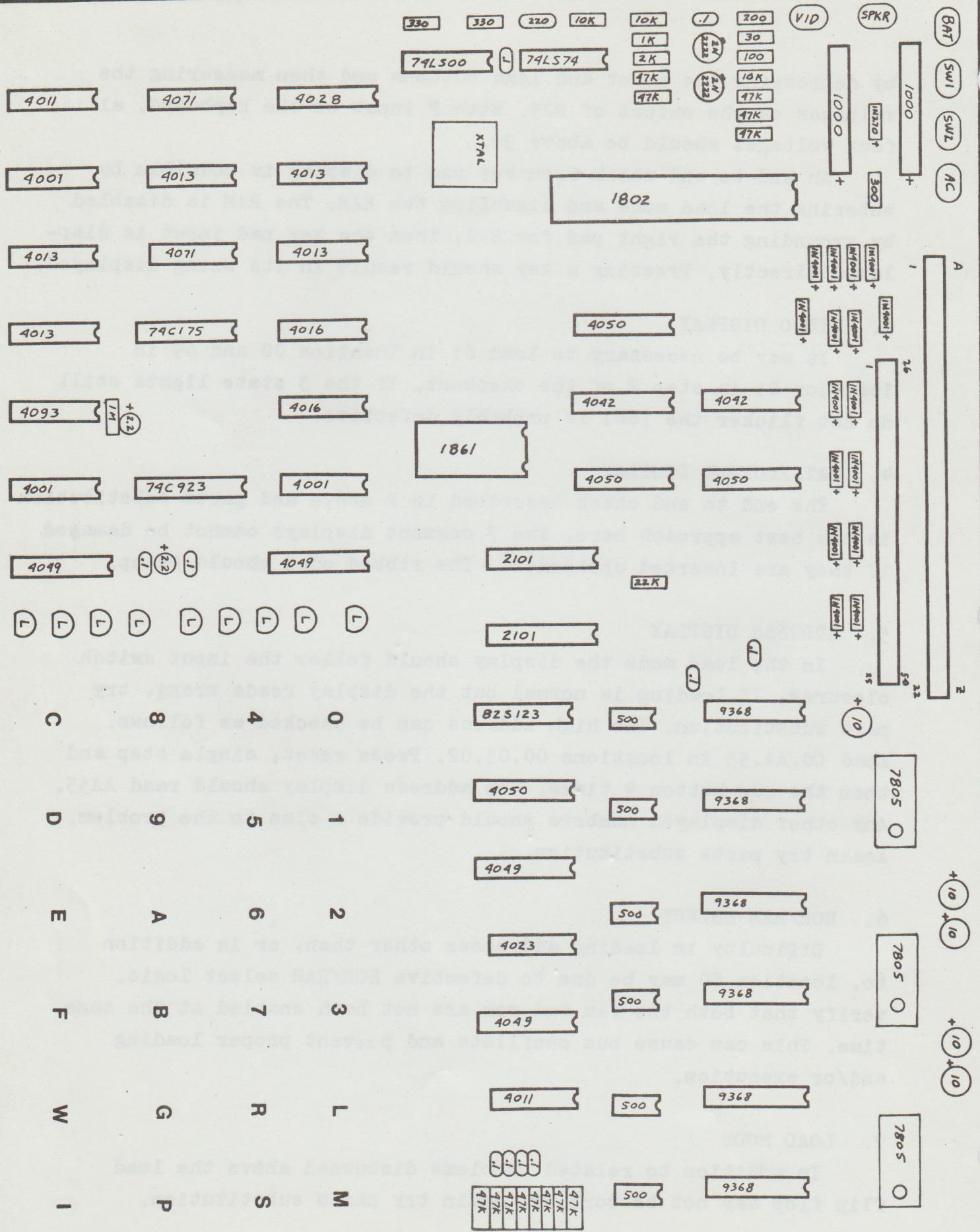
### 6. ROM/RAM SELECT

Difficulty in loading addresses other than, or in addition to, location 00 may be due to defective ROM/RAM select logic. Verify that both the ram and rom are not both enabled at the same time. This can cause bus conflicts and prevent proper loading and/or execution.

### 7. LOAD MODE

In addition to related problems discussed above the load flip flop may not be working. Again try parts substitution.

## COMPONENT LAYOUT (V 1.0)



**Figure 13**

COMPONENT LAYOUT V2.0

37

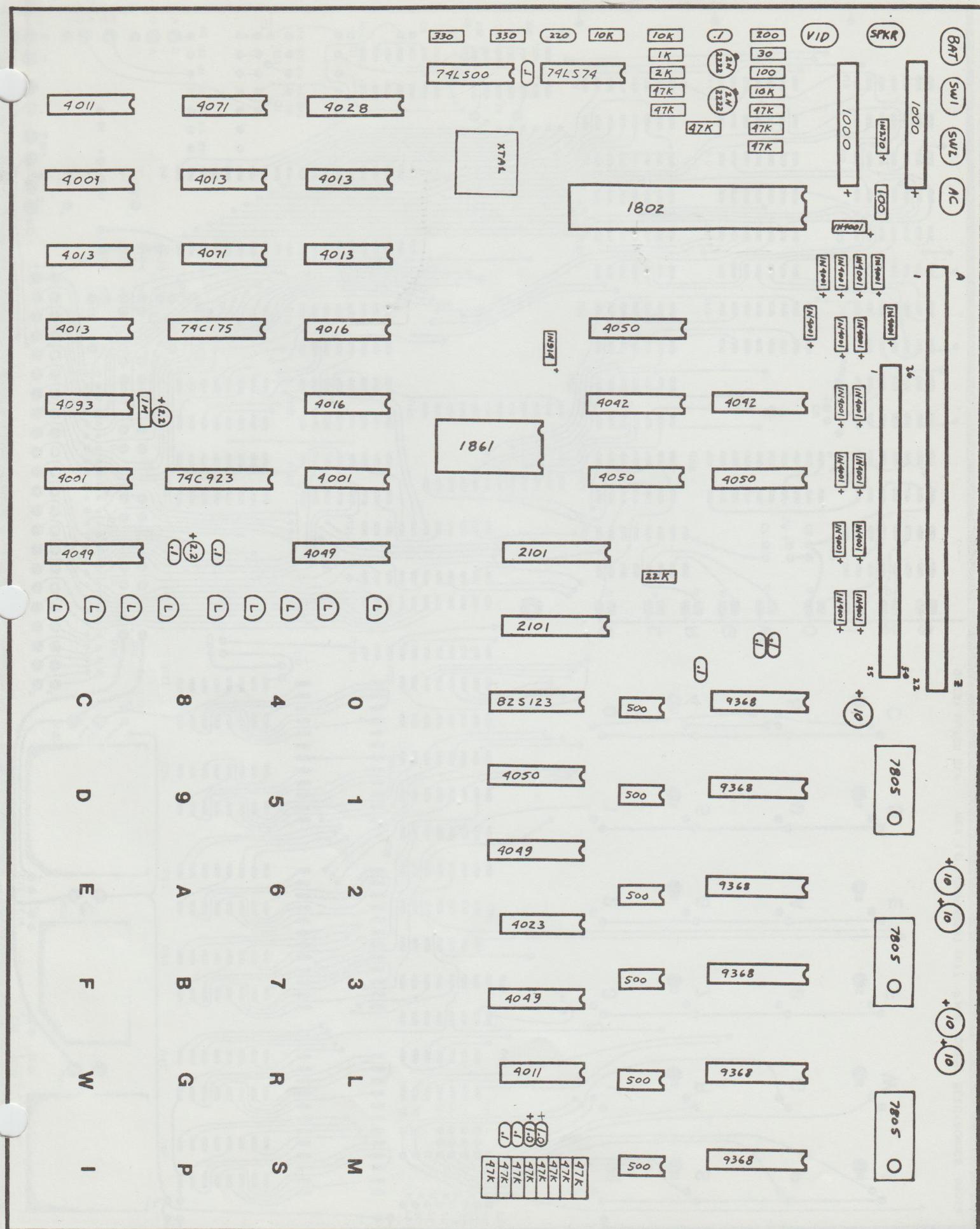


Figure 14

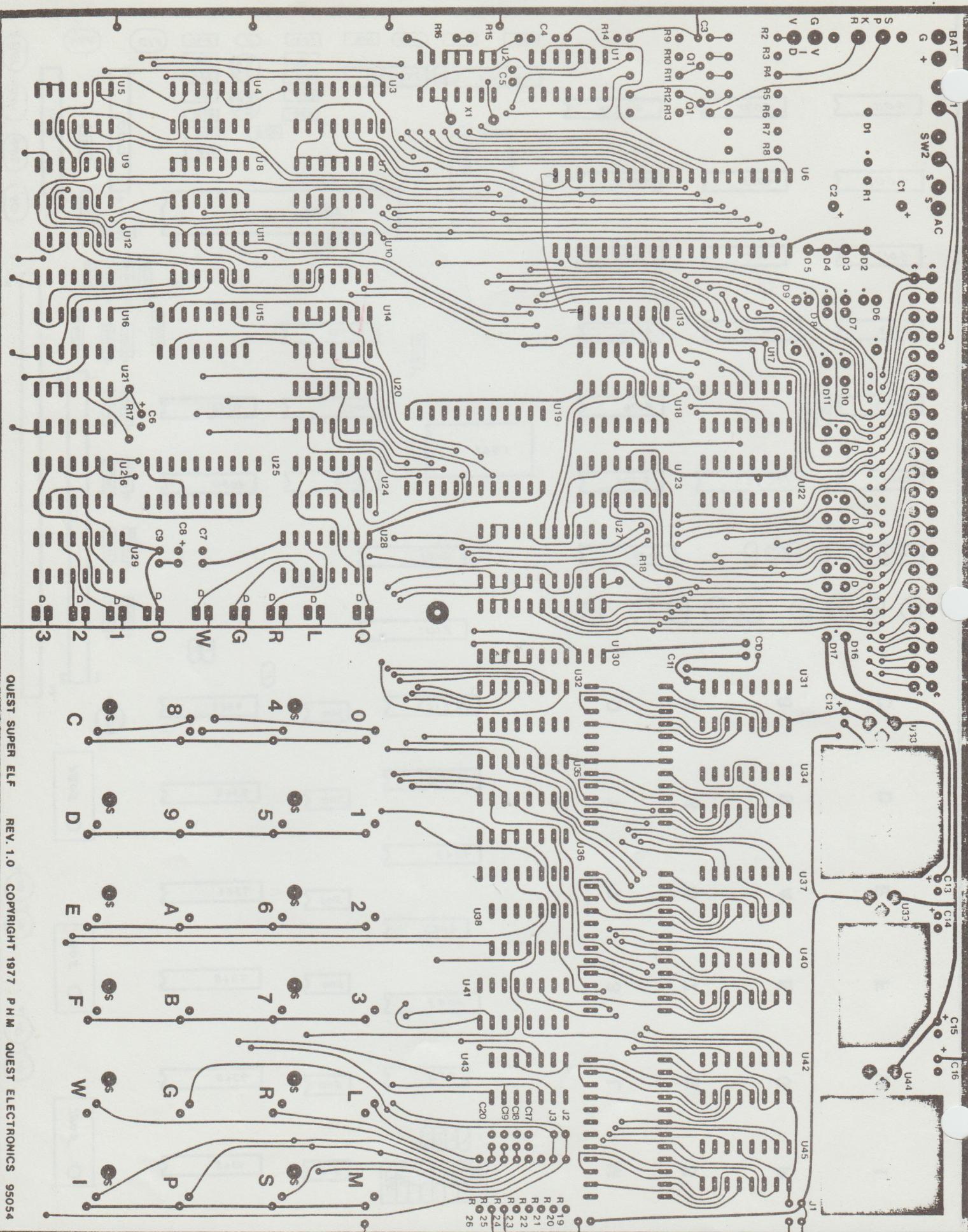


Figure 15

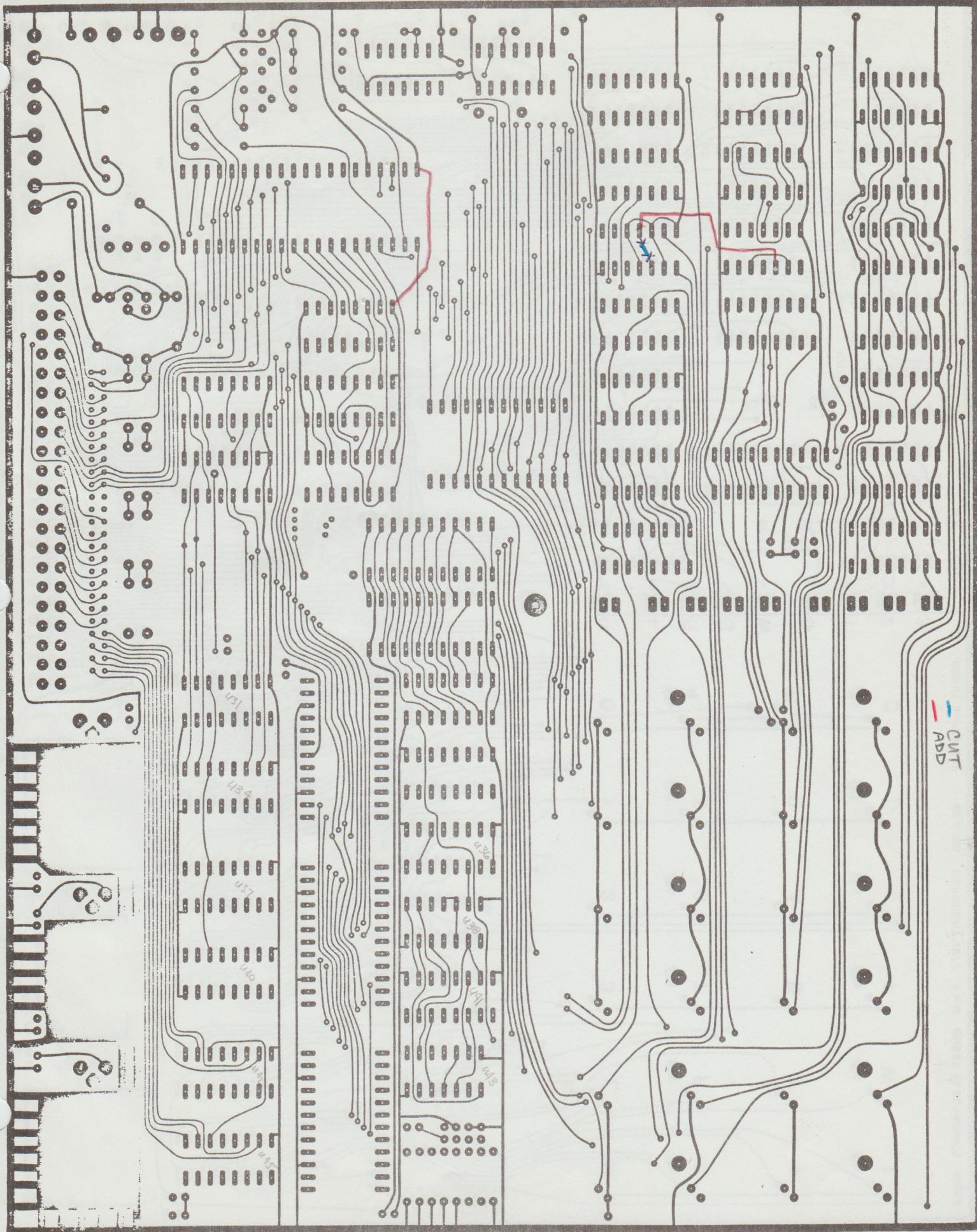


Figure 16

## BOARD WIRING PATTERN V 2.0 FRONT

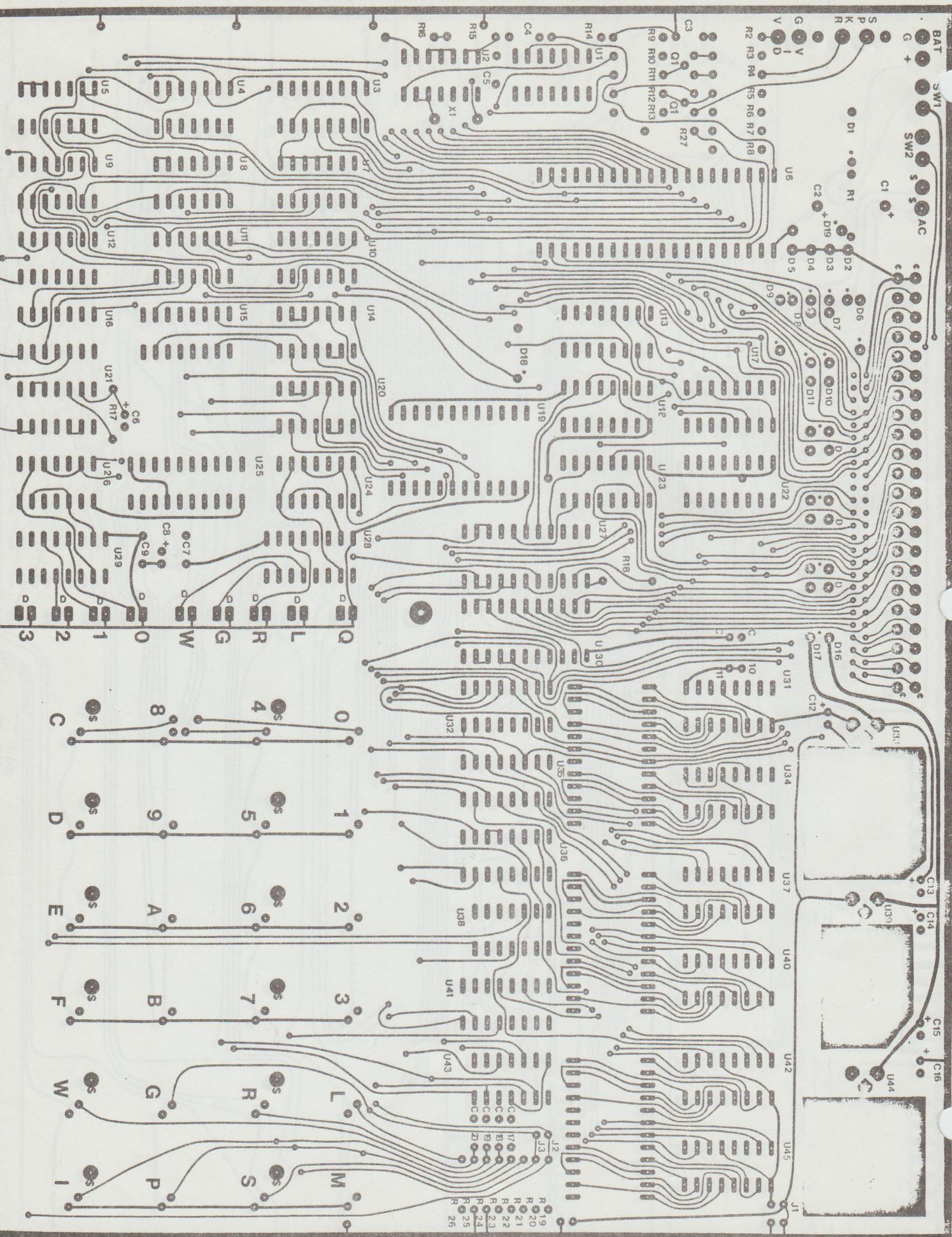


Figure 17

## BOARD WIRING PATTERN V.2.0 BACK

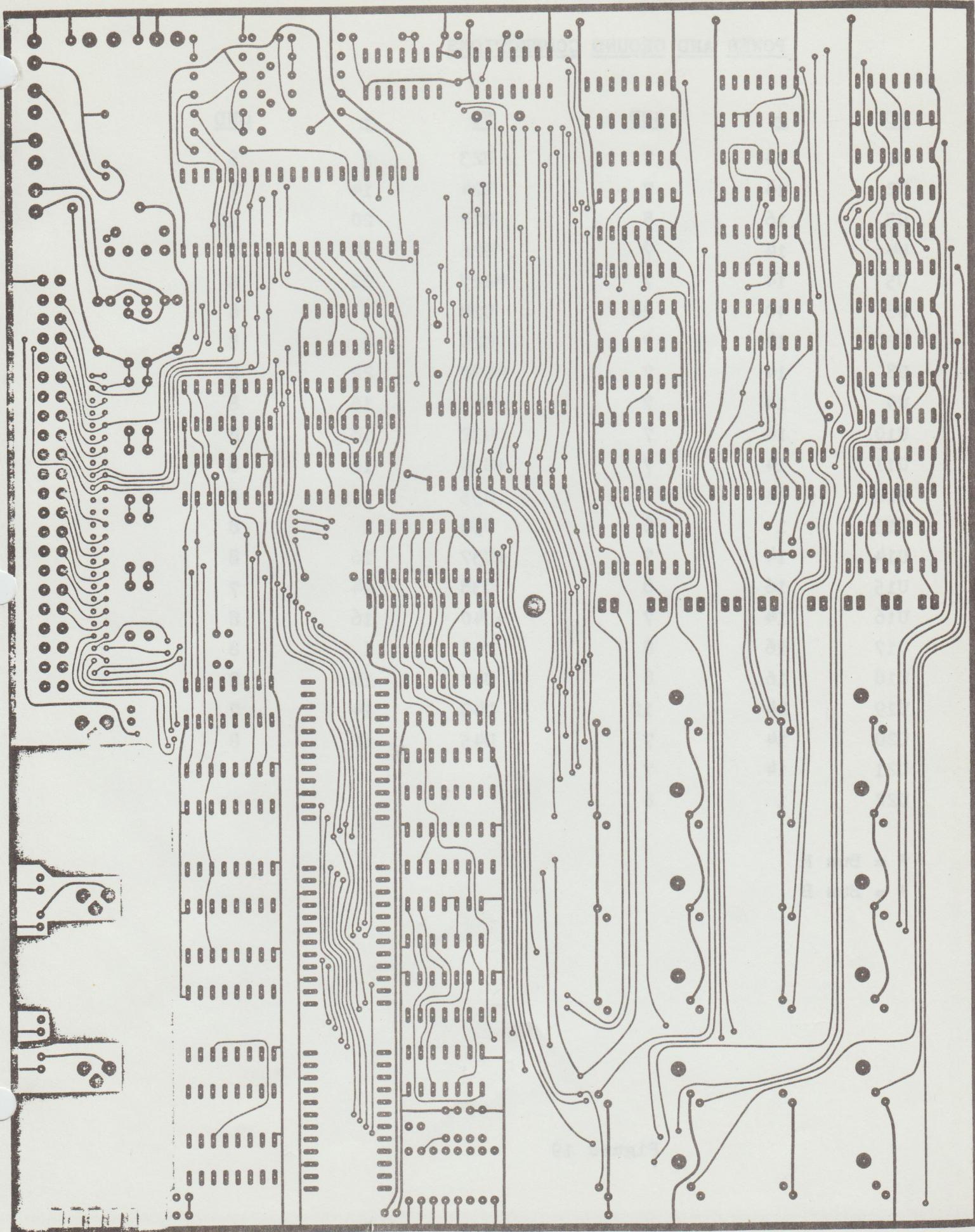


Figure 18

POWER AND GROUND CONNECTIONS

<u>NO</u>	<u>±</u>	<u>GND</u>	<u>NO</u>	<u>±</u>	<u>GND</u>
U1	14	7	U23	1	8
U2	14	7	U24	14	7
U3	16	8	U25	20	10
U4	14	7	U26	14	7
U5	14	7	*U27	22	8
U6	40	20	U28	1	8
U7	14	7	U29	1	8
U8	14	7	*U30	22	8
U9	14	7	+U31	16	8
U10	14	7	U32	16	8
U11	14	7	+U34	16	8
U12	14	7	U35	1	8
U13	1	8	U36	1	8
U14	14	7	+U37	16	8
U15	16	8	U38	14	7
U16	14	7	+U40	16	8
U17	16	8	U41	1	8
U18	16	8	U42	16	8
U19	24	12	U43	14	7
U20	14	7	U45	16	8
U21	14	7			
U22	1	8			

\* = Bus M

+ = Bus B

APPENDIX A PARTS LIST AND ASSEMBLY INSTRUCTIONS

1. PARTS LIST - BASIC

TYPE	NUMBER	QTY	DESCRIPTION
<b>INTEGRATED CIRCUITS</b>			
U1	74L74/74LS74	1	Dual D Flip-Flop
U2	74L00/74LS00	1	Quad 2-Input NAND Gate
U3	4028	1	BCD-to-Decimal Decoder
U4	4071	1	Quad 2-Input OR Gate
U5	4011	1	Quad 2-Input NAND Gate
U6	1802	1	COSMAC microprocessor
U7	4013	1	Dual D Flip-Flop
U8	4013	1	Dual D Flip-Flop
U9	4001	1	Quad 2-Input NOR Gate
U10	4013	1	Dual D Flip-Flop
U11	4071	1	Quad 2-Input OR Gate
U12	4013	1	Dual D Flip-Flop
U13	4050	1	Hex Non-Inverting Buffer
U14	4016/4116	1	Quad Bilateral Switch
U15	74C175	1	Quad D Flip-Flop
U16	4013	1	Dual D Flip-Flop
U19	1861	1	Video Display Controller
U20	4016/4116	1	Quad Bilateral Switch
U21	4093	1	Quad 2-Input NAND Schmidt Trigger
U23	4050	1	Hex Non-Inverting Buffer
U24	4001	1	Quad 2-Input NOR Gate
U25	74C923/8246	1	20-Key Encoder
U26	4001	1	Quad 2-Input NOR Gate
U27	2101/2101L/5101	1	256 x 4 MOS RAM
U28	4049	1	Hex Inverting Buffer
U29	4049	1	Hex Inverting Buffer
U30	2101/2101L/5101	1	256 x 4 MOS RAM
U32	82S123	1	32x8 PROM Programmed With Monitor
U35	4050	1	Hex Non-Inverting Buffer
U36	4049	1	Hex Inverting Buffer

TYPE	NUMBER	QTY	DESCRIPTION
<b>INTEGRATED CIRCUITS</b>			
U38	4023	1	Triple 3-Input NAND Gate
U41	4049	1	Hex Inverting Buffer
U42	9368	1	Hex Decoder Latch Driver
U43	4011	1	Quad 2-Input NAND Gate
U44	7805/340T-5	1	5V 1A Regulator
U45	9368	1	Hex Decoder Latch Driver
<b>RESISTORS</b>			
R2	200 OHM	1	½ Watt Carbon Film
R3	30 OHM	1	½ Watt Carbon Film
R4	100 OHM	1	½ Watt Carbon Film
R5	10K OHM	1	½ Watt Carbon Film
R6	47K OHM	1	½ Watt Carbon Film
R7	47K OHM	1	½ Watt Carbon Film
R8	47K OHM	1	½ Watt Carbon Film
R9	10K OHM	1	½ Watt Carbon Film
R10	1K OHM	1	½ Watt Carbon Film
R11	2K OHM	1	½ Watt Carbon Film
R12	47K OHM	1	½ Watt Carbon Film
R13	47K OHM	1	½ Watt Carbon Film
R14	10K OHM	1	½ Watt Carbon Film
R15	330 OHM	1	½ Watt Carbon Film
R16	330 OHM	1	½ Watt Carbon Film
R17	1M OHM	1	½ Watt Carbon Film
R18	22K OHM	1	½ Watt Carbon Film
R19	47K OHM	1	½ Watt Carbon Film
R20	47K OHM	1	½ Watt Carbon Film
R21	47K OHM	1	½ Watt Carbon Film
R22	47K OHM	1	½ Watt Carbon Film
R23	47K OHM	1	½ Watt Carbon Film
R24	47K OHM	1	½ Watt Carbon Film
R25	47K OHM	1	½ Watt Carbon Film
R26	47K OHM	1	½ Watt Carbon Film
R27	47K OHM	1	½ Watt Carbon Film

TYPE	NUMBER	QTY	DESCRIPTION
<b>CAPACITORS</b>			
C1	1000 MFD 16V	1	Electrolytic
C3	0.1 MFD 50V	1	Monolythic
C4	220 PFD 100V	1	Disc Ceramic
C5	0.1 MFD 50V	1	Monolythic
C6	2.2 MFD 25V	1	Tantalum
C7	0.1 MFD 50V	1	Monolythic
C8	2.2 MFD 25V	1	Tantalum
C9	0.1 MFD 50V	1	Monolythic
C10	0.1 MFD 50V	1	Monolythic
C11	0.1 MFD 50V	1	Monolythic
C15	10.0 MFD 35V	1	Tantalum
C16	10.0 MFD 35V	1	Monolythic
C17	1.0 MFD 50V	1	Tantalum
C18	1.0 MFD 50V	1	Tantalum
C19	0.1 MFD 50V	1	Monolythic
C20	0.1 MFD 50V	1	Monolythic
<b>DIODES</b>			
D2	1N4001	1	Silicon Rectifier
D3	1N4001	1	Silicon Rectifier
D6	1N4001	1	Silicon Rectifier
D7	1N4001	1	Silicon Rectifier
D10	1N4001	1	Silicon Rectifier
D12	1N4001	1	Silicon Rectifier
D14	1N4001	1	Silicon Rectifier
D16	1N4001	1	Silicon Rectifier
D18	1N914	1	Switching Diode
<b>MISCELLANEOUS-ELECTRICAL</b>			
Q1	2N2222A	1	Switching Transistor NPN
Q2	2N2222A	1	Switching Transistor NPN
X1	3579.545	1	Crystal
-	LED	9	Jumbo Red
-	FND 500	2	½" Seven Segment Display
-	10V16VA	1	117V Plug-In Transformer
-	Key Switch	6	4 Section NO Push Button Switch

TYPE	NUMBER	QTY	DESCRIPTION
<b>MISCELLANEOUS-ELECTRICAL</b>			
-	Speaker	1	
-	Wire	6 ft	Two Conductor Pwr Cord
-	Wire	2 ft	No. 26 Stranded
<b>MISCELLANEOUS - MECHANICAL</b>			
-	Heat Sink	1	Regulator Heat Sink
-	6-32 x 3/8 Screw	1	For Regulator
-	6-32 Lock Washer	1	For Regulator
-	6-32 Nut	1	For Regulator
-	2-56 Nut	12	For Key Switch
-	2-56 Lockwasher	12	For Key Switch
-	Key Tops	24	One Each 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F, L, R, G, W, M, S, P, I
-	40 Pin Socket	1	Low Profile
-	24 Pin Socket	1	Low Profile
-	24 Pin Socket	1	Standard or W.W.
-	22 Pin Socket	2	Low Profile
-	20 Pin Socket	1	Low Profile
-	14 Pin Socket	18	Low Profile
-	16 Pin Socket	13	Low Profile
-	Circuit Board	1	SUPER ELF

**2. PARTS LIST - OPTIONAL LOW ADDRESS DISPLAY**

TYPE	NUMBER	QTY	DESCRIPTION
U33	7805/340T-5	1	5V 1A Regulator
U37	9368	1	Hex Decoder Latch Driver
U40	9368	1	Hex Decoder Latch Driver
C2	1000 MFD 16V	1	Electrolytic
C12	10 MFD 25V	1	Tantalum
C13	10 MFD 25V	1	Tantalum
D4	1N4001	1	Silicon Rectifier
D5	1N4001	1	Silicon Rectifier
D8	1N4001	1	Silicon Rectifier

TYPE	NUMBER	QTY	DESCRIPTION
D9	1N4001	1	Silicon Rectifier
D11	1N4001	1	Silicon Rectifier
D13	1N4001	1	Silicon Rectifier
D15	1N4001	1	Silicon Rectifier
D17	1N4001	1	Silicon Rectifier
-	FND 500	2	½" Seven Segment Display
-	16 Pin Socket	2	Low Profile
-	24 Pin Socket	1	Standard Or W.W.
-	6-32 x 3/8 Screw	1	
-	6-32 Lockwasher	1	
-	6-32 Nut	1	
-	Heat Sink	1	

### 3. PARTS LIST - OPTIONAL HIGH ADDRESS DISPLAY

TYPE	NUMBER	QTY	DESCRIPTION
U17	4042	1	Quad Clocked D Latch
U18	4042	1	Quad Clocked D Latch
U22	4050	1	Hex Non-Inverting Buffer
U31	9368	1	Hex Decoder Latch Driver
U34	9368	1	Hex Decoder Latch Driver
-	FND 500	2	½" Seven Segment Display
-	16 Pin Socket	4	Low Profile
-	24 Pin Socket	1	Standard Or W.W.

### 4. PARTS LIST - OPTIONAL MEMORY SAVER

TYPE	NUMBER	QTY	DESCRIPTION
U39	7805/340T-5	1	
C14	10.0 MFD 35V	1	Tantalum
R1	300 OHM(100, V2.0)	1	½ Watt Carbon Resistor
D1	1N270	1	Germanium Diode
-	2 PST Switch	1	
-	1 AH Battery	2	NI-CAD Battery
-	Wire	4 ft	No. 24 Stranded
-	6-32x3/8 Screw	1	
-	6-32 Lockwasher	1	
-	6-32 Nut	1	
D19	1N4001(V2.0 Only)	1	Silicon Rectifier

NOTE: INTEL 5101L Rams may be substituted for the 2101L Rams to extend battery life from 20 hrs minimum to 4 weeks minimum.

## 5. PARTS LIST - OPTIONAL ACCESSORIES

- 44 Pin PC connector for Expansion Bus
- 50 Pin Ribbon cable connector for SUPER ELF Expander Board
- Video modulator kit
- 5101L Rams
- Custom hardwood case and front panel

## 6. ASSEMBLY INSTRUCTIONS - BASIC

Prior to starting assembly, please carefully read this manual and inspect the printed circuit board to observe the soldering skills and kit building experience required. If you have any doubts about your ability to assemble this kit or do not have the required tools we suggest that you exchange the kit for an assembled SUPER ELF.

You will need the following tools and supplies.

A. A 25 watt soldering iron with a small dia (.063 in. maximum) tip. A higher wattage iron usually has a tip temperature too high for safe printed circuit work. A lower wattage iron may take too long to heat the joint and result in poor solder joints. A larger tip diameter is likely to cause solder bridges.

B. A radio type rosin core solder of .032 in. dia maximum with an alloy of 60 to 65 percent tin. Do not use 50-50 solder as its melting point is much higher.

- C. Small screw driver.
- D. Small wrenches.
- E. Small diagonal cutters.
- F. Needlenose pliers
- G. Magnifying glass (to check for shorts)
- H. Multimeter (sensitivity at least 20000 OHMS/volt).
- I. Heat sink thermal grease.

NOTE: Failure to use good soldering techniques and the proper solder can void the warranty.

The following tools are not required but will be helpful if available.

- A. An IC insertion tool.
- B. A component lead bender.
- C. A nut driver set.

Check the parts in the kit against the parts list to insure that the kit is complete and to familiarize yourself with the parts. CAUTION: DO NOT remove the integrated circuits from the antistatic (black) foam they were shipped in until told to do so.

The printed circuit board is double-sided epoxy glass with plated through holes. The front of the board has component designations on it. All components are installed from the front and all soldering is on the back.

Carefully inspect both sides of the printed circuit board for shorts and defects. The top of the board is more critical since the sockets, etc., cover up the traces, and defects are harder to detect and correct. NOTE: Every board is carefully inspected, under magnification, prior to shipment and the above suggestion is a double check to minimize any inconvenience to you from undetected defects. Any defects found are of course covered by our warranty.

Referring to the component identification on the board and figure 2 component layout, start assembly using the following steps. NOTE: If you purchased options with your SUPER ELF, they can be added now or later. We recommend adding them now by doing all corresponding steps at one time. For example, install both the basic and optional sockets at the same time. CAUTION: in each of the following steps, be sure that you have installed the parts in the correct locations prior to soldering. This is particularly important if you did not buy all the options since some locations will be empty.

- ( ) A. Install low profile sockets for ICs U1 through U45 except for ICs listed as optional. Note: Install a socket for U18 as part of the basic kit. Slightly bend two leads on diagonally opposite corners to hold the socket in place while you turn the board over. Solder these two pins while the socket is

snug against the board. Before soldering the remaining pins, check to be sure the socket is seated on the board properly. SOLDER all the remaining pins.

( ) B. Install all the resistors. SOLDER. Trim off excess leads.

Note: Pre-bending resistors to a lead spacing of 0.4 inch with a lead bender will simplify this job.

( ) C. Install all the diodes. SOLDER. Trim off excess leads.

Note: Pre-bending diodes to a lead spacing of 0.4 inch is helpful. Note: The cathode (band) end of all diodes should be next to the hole with a dot or + sign. All diodes have their bands on the right side.

( ) D. Install the standard 24 pin socket horizontally in the right hand set of holes (below IC No. U42 and U45). SOLDER.

( ) E. Install the capacitors. SOLDER. Note: Observe polarity on the electrolytics and tantalums. Note: Some tantalums may not be marked with A+. These will have a colored dot on one side. With the leads down and the dot facing you, the right lead is +. The + leads of C17/C18 are nearest 'C17/C18'. *M.D.*

( ) F. Install the two transistors Q<sub>1</sub> and Q<sub>2</sub>. They should stand approximately 1/8 inch off the board. SOLDER.

( ) G. Install the LEDS. The base of the LED should be 3/16 to 1/4 inch from the board. The flat (or short lead or dot) should be toward the bottom of the board. SOLDER.

( ) H. Install the crystal. Carefully bend the leads 90 degrees so the crystal will lie down on its side on the board. One side of the crystal has a foam double-backed tape attached. Remove the protective paper, insert the leads in the holes, and gently press the crystal down on the board so the foam holds it in place. SOLDER.

( ) I. Install U44--the regulator. Bend the 3 leads down to fit the hole spacing. Put thermal grease on the bottom of the regulator and the bottom of the heat sink. Only a SMALL amount is required. Using a 6-32 x 3/8 screw, assemble in the following order. The screw goes through the regulator, then the heat sink, and then the PC board with a lockwasher and nut on the back. Tighten the screw carefully. Avoid over-tightening. The thermal grease is slippery and with a properly tightened assembly you can still move the heat sink with a little effort. SOLDER.

- ( ) J. Install the 6 4 key key switches. CAREFULLY straighten any bent leads so that they are nearly straight. (Overbending can cause breakage and they need not be perfect for installation). Position the switch over the holes with one end closer to the board and, using a thin screwdriver or other blade, gently push the leads into the holes one set at a time, moving from one end to the other. Start installing switch banks with the left column. Use an OHM meter to verify correct switch closure before installation since later removal of any multi-pin device (like these switches) is very difficult. When the switch bank is in place on the board use 2-56 nuts and lockwashers to bolt the switch down. Then SOLDER the leads.
- ( ) K. Connect the plug-in transformer to the board using the 6 foot long twisted pair wire. SOLDER to the connections labeled AC on the board.
- ( ) L. Cut the 2 foot wire in half and twist the two wires together. Using this wire connect the speaker to the connections labeled SPKR on the board. SOLDER.
- ( ) M. Omit this step if you purchased the high address option. Otherwise, using cut-off resistor leads, make 4 short jumpers and plug them into the socket for U18.
- Jumper 1 between pin 2 and pin 4.  
Jumper 2 between pin 7 and pin 10.  
Jumper 3 between pin 11 and pin 13.  
Jumper 4 between pin 1 and pin 14.
- Be sure the jumpers are short and do not touch each other. You can also use a 4042 instead of the jumpers. The purpose of the jumpers is to terminate the inputs to U23. Failure to terminate CMOS inputs may result in improper operation of other circuits on that IC and even destruction of that IC.
- ( ) N. Install the integrated circuits. The 14 and 16 pin ICs can be installed using an insertion tool. Most IC leads are spread at the tip and must be bent inward to provide the right row spacing to fit the socket. Most of the ICs are CMOS types and require extra care in handling to prevent static damage. Grounding yourself and the board is recommended. Also avoid wearing nylon or other synthetic clothing during this step.

- ( ) O. Install the seven segment displays in the 24 pin standard socket. The grooved side goes up (like the notch on the ICs). Install the two displays on the ends of the socket, leaving two socket pins empty between the displays. (Pins 6 and 7, 18 and 19, of the 24 pin socket are not used by the displays.)
- ( ) P. This completes the basic SUPER ELF.

## 7. ASSEMBLY INSTRUCTIONS LOW ADDRESS DISPLAY OPTION

Refer to corresponding steps in the basic assembly instructions for more details.

- ( ) A. Install the low profile sockets. SOLDER.
- ( ) B. Install the diodes. SOLDER.
- ( ) C. Install the capacitors. SOLDER.
- ( ) D. Install the regulator and heat sink. SOLDER.
- ( ) E. Install the standard 24 pin socket in the space provided below U37 and U40. SOLDER.
- ( ) F. Install the ICs.
- ( ) G. Install the seven segment displays spaced apart like the data displays.
- ( ) H. This completes the high address display option.

## 8. ASSEMBLY INSTRUCTIONS HIGH ADDRESS DISPLAY OPTION

Refer to corresponding steps in the basic assembly instructions for more details.

- ( ) A. Install the low profile IC sockets. SOLDER.
- ( ) B. Install the standard 24 pin socket in the space provided below U31 and U34. SOLDER.
- ( ) C. Install the ICs.
- ( ) D. Install the seven segment displays spaced apart like the data displays.
- ( ) E. This completes the high address display option.

## 9. ASSEMBLY INSTRUCTIONS MEMORY SAVER OPTION

Refer to corresponding steps in the basic assembly instructions for more details.

- ( ) A. Install the regulator. NOTE: No heat sink is necessary. SOLDER.

- ( ) B. Install the capacitor. SOLDER.
- ( ) C. Install the resistor. SOLDER.
- ( ) D. Install the diode. SOLDER.
- ( ) E. Connect the two batteries in series with a short length of wire.
- ( ) F. Cut two 10 to 12 inch lengths of wire and connect the battery to the PC board BAT connections. OBSERVE POLARITY. SOLDER.
- ( ) G. Cut the remaining wire into 4 equal lengths. Using two wires, connect one pole of the two pole slide switch to the PC board SW1 connections. SOLDER. Using the other two wires, connect the other pole of the two pole switch to the PC board SW2 connections. SOLDER. NOTE: If the switch supplied has more than 4 terminals, be sure that you wire up the switch as a two pole single throw switch.
- ( ) H. On the front of the PC board cut jumper J1 (near the right top side of U45).
- ( ) K. This completes the memory saver option.

#### 10. INITIAL CHECKOUT

The following steps will provide you with an orderly approach to an initial functional circuit verification. If you fail to obtain the proper response, refer to the sections on troubleshooting and logic design. Or, if you wish, return your SUPER ELF and we will replace any defective parts without charge. Charges will be made for any parts damaged through improper assembly, etc.

- A. Plug the transformer in and verify:
  - (1) The displays are lit.
  - (2) Only one mode LED is lit.
  - (3) Only one state LED is lit.
- B. Push the RESET button and verify:
  - (1) The R LED is lit.
  - (2) The 1 LED is lit.
- C. Push the LOAD button and verify:
  - (1) The L LED is lit.
  - (2) The 1 LED is lit.

- D. Push the RESET button and verify:
  - (1) The R LED is lit.
  - (2) The 1 LED is lit.
- E. Push the RUN button and verify:
  - (1) The G LED is lit.
  - (2) The 1 LED is lit.
  - (3) The 0 LED may be lit depending upon the contents of memory.
- F. Push the WAIT button and verify:
  - (1) The W LED is lit.
  - (2) Either (but not both) the 0 LED or the 1 LED is lit.
- G. Push the RUN button and verify:
  - (1) The G LED is lit.
  - (2) The 1 LED is lit.
  - (3) The 0 LED may be lit.
- H. Push the RESET button and then the LOAD button and verify:
  - (1) The L LED is lit.
  - (2) The 1 LED is lit.
- I. Push the 0 and then the 1 button on the HEX keypad. Push the INPUT button and verify:
  - (1) The data displays show 01.
  - (2) The address displays show 0000.
- J. Push the 2 button on the HEX keypad and then push the INPUT switch and verify:
  - (1) The data displays show 12.
  - (2) The address displays show 0001.
- K. Repeat Step J above using the other HEX keys verifying corresponding outputs. If you make no mistakes, location 000E will contain EF.
- L. Push RESET, LOAD, MEMORY PROTECT, and INPUT in that order and verify:
  - (1) The data displays show 01.
  - (2) The address displays show 0000.
- M. Push the INPUT switch and you can step through MEMORY reading out what you loaded in steps I, J, and K.
- N. Repeat Step L and then push the WAIT button, the F button twice on the HEX keypad and the INPUT button and verify:
  - Location 0002 contains FF.

O. Push the MEMORY PROTECT button and the INPUT button and verify:

Location 0002 contains 23.

P. Push RESET, MONITOR SELECT, LOAD, AND INPUT buttons in that order and verify:

Location 0000 contains F8

Q. Continue pushing the INPUT button to read out the contents of the Monitor.

R. Push RESET, MONITOR SELECT, and SINGLE STEP buttons in that order. Push the 0 Button and then the 2 button. Then push the RUN button but do not hold it in and verify:

(1) The W LED is lit.

(2) The 0 LED is lit.

(3) Location 0000 contains F8.

S. Push the RUN button but do not hold it in and verify:

(1) The W LED is lit.

(2) The 1 LED is lit.

(3) The address/data display shows 000120.

T. Push the RUN button again and verify:

(1) The W LED is lit.

(2) The 0 LED is lit.

(3) The address/data display shows 0002A1

U. Push the RUN button again and verify:

(1) The W LED is lit.

(2) The 1 LED is lit.

(3) The address/data display shows XX2020 (where XX can be any value and is CPU chip dependent).

V. Push and hold the RUN button down and verify:

(1) After approximately one second, the CPU will cycle through machine cycles at a rate of 1 to 2 per second.

(2) Shortly the displays will alternate between 000807 and 00073F. This is the point in the MONITOR where the MONITOR is waiting for an INPUT switch closure. At this point release the RUN button.

W. Push the WAIT button and then push the RUN button and verify:

(1) The display is either 00083F or 000807.

(2) The G LED is lit.

(3) The 0 and 1 LEDS are both lit.

X. Push the 5 and 0 buttons and then the INPUT button and verify:

The Q light comes on. No other change should be observed.

Y. Load the following program starting in Location zero - 7A, 3F, 00, 7B, 30, 01. After loading, push RESET and RUN.

Verify:

(1) The Q light is on while the INPUT switch is depressed.

(2) Pushing the INPUT switch causes a clicking sound in the speaker.

Z. Load A 69 into Location zero and press RESET and RUN and verify:

(1) The address displays flicker and appear to display 8888.

(2) The data display displays 69.

(3) The G LED is lit.

(4) The 0, 1, and 2 LEDS are lit.

(5) If you are connected to a MONITOR, you will see a row of vertical bars.

AA. If you have the Memory Saver option installed, reload the program from Step Y above. Set the slide switch to ON (contacts closed). Note that you should be in the RESET mode. Remove power from the board and then turn it back on. Hit RESET and set the slide switch to the OFF (contacts open) position. Pushing RUN should provide the same results as it did in Step Y. NOTE: Before performing this check, charge the batteries by leaving power on for several hours ( 24-36 hours are required for a full charge ).

This completes the initial checkout of your SUPER ELF.

Additional operational information is contained in Section II.

NOTE: If you have low line voltage (117 vac), it may be necessary to short out one or two of the series diodes D14, D16. Low line voltage can cause a weaving of the bars in step Z above. Short out the diodes one at a time to stop the weaving. If the weaving does not stop with two diodes shorted, the cause is not low line voltage.

- ( ) B. Install the capacitor. SOLDER.
- ( ) C. Install the resistor. SOLDER.
- ( ) D. Install the diode. SOLDER.
- ( ) E. Connect the two batteries in series with a short length of wire.
- ( ) F. Cut two 10 to 12 inch lengths of wire and connect the battery to the PC board BAT connections. OBSERVE POLARITY. SOLDER.
- ( ) G. Cut the remaining wire into 4 equal lengths. Using two wires, connect one pole of the two pole slide switch to the PC board SW1 connections. SOLDER. Using the other two wires, connect the other pole of the two pole switch to the PC board SW2 connections. SOLDER. NOTE: If the switch supplied has more than 4 terminals, be sure that you wire up the switch as a two pole single throw switch.
- ( ) H. On the front of the PC board cut jumper J1 (near the right top side of U45).
- ( ) K. This completes the memory saver option.

#### 10. INITIAL CHECKOUT

The following steps will provide you with an orderly approach to an initial functional circuit verification. If you fail to obtain the proper response, refer to the sections on troubleshooting and logic design. Or, if you wish, return your SUPER ELF and we will replace any defective parts without charge. Charges will be made for any parts damaged through improper assembly, etc.

A. Plug the transformer in and verify:

- (1) The displays are lit.
- (2) Only one mode LED is lit.
- (3) Only one state LED is lit.

B. Push the RESET button and verify:

- (1) The R LED is lit.
- (2) The 1 LED is lit.

C. Push the LOAD button and verify:

- (1) The L LED is lit.
- (2) The 1 LED is lit.

DO #1 MODIFICATION  
ON Pg 89 NO POWER  
FRONT PAGE THIS SECTION  
COMPLETED

- D. Push the RESET button and verify:
- (1) The R LED is lit.
  - (2) The 1 LED is lit.
- E. Push the RUN button and verify:
- (1) The G LED is lit.
  - (2) The 1 LED is lit.
  - (3) The 0 LED may be lit depending upon the contents of memory.
- F. Push the WAIT button and verify:
- (1) The W LED is lit.
  - (2) Either (but not both) the 0 LED or the 1 LED is lit.
- G. Push the RUN button and verify:
- (1) The G LED is lit.
  - (2) The 1 LED is lit.
  - (3) The 0 LED may be lit.
- H. Push the RESET button and then the LOAD button and verify:
- (1) The L LED is lit.
  - (2) The 1 LED is lit.
- I. Push the 0 and then the 1 button on the HEX keypad. Push the INPUT button and verify:
- (1) The data displays show 01.
  - (2) The address displays show 0000.
- J. Push the 2 button on the HEX keypad and then push the INPUT switch and verify:
- (1) The data displays show 12.
  - (2) The address displays show 0001.
- K. Repeat Step J above using the other HEX keys verifying corresponding outputs. If you make no mistakes, location 000E will contain EF.
- L. Push RESET, LOAD, MEMORY PROTECT, and INPUT in that order and verify:
- (1) The data displays show 01.
  - (2) The address displays show 0000.
- M. Push the INPUT switch and you can step through MEMORY reading out what you loaded in steps I, J, and K.
- N. Repeat Step L and then push the WAIT button, the F button twice on the HEX keypad and the INPUT button and verify:  
Location 0002 contains FF.

O. Push the MEMORY PROTECT button and the INPUT button and verify:

Location 0002 contains 23.

P. Push RESET, MONITOR SELECT, LOAD, AND INPUT buttons in that order and verify:

Location 0000 contains F8

Q. Continue pushing the INPUT button to read out the contents of the Monitor.

R. Push RESET, MONITOR SELECT, and SINGLE STEP buttons in that order. Push the 0 Button and then the 2 button. Then push the RUN button but do not hold it in and verify:

(1) The W LED is lit.

(2) The 0 LED is lit.

(3) Location 0000 contains F8.

S. Push the RUN button but do not hold it in and verify:

(1) The W LED is lit.

(2) The 1 LED is lit.

(3) The address/data display shows 000120.

T. Push the RUN button again and verify:

(1) The W LED is lit.

(2) The 0 LED is lit.

(3) The address/data display shows 0002A1

U. Push the RUN button again and verify:

(1) The W LED is lit.

(2) The 1 LED is lit.

(3) The address/data display shows XX2020 (where XX can be any value and is CPU chip dependent).

V. Push and hold the RUN button down and verify:

(1) After approximately one second, the CPU will cycle through machine cycles at a rate of 1 to 2 per second.

(2) Shortly the displays will alternate between 000807 and 00073F. This is the point in the MONITOR where the MONITOR is waiting for an INPUT switch closure. At this point release the RUN button.

W. Push the WAIT button and then push the RUN button and verify:

(1) The display is either 00083F or 000807.

(2) The G LED is lit.

(3) The 0 and 1 LEDS are both lit.

X. Push the 5 and 0 buttons and then the INPUT button and verify:

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Verify:

(1) The Q light is on while the INPUT switch is depressed.

(2) Pushing the INPUT switch causes a clicking sound in the speaker.

Z. Load A 69 into Location zero and press RESET and RUN and verify:

(1) The address displays flicker and appear to display 8888.

(2) The data display displays 69.

(3) The G LED is lit.

(4) The 0, 1, and 2 LEDS are lit.

(5) If you are connected to a MONITOR, you will see a row of vertical bars.

AA. If you have the Memory Saver option installed, reload the program from Step Y above. Set the slide switch to ON (contacts closed). Note that you should be in the RESET mode. Remove power from the board and then turn it back on. Hit RESET and set the slide switch to the OFF (contacts open) position. Pushing RUN should provide the same results as it did in Step Y. NOTE: Before performing this check, charge the batteries by leaving power on for several hours ( 24-36 hours are required for a full charge ).

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Additional operational information is contained in Section II