CD4018B Types

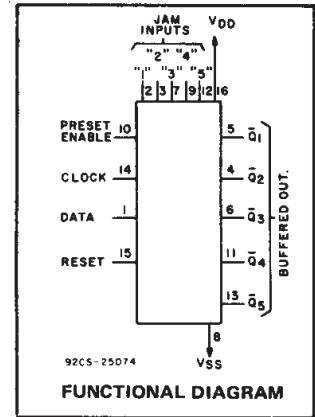## CMOS Presettable Divide-By-'N' Counter

High-Voltage Types (20-Volt Rating)

■ CD4018B types consist of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, $\overline{Q}1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5; or 3 counter configurations can be implemented by the use of a CD4011B to gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018B units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.
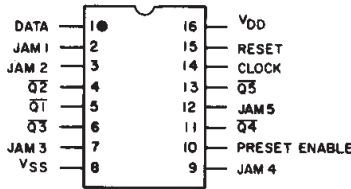
The CD4018B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

■ Medium speed operation . . . . 10 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V
■ Fully static operation
■ 100% tested for quiescent current at 20 V
■ Standardized, symmetrical output characteristics
■ 5-V, 10-V, and 15-V parametric ratings
■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Noise margin (full package-temperature range) =   1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

FUNCTIONAL DIAGRAM

Applications:

■ Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
■ Fixed and programmable counters greater than 10
■ Programmable decade counters
■ Divide-by-"N" counters/frequency synthesizers
■ Frequency division
■ Counter control/timers

TERMINAL DIAGRAM
Top View

92CS-24460

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  Voltages referenced to V_{SS} Terminal) . . . . –0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = –55°C to +100°C 500mW
  For T_A = +100°C to +125°C . . . . Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE–TEMPERATURE RANGE (All Package Types) 100mW
OPERATING–TEMPERATURE RANGE (T_A) . . . . –55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . –65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max . . . . +265°C

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4018B Types

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC		V_{DD}	Min.	Max.	UNITS
Supply Voltage Range (at T_A = Full Package-Temperature Range)			3	18	V
Clock Input Frequency,	f_{CL}	5	—	3	MHz
		10	—	7	
		15	—	8.5	
Clock Pulse Width,	t_W	5	160	—	ns
		10	70	—	
		15	50	—	
Clock Rise & Fall Time,	t_rCL, t_fCL	5	Unlimited		μs
		10			
		15			
Data Input Set-Up Time,	t_S	5	40	—	ns
		10	12	—	
		15	16	—	
Data Input Hold Time,	t_H	5	140	—	ns
		10	80	—	
		15	60	—	
Preset or Reset Pulse Width,	t_W	5	160	—	ns
		10	70	—	
		15	50	—	
Preset or Reset Removal Time		5	160	—	ns
		10	60	—	
		15	40	—	

Fig. 1 — Logic diagram.

Fig. 2 — Detail of a typical stage.

92CM-28752

* ALL INPUTS PROTECTED BY CMOS INPUT PROTECTION NETWORK

CD4018B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARAC-TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	mA
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	±10⁻⁵	±0.1	µA
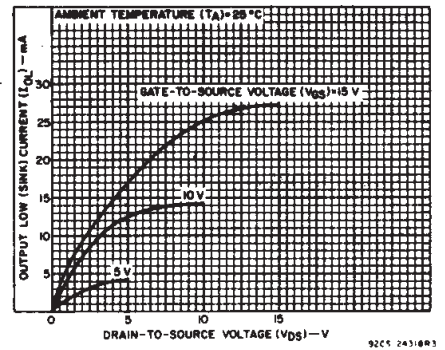
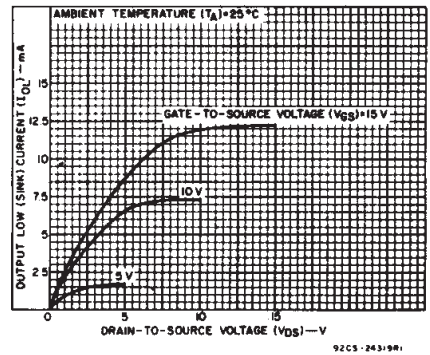Fig. 3 — Typical output low (sink) current characteristics.

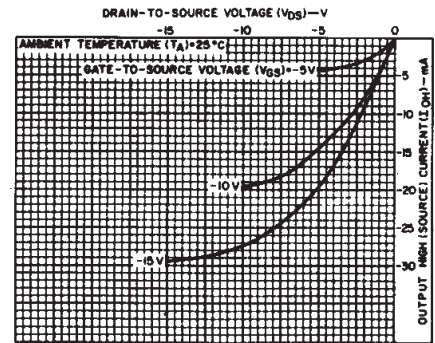Fig. 4 — Minimum output low (sink) current characteristics.

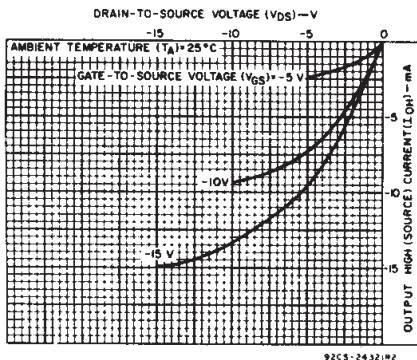Fig. 5 — Typical output high (source) current characteristics.

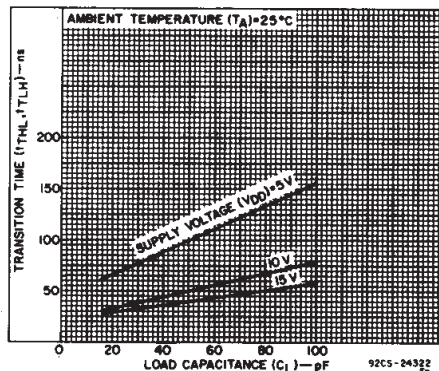Fig. 6 — Minimum output high (source) current characteristics.

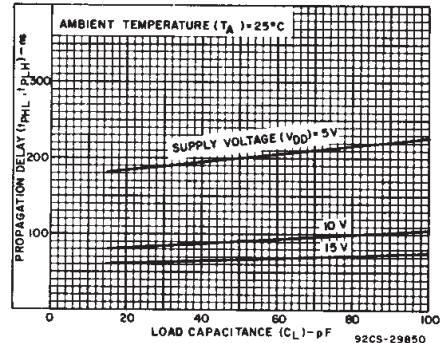Fig. 7 — Typical transition time as a function of load capacitance.

Fig. 8 — Typical propagation delay time as a function of load capacitance (CLOCK to Q).

3 COMMERCIAL CMOS HIGH VOLTAGE ICs

DYNAMIC ELECTRICAL CHARATERISTICS at $T_A = 25°C$, Input $t_r, t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	V_{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION					
Propagation Delay Time; t_{PLH}, t_{PHL}	5	—	200	400	ns
	10	—	90	180	
	15	—	65	130	
Transition Time; t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Maximum Clock Input Frequency, f_{CL}	5	3	6	—	MHz
	10	7	14	—	
	15	8.5	17	—	
Minimum Clock Pulse Width, t_W	5	—	80	160	ns
	10	—	35	70	
	15	—	25	50	
Clock Rise & Fall Time; t_rCL, t_fCL	5				μs
	10		Unlimited		
	15				
Minimum Data Input Set-Up Time. t_S	5	—	20	40	ns
	10	—	6	12	
	15	—	3	6	
Minimum Data Input Hold Time, t_H	5	—	70	140	ns
	10	—	40	80	
	15	—	30	60	
Average Input Capacitance, C_I	Any Input	—	5	7.5	pF
PRESET* OR RESET OPERATION					
Propagation Delay Time; Preset or Reset to $\overline{Q}$ t_{PLH}, t_{PHL}	5	—	275	550	ns
	10	—	125	250	
	15	—	90	180	
Minimum Preset or Reset Pulse Width, t_W	5	—	80	160	ns
	10	—	35	70	
	15	—	25	50	
Minimum Preset or Reset Removal Time	5	—	80	160	ns
	10	—	30	60	
	15	—	20	40	

* At PRESET ENABLE or JAM Inputs.

Fig. 9 — Typical propagation delay time as a function of load capacitance (RESET to Q).

Fig. 10 — Typical dynamic power dissipation as a function of clock input frequency.
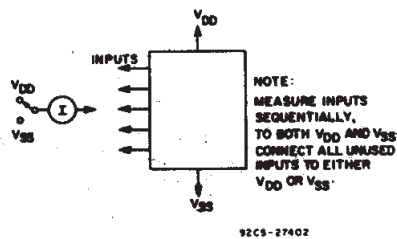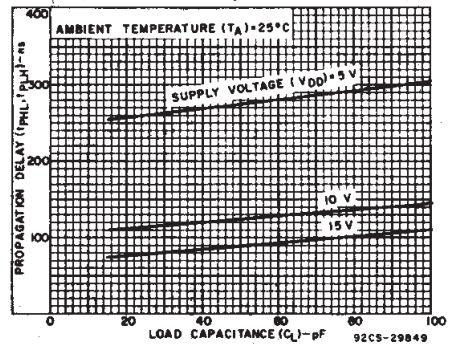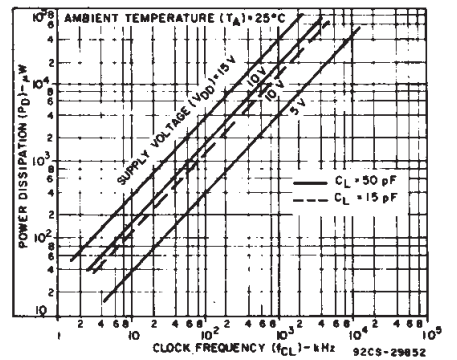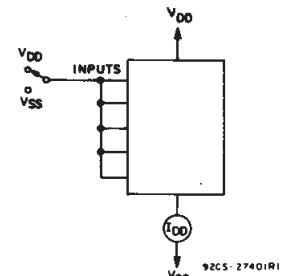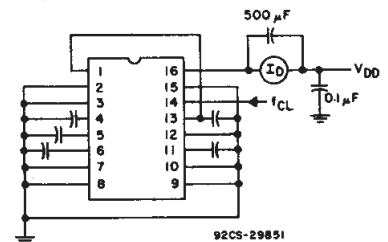

Fig. 11 — Quiescent device current test circuit.

Fig. 12 — Input voltage test circuit.

Fig. 13 — Input current test circuit.

Fig. 14 — Dynamic power dissipation test circuit.

("DATA" INPUT TIED TO $\overline{Q}_5$ FOR DECADE COUNTER CONFIGURATION)

CLOCK
RESET
PRESET
Jam$_1$
Jam$_2$
Jam$_3$
Jam$_4$
Jam$_5$
$\overline{Q}_1$
$\overline{Q}_2$
$\overline{Q}_3$
$\overline{Q}_4$
$\overline{Q}_5$

DON'T CARE UNTIL "PRESET" GOES HIGH

92SS-4148R2
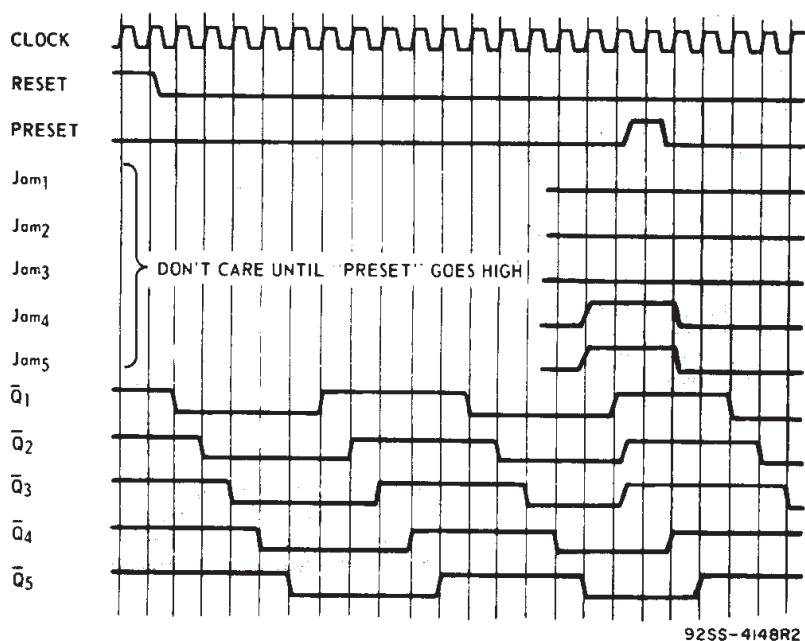
Fig. 15 — Timing diagram.

EXTERNAL CONNECTIONS FOR DIVIDE
BY 10, 9, 8, 7, 6, 5, 4, 3 OPERATION

DIVIDE BY 10	$\overline{Q}_5$	
DIVIDE BY 8	$\overline{Q}_4$	CONNECTED BACK TO "DATA"
DIVIDE BY 6	$\overline{Q}_3$	NO EXTERNAL COMPONENTS REQUIRED
DIVIDE BY 4	$\overline{Q}_2$	
DIVIDE BY 2	$\overline{Q}_1$	

DIVIDE BY 9   1/2 CD4011B
$\overline{Q}_4$
$\overline{Q}_5$ CONNECTED BACK TO "DATA" (SKIPS "ALL-1's" STATE)

DIVIDE BY 7   1/2 CD4011B
$\overline{Q}_3$
$\overline{Q}_4$ CONNECTED BACK TO "DATA" (SKIPS "ALL-1's" STATE)

DIVIDE BY 5   1/2 CD4011B
$\overline{Q}_2$
$\overline{Q}_3$ CONNECTED BACK TO "DATA" (SKIPS "ALL-1's" STATE)

DIVIDE BY 3   1/2 CD4011B
$\overline{Q}_1$
$\overline{Q}_2$ CONNECTED BACK TO "DATA" (SKIPS "ALL-1's" STATE)

92CS-1707IR3

Fig. 16 — External connections for divide by 10, 9, 8, 7, 5, 4, 3, 2 operation.

85-93
(2.159-2.362)

4-10
(0.102-0.254)

77-85
(1.956-2.159)

92CM-29853
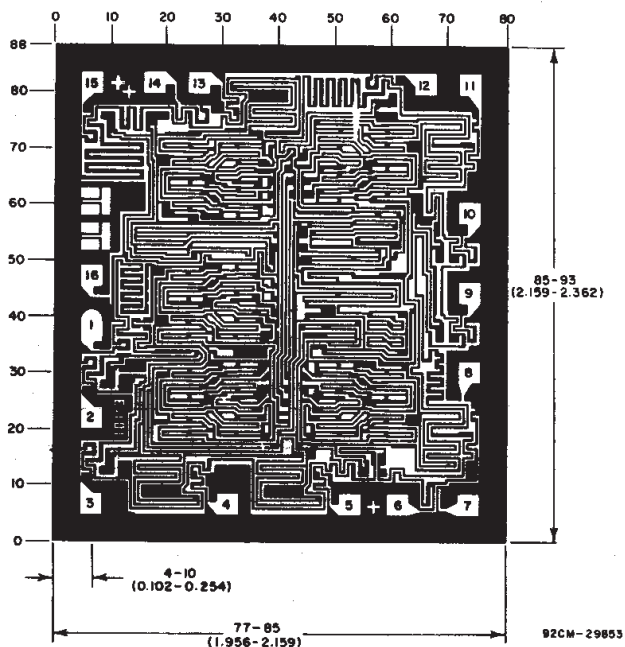
Chip dimensions and pad layout for CD4018B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

| J1 | J2 | J3 | J4 | J5 | ⏚ |

CL
D
R $\overline{Q3}$ $\overline{Q4}$

CL ÷ 7

92CS-35270

Fig. 17 — Example of divide by 7.

PACKAGING INFORMATION

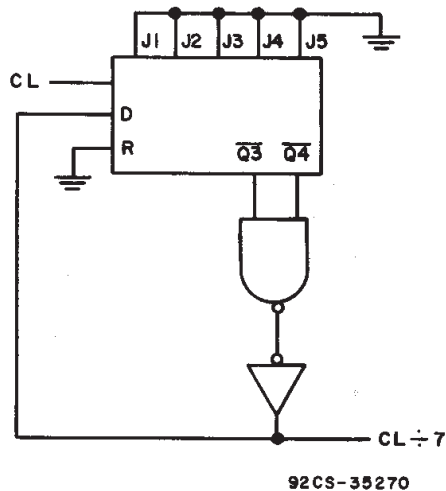| Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD4018BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4018BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4018BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4018BM	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4018BM96	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4018BMT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4018BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4018BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4018BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
JM38510/05652BEA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

N (R−PDIP−T**)　　　　　PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES:　A. All linear dimensions are in inches (millimeters).
　　　　B. This drawing is subject to change without notice.
　　　　C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
　　　　D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G16) PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/F   07/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM	PINS ** 14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-153

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