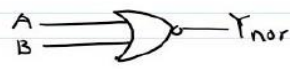
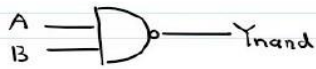


\* 2 i/p NAND, 2 i/p NOR Gates:-

2 i/p NAND

2 i/p NOR

Symbols:



Expression:

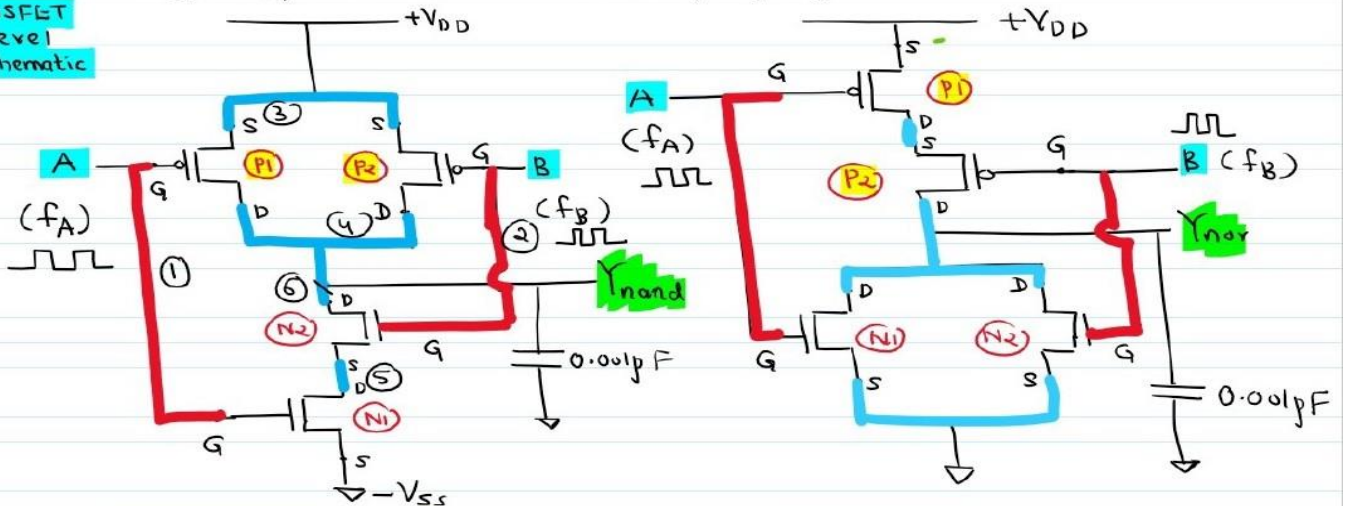
$$Y_{nand} = \overline{A \cdot B}$$

(P1/P2), (N1-N2)

$$Y_{nor} = \overline{A + B}$$

(P1-P2), (N1/N2)

MOSFET Level Schematic

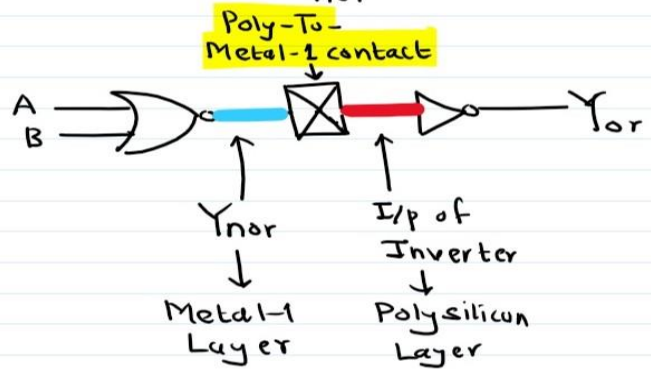
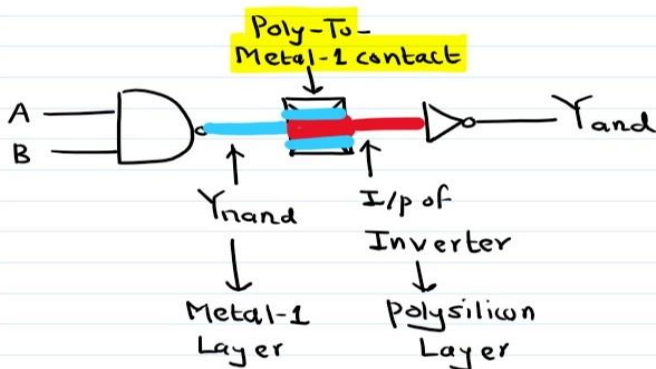
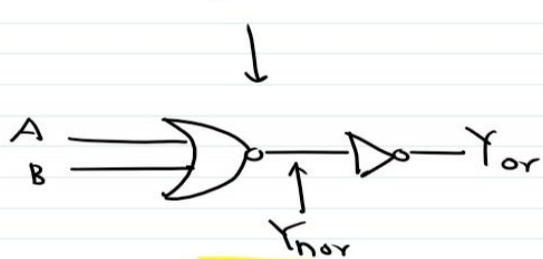
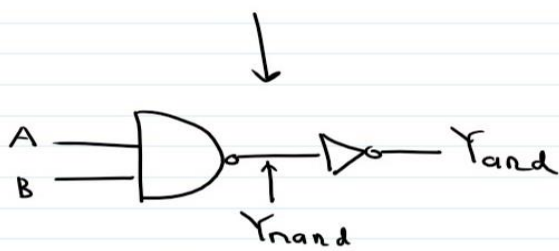
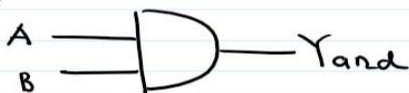


$$f_A = \frac{1}{2} \cdot f_B$$

$$f_A = \frac{1}{2} f_B$$

\* 2 i/p AND, 2 i/p OR Gate:-

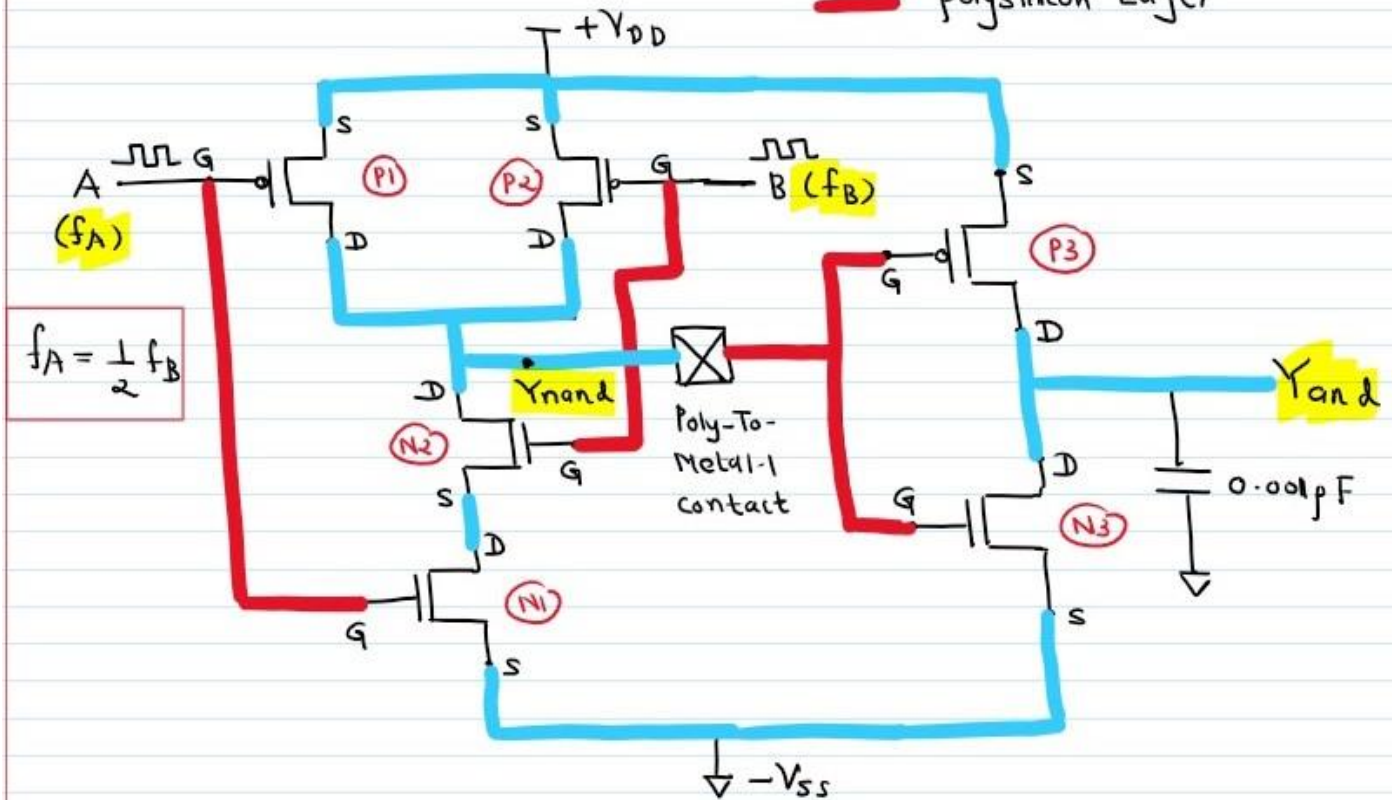
Symbols:-



⊛ MOSFET-Level Schematics for 2 i/p AND, 2 i/p OR Gate :-

⊛ 2 i/p AND Gate :-

— Meta-1 Layer  
— polysilicon Layer



⊛ 2 i/p OR Gate :-

