P8_12-10-21

12 October 2021 08:52

⊛ Assignments :-

① B.1.c :- Transmission Gate (TG)

② B.2 :- 2:1 MUX using TG

⊛ B.1.c :- Transmission Gate (TG)

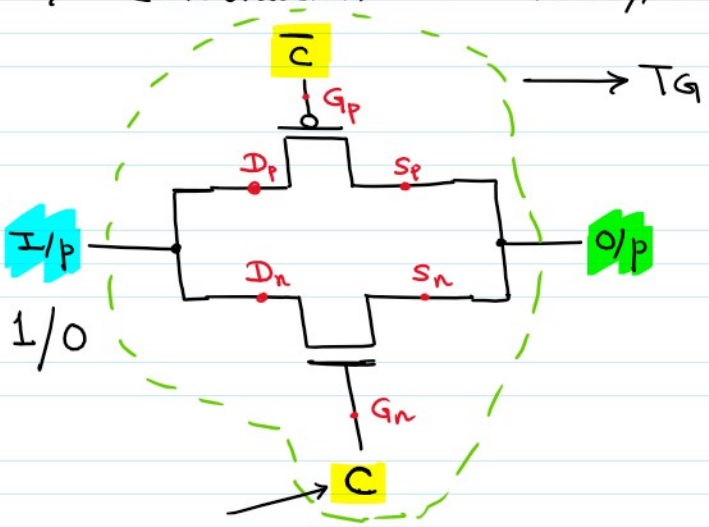
⇒ TG is one of the four CMOS - Logic sub-families

⇒ TG is a **CMOS switch**; ie:- a semiconductor S/ω built by combining 1 PMOS & 1 NMOS S/ω

⇒ TG = (1 PMOS) // (1 NMOS)

⇒ Being a combination of PMOS & NMOS; it gives both S1, S0 @ o/p

⇒ Construction :- → PMOS // NMOS



For I/p = 1

ⓐ If pmos = ON, nmos = OFF } o/p = S1 ✓

ⓑ If pmos = OFF, nmos = ON } o/p = W1 ✗

For I/p = 0

ⓐ If pmos = ON, nmos = OFF } o/p = W0 ✗

ⓑ If pmos = OFF, nmos = ON } o/p = S0 ✓

Thus; to get STRONG o/p ; irrespective of the value of I/p; we simultaneously S/ω ON, both pmos & nmos

∵ pmos = ON, for Gate = 0

nmos = ON, for Gate = 1

We give opposite values of Trigger to pmos & nmos

⇒ The **Control Signal for TG**, denoted as **"C"** is applied to **NMOS**

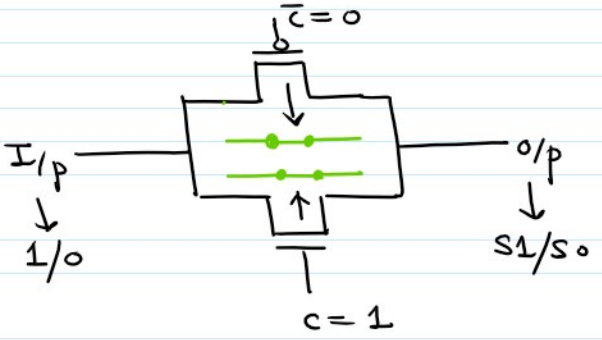
⇒ The **complement of "C"** ie. **$\bar{C}$** is applied to **PMOS**

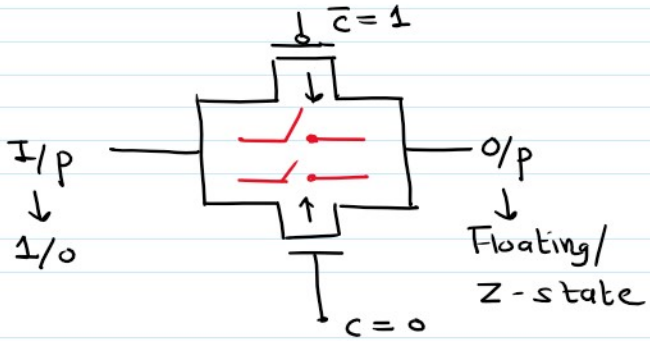
⇒ Operation of TG can be summarised as follows:-

⇒ Operation of TG can be summarised as follows:-

For $c = 1$ ($\bar{c} = 0$) → nmos = ON, pmos = ON

For $c = 0$ ($\bar{c} = 1$) → nmos = OFF, pmos = OFF

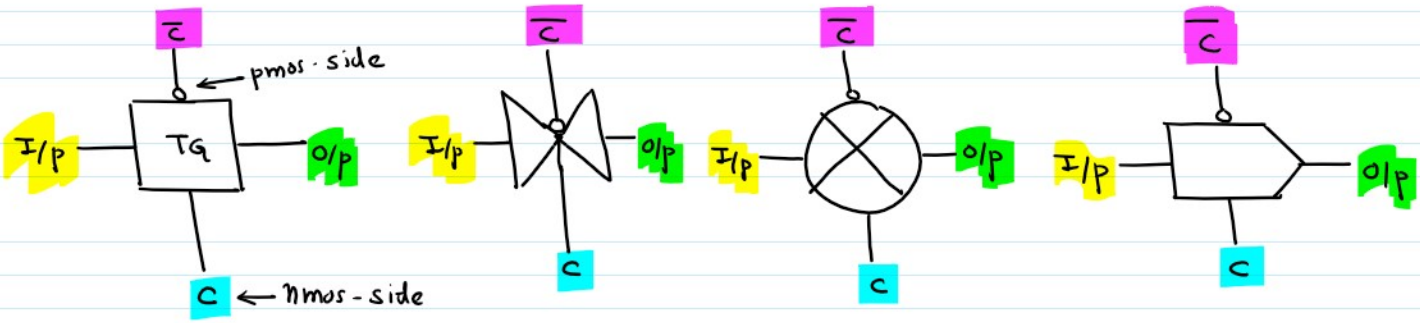




⇒ Thus; TG closes for $c = 1$ (NMOS side)

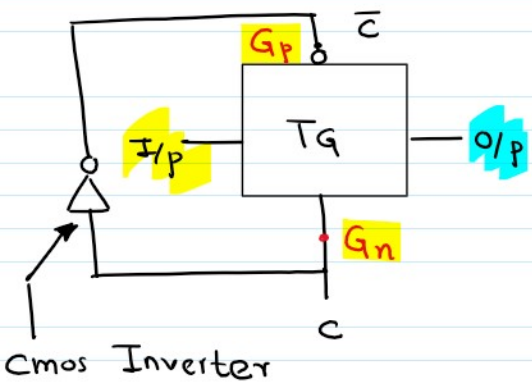
TG opens for $c = 0$ (NMOS side)

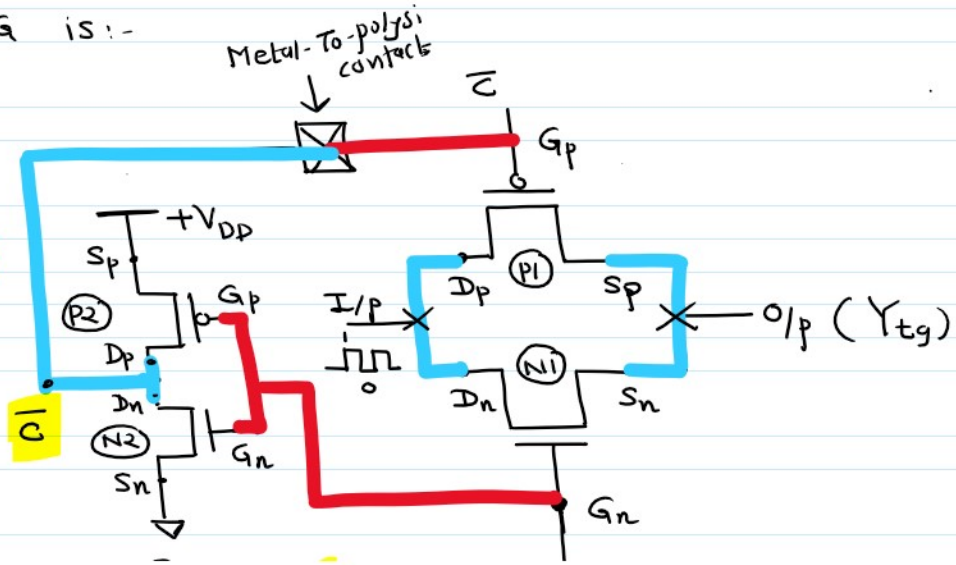
⇒ Symbols:- TG has multiple Representations as follows:-



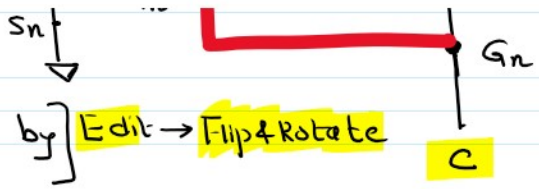
⇒ MOSFET-level Schematic of TG:-

The symbol for TG is:-





CMOS Inverter



⊛ Flip-Horizontal the CMOS-Invtr by after making it] Edit → Flip & Rotate

⇒ To check functionality of TG :-

① Apply 2.5 GHz Clock @ I/p

② For clock = 1 ; we should get o/p = $+V_{DD} = 1.2V$ (S1)

③ For clock = 0 ; we should get o/p = $-V_{SS} = 0V$ (S0)

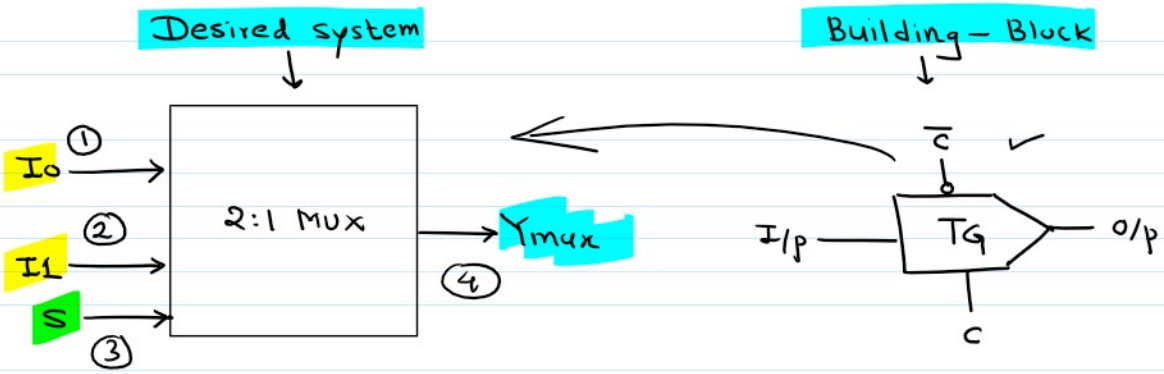
⊛ Refer to the YouTube channel video for Demo of TG-Layout

⊛ B.2 :- 2:1 MUX

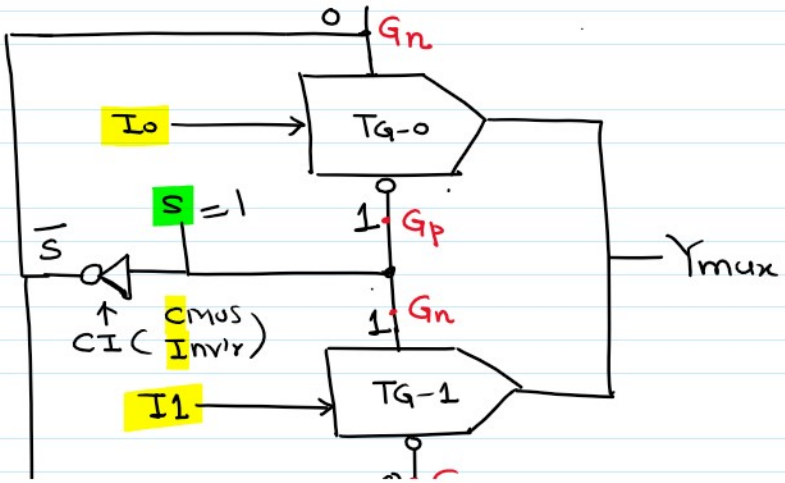
⇒ For Implementing N:1 Mux using TG-Logic

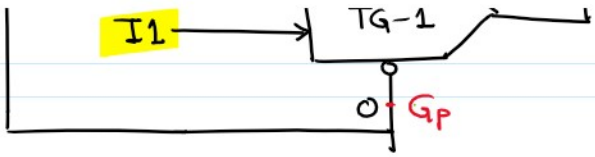
⇒ As Many I/p's of Mux, Those many TG's

⇒ ∵ We have 2:1 Mux; We need 2 TG's ie. TG-0, TG-1

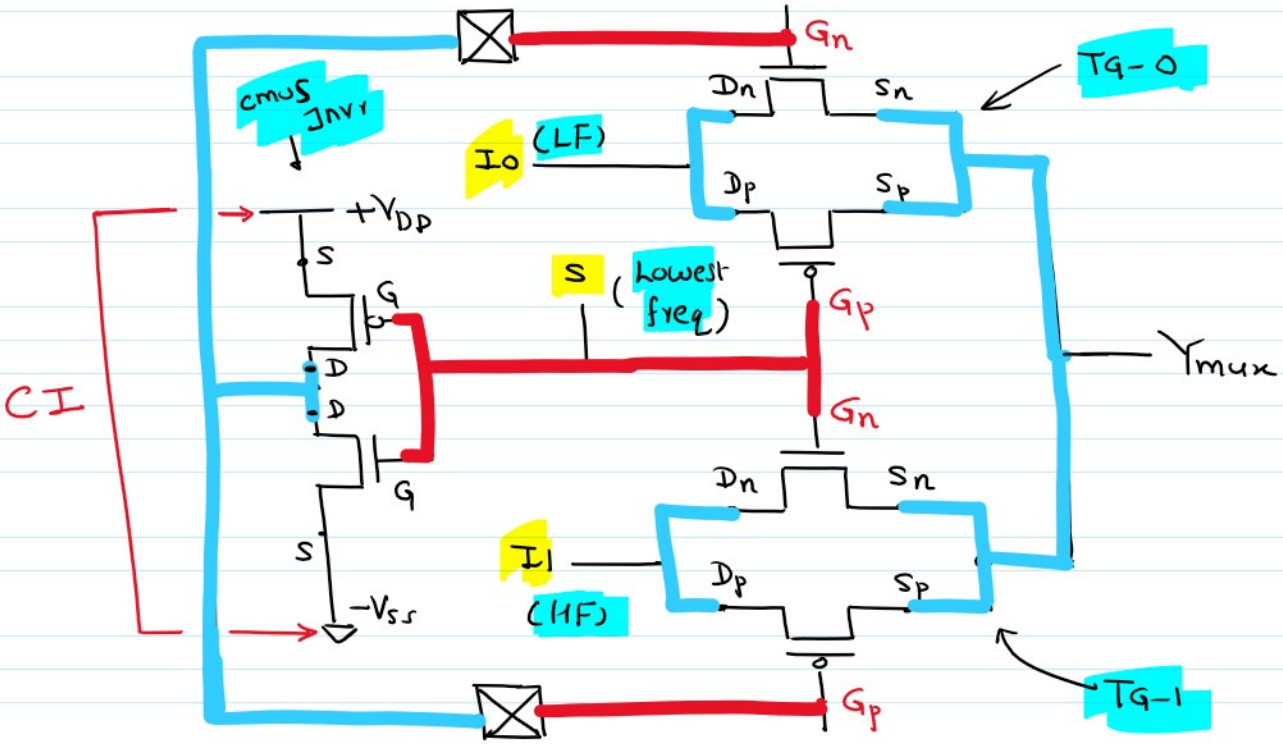


⊛ Block-Schematic of 2:1 Mux using TG's :-





✳ MOSFET-level Schematic of 2:1 Mux using TG's :-



✳ Refer to the YouTube channel video for Demo of 2:1 MUX. Layout