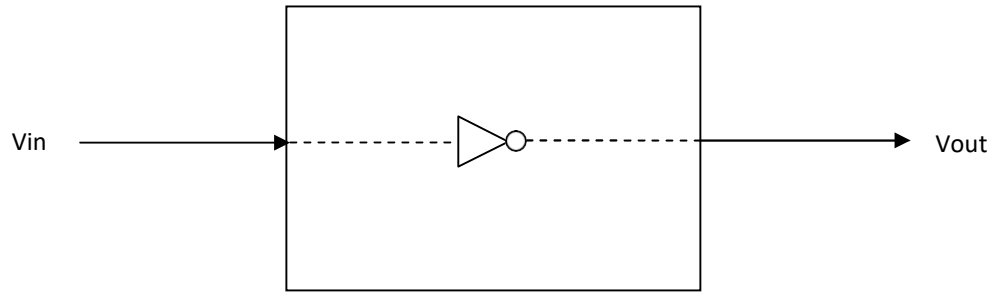
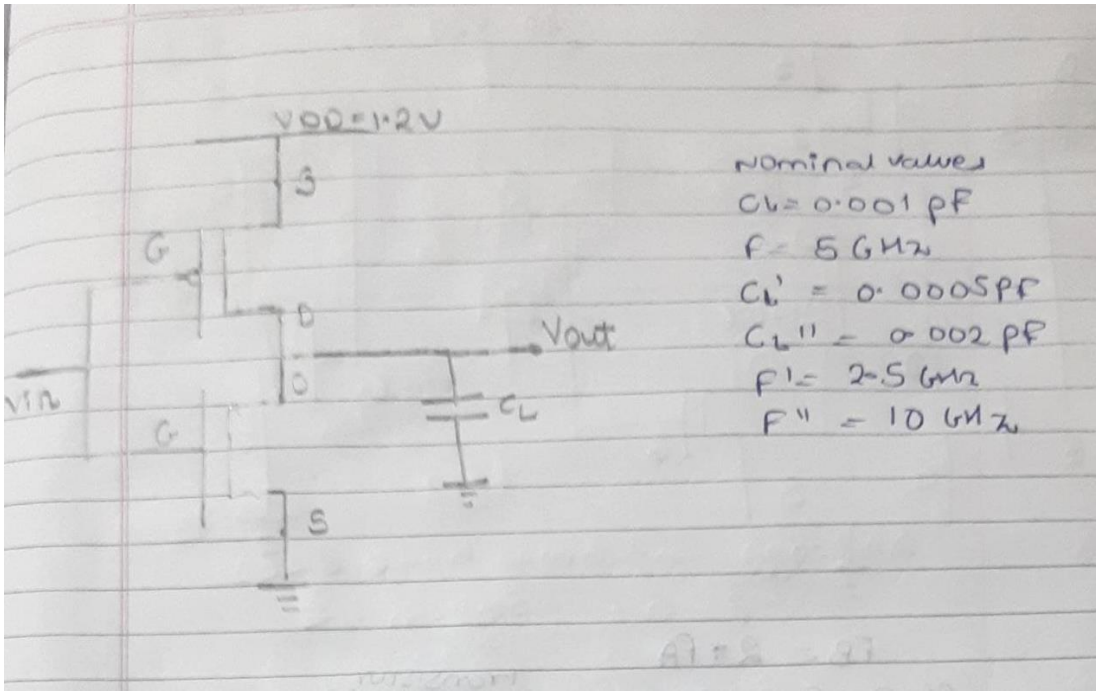
Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	B.1.a
Assignment Name	:	CMOS INVERTER & Dynamic Power Dissipation Analyses
Date Of Performance	:	

SYMBOL:-



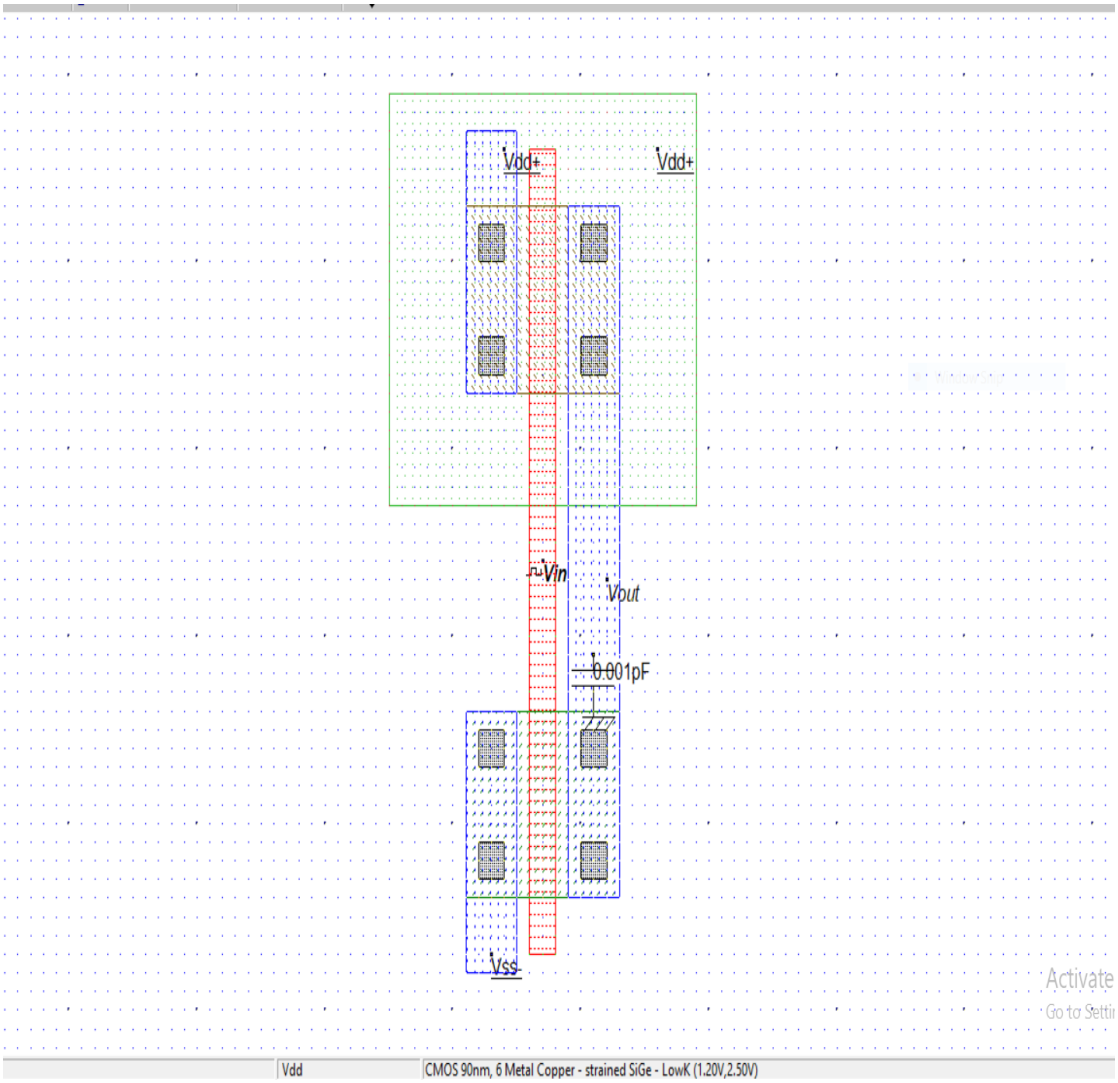
$Vout = \overline{Vin}$



Truth Table:-

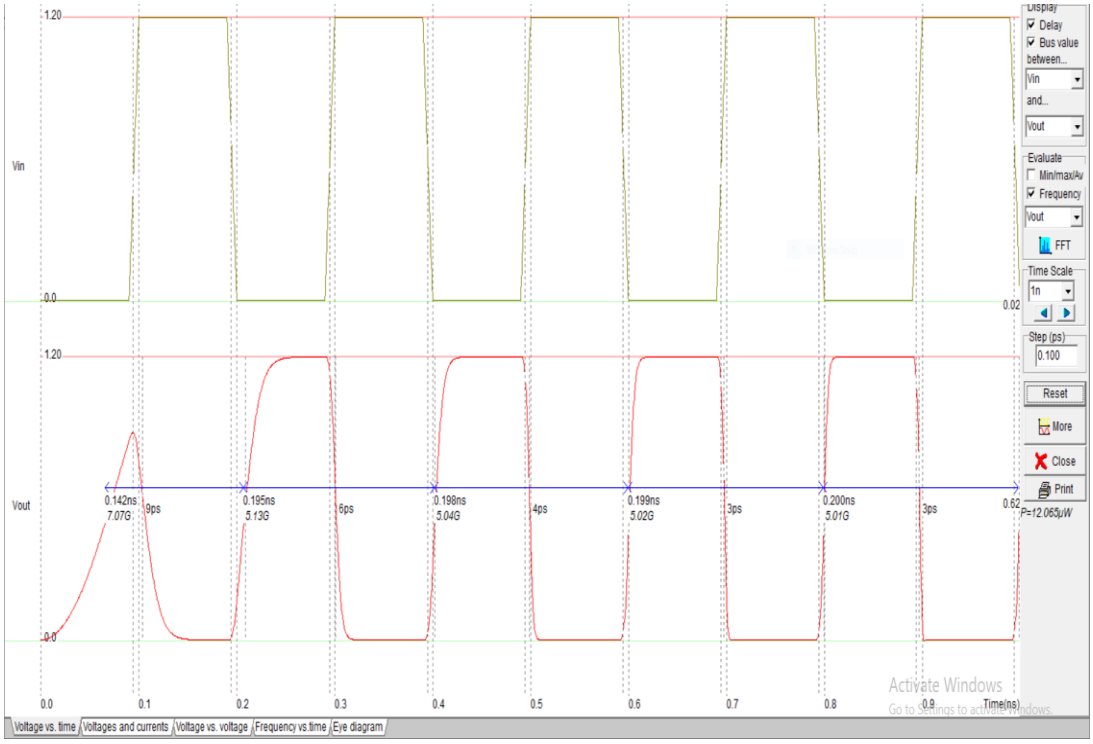
Vin	Vout
0	Strong-1 (1.2 V)
1	Strong-0 (0 V)

Layout for 90 nm Foundry : (V_{dd} = 1.2 V)

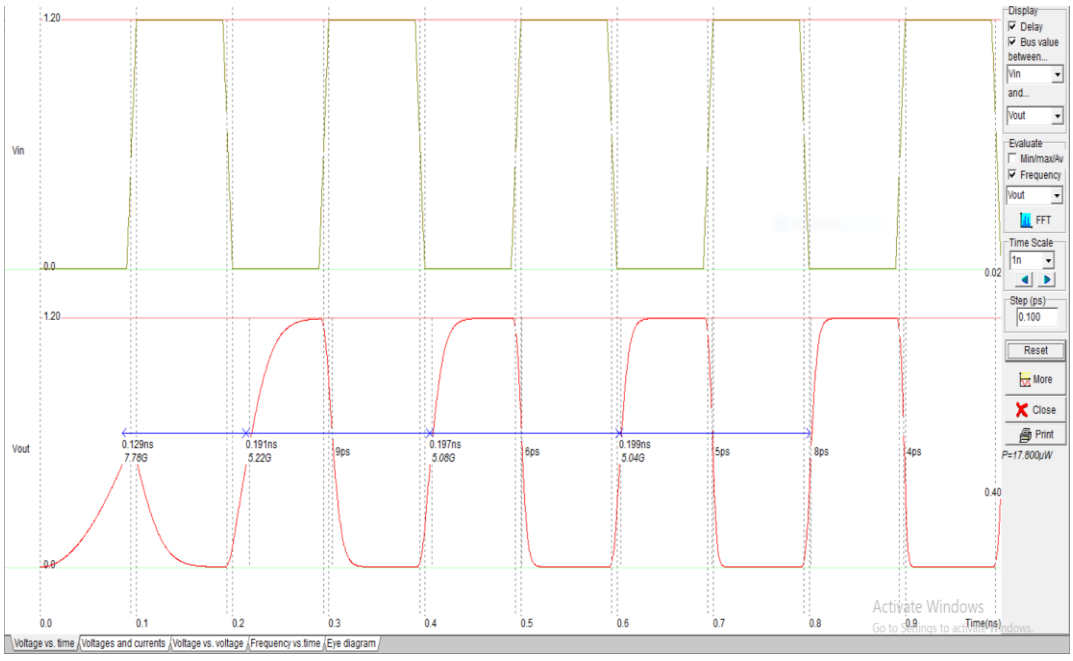


Waveforms:

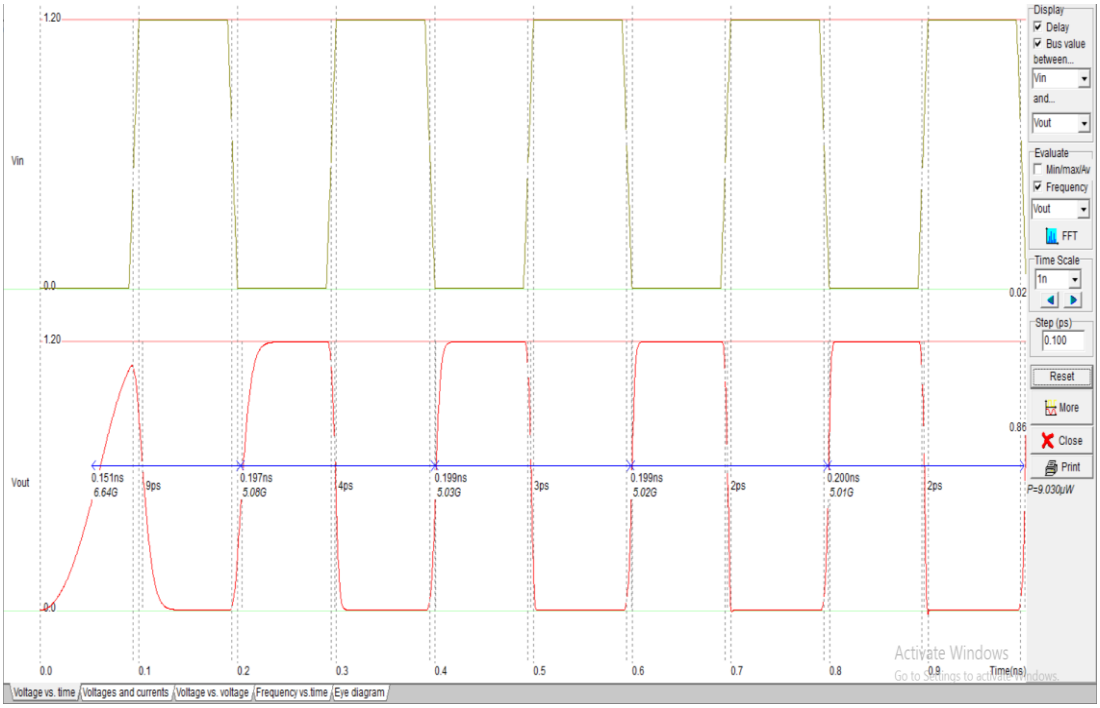
1) C_L=0.001pF , f_{clk}=5 GHz



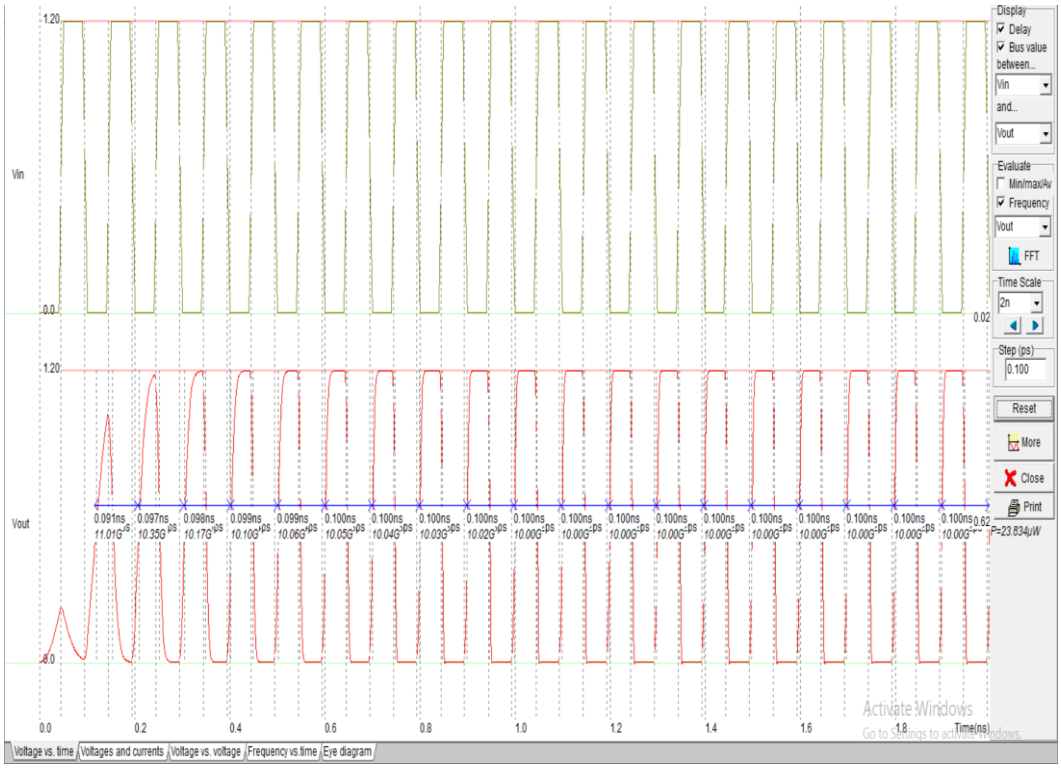
2) C_L=0.002pF , f_{clk}=5 GHz



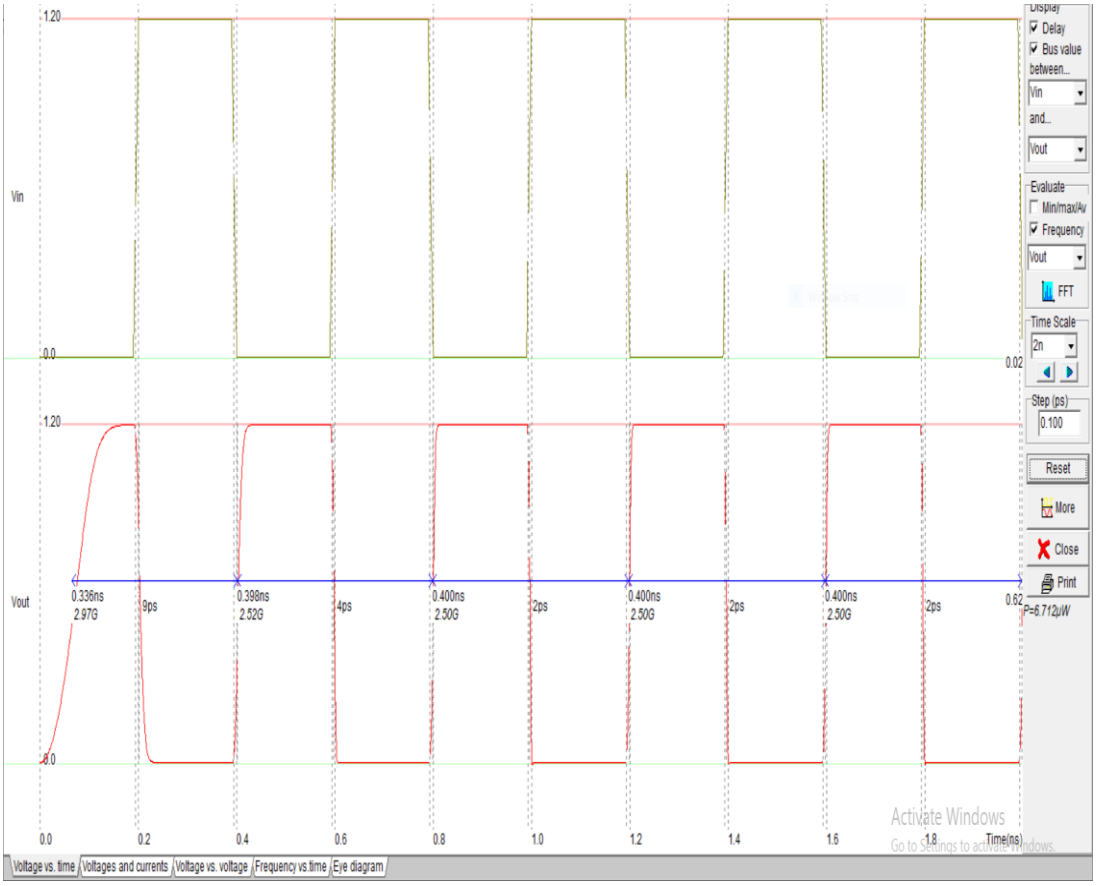
3) C_L=0.0005pF , f_{clk}=5 GHz



4) C_L=0.001pF , f_{clk}=10 GHz



5) C_L=0.001pF , f_{clk}=2.5 GHz



DYNAMIC POWER DISSIPATION ANALYSES

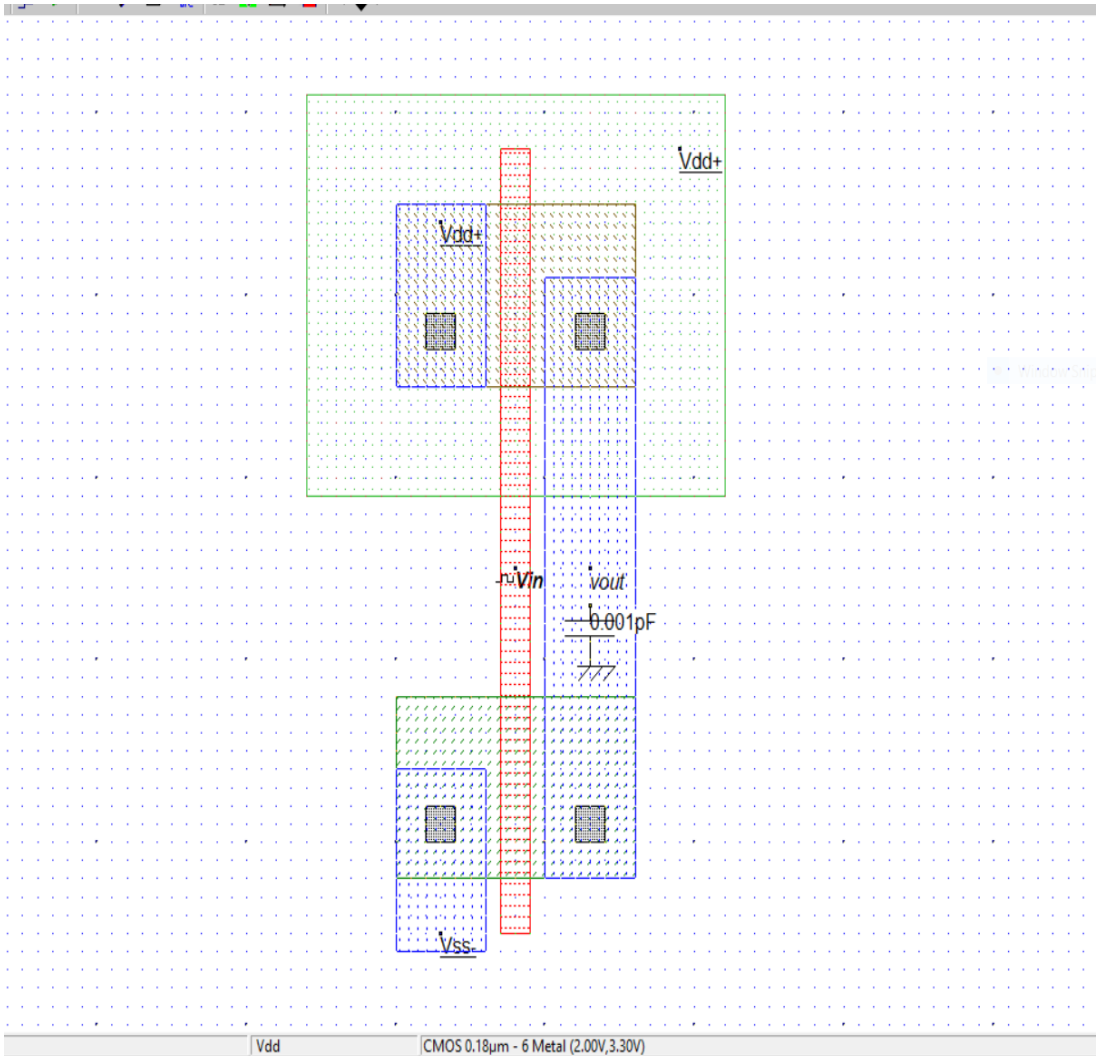
(I) Effect of change in C_L :

SR.NO.	C_L (pF)	P_{dyn} (µW)
1)	0.001	
2)	0.002	
3)	0.0005	

(II) Effect of change in f_{clk} :

SR.NO.	f_{clk} (GHz)	P_{dyn} (µW)
1)	5	
2)	2.5	
3)	10	

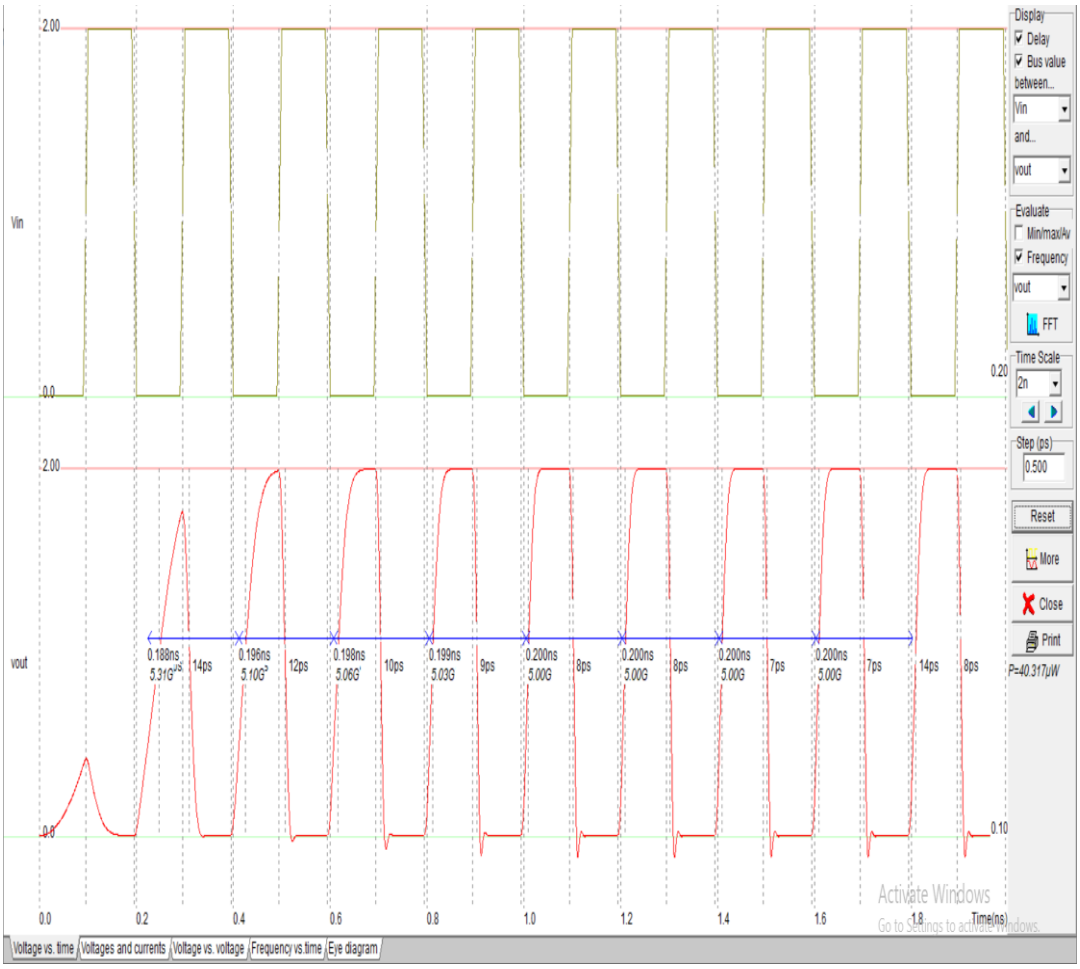
Layout for 180nm foundry : (V_{dd} = 2 V)



Set CLOCK parameters as :
Time low = Time High = 0.090 nS
Rise Time = Fall Time = 0.01 nS

Waveforms:-

C_L=0.001pF , f_{clk}= 5 GHz , V_{dd} = 2 V (180 nm Foundry)



DYNAMIC POWER DISSIPATION ANALYSES

V_{dd} (V)	P_{dyn} (µW)
1.2 (90 nm)	
2 (180 nm)	

Conclusions:-

1) Drawn the LAYOUT for CMOS Inverter using 90 nm & 180 nm Foundry.
2) Simulated LAYOUT to observe w/f's & verified functionality.
3) Being a **Pure-CMOS System** (PMOS // NMOS & CMOS INVERTER) , it gives both **S-1** & **S-0** as O/P.
4) Appreciated the validity of the mathematical model
   $P_{dynamic} = C_L * (Vdd)^2 * f_{clk}$
5) Found a reduction in $P_{dynamic}$ by using a better Foundry i.e., **90 nm** instead of **180 nm**
6) Learnt that the presence of spikes in O / P waveform at Switching instants indicate the inabilityof the MOSFETs to switch at GHz frequencies.