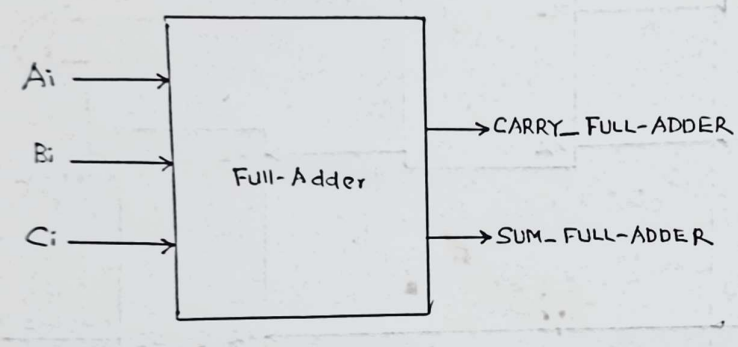
Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	B.2.b
Assignment Name	:	FULL-ADDER (Using HALF-ADDER & OR-GATE)
Date Of Performance	:	

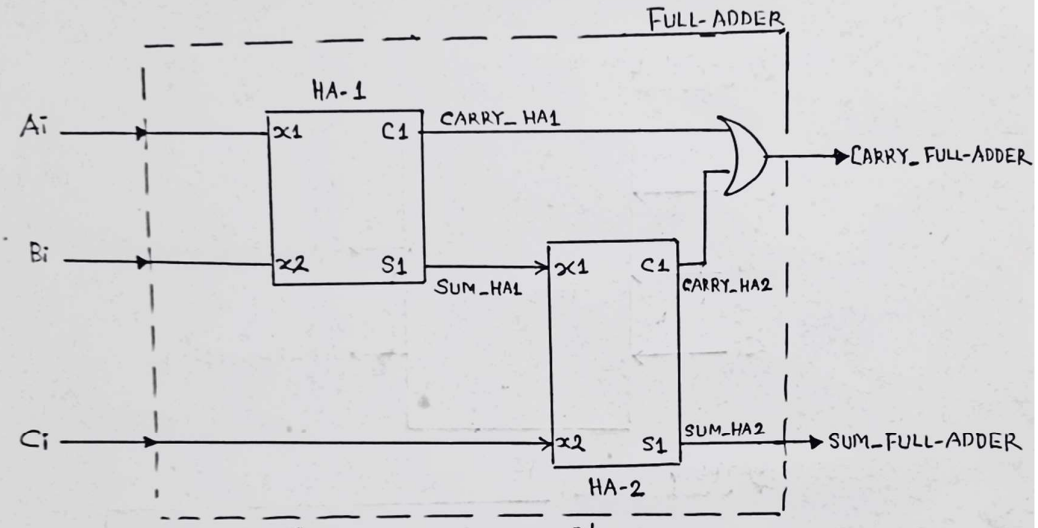
Block Diagram:- Kindly Note that 1 & 0 in O/P are STRONG Values only

⊛ SYMBOL :-



⊛ TRUTH-TABLE :-

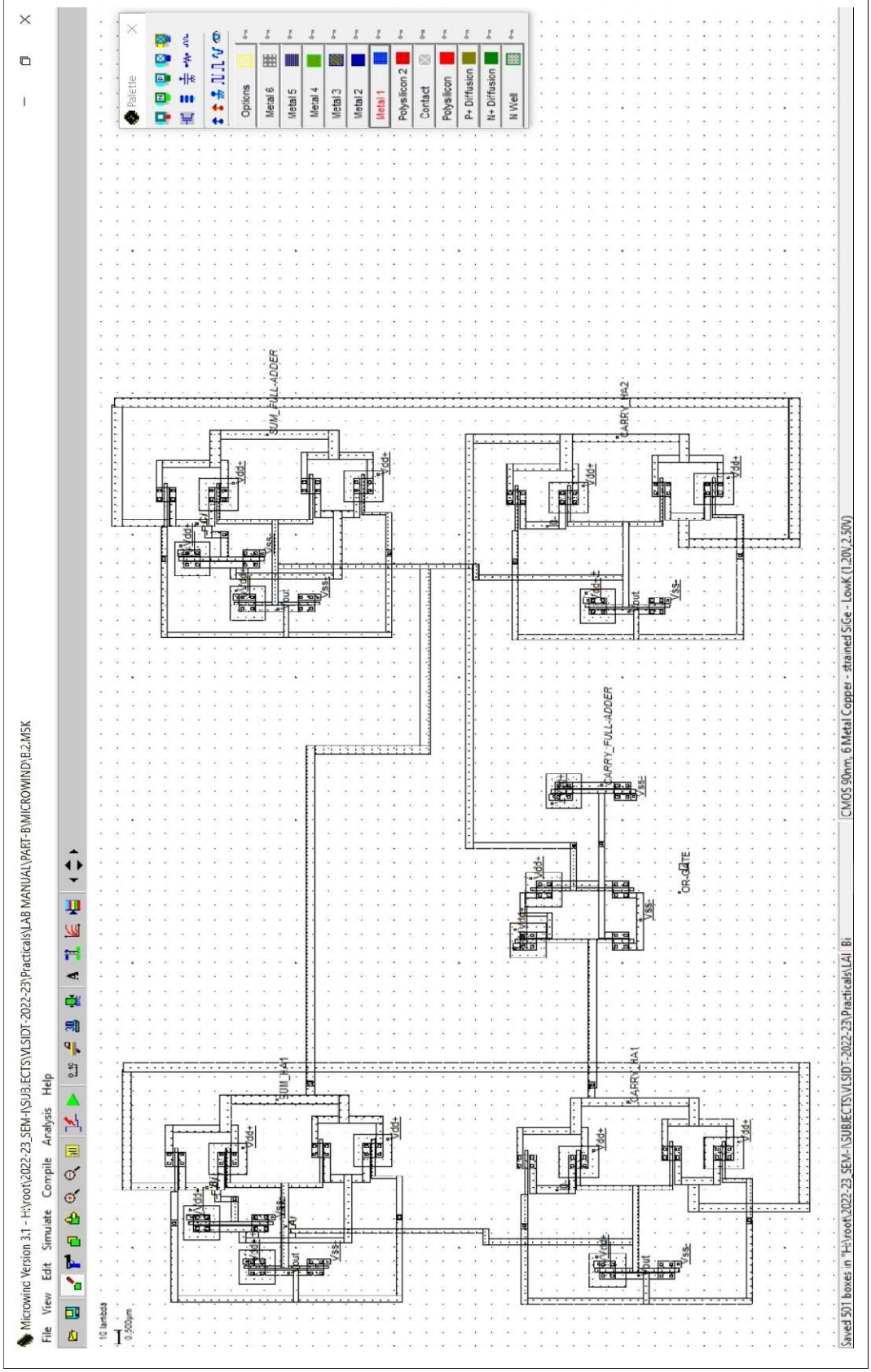
Ai	Bi	Ci	CARRY_FA	SUM_FA
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



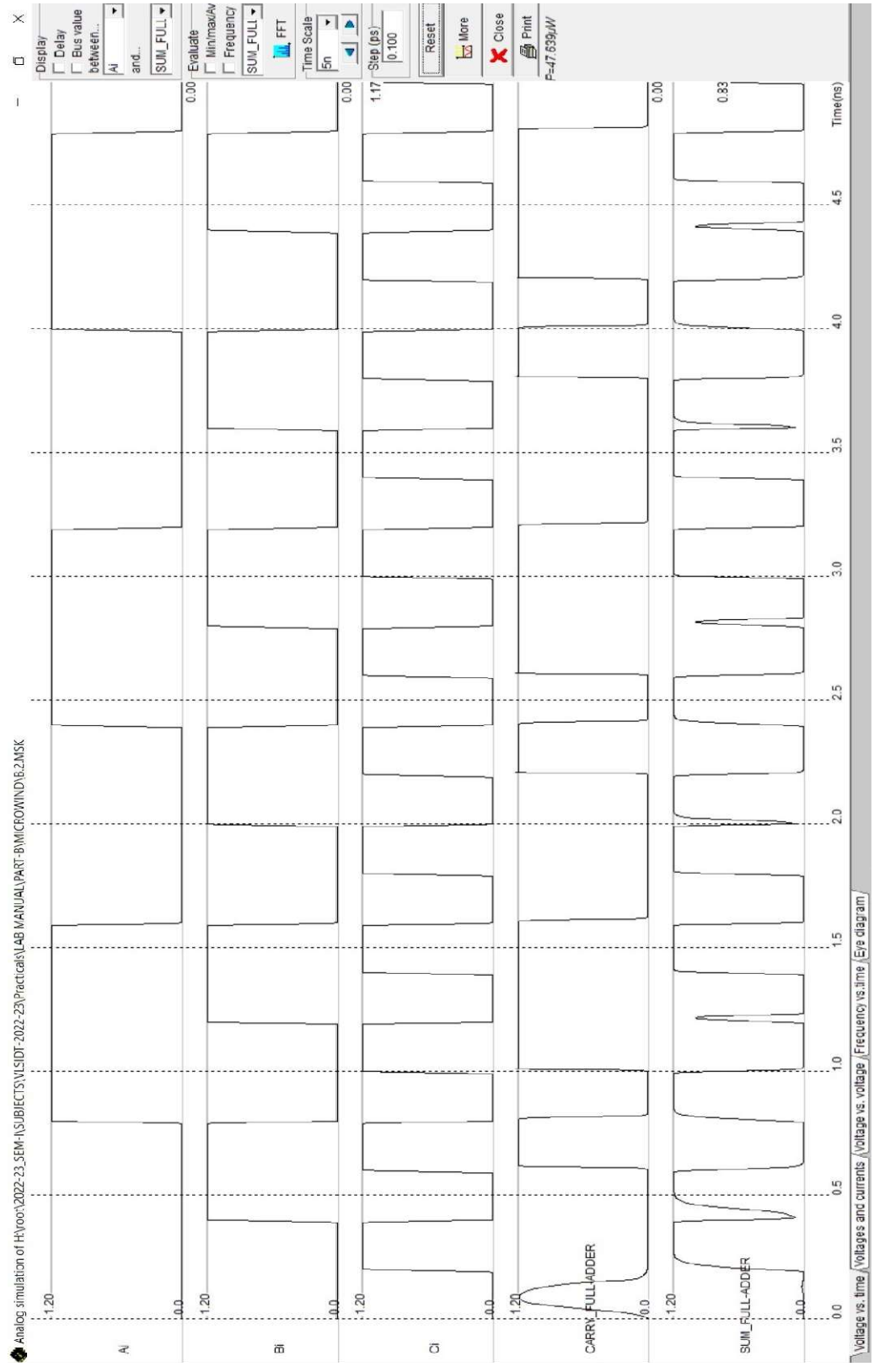
HA-1 = 1st Half-Adder , HA-2 = 2nd Half-Adder
x1, x2 = Inputs of Half-Adder
C1 = Carry o/p of Half-Adder
S1 = Sum o/p of Half-Adder

Map the Signals shown above to the Layout shown below

Layout (90 nm Foundry) : (V_{dd} = 1.2 V)



Waveform:


Analog simulation of H:\roo\2022-23_SEM-I\SUBJECTS\VLSIDT 2022-23\Practicals\LAB MANUAL\PART-B\MICROWIND\6.2.MSK
Display
Delay
Bus value between...
Ai
and...
SUM_FULL_
Evaluate
Min/max/Av
Frequency
SUM_FULL_
FFT
Time Scale
5n
Step (ps)
0.100
Reset
More
Close
Print
P=47.639uW
Ai
Bi
Ci
CARRY_FULLADDER
SUM_FULL-ADDER
1.20
0.0
0.00
1.17
0.83
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
Time(ns)
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram

Conclusion:-

1) Drawn the LAYOUT for CMOS FULL-ADDER using 90 nm Foundry.
2) Full-Adder is Implemented Using “Two HALF-ADDERS “ & “One 2 i/p OR Gate”.
3) Half-Adder is Implemented Using “TWO 2:1 Multiplexers configured as EX-OR Gate & AND Gate.
4) 2:1 Multiplexer , in turn is implemented using Transmission Gate , a Pure CMOS System.
5) Being a **Pure-CMOS System**, it gives both **S-1** & **S-0** as O/P.
6) Frequency Relationships for I/P’s are : $f_{Ai} = (f_{Bi} / 2) = (f_{Ci} / 4)$
7) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.