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SPPU Part-B Assignment : 3 (1-bit SRAM cell)

⇒ 1-bit Memory

⇒ It can store 1-bit of data (1/0) using SRAM Technology

⇒ SRAM = Static RAM

⇒ Circuit Diagram:-

① 2 NMOS X'stors (N1, N2) (Act as S/W's)

② 2 Cross-coupled CMOS NOT Gates (I1, I2)

O/p of 1st → given as i/p of 2nd →

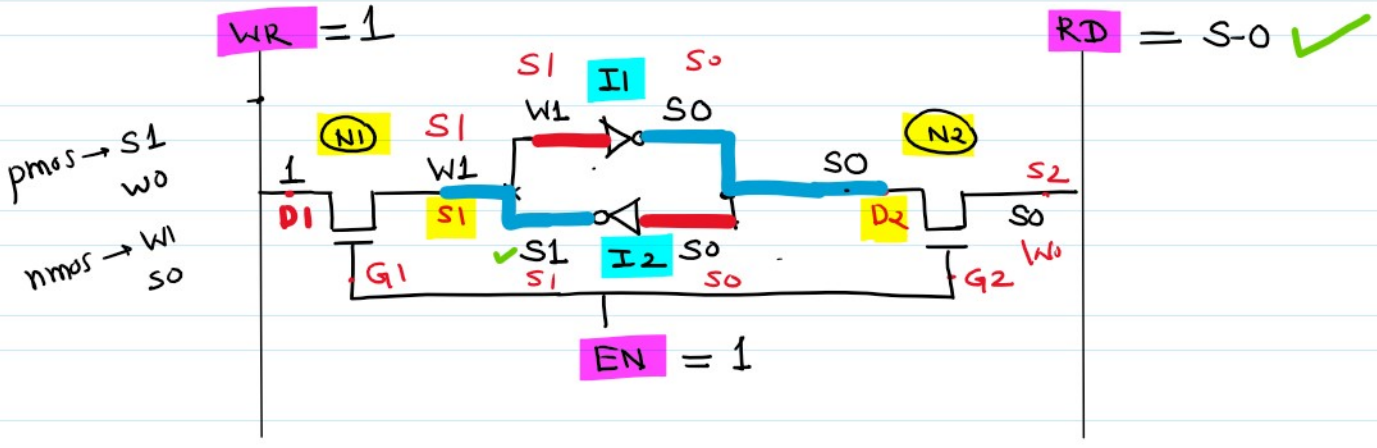
O/p of 2nd → given as i/p of 1st →

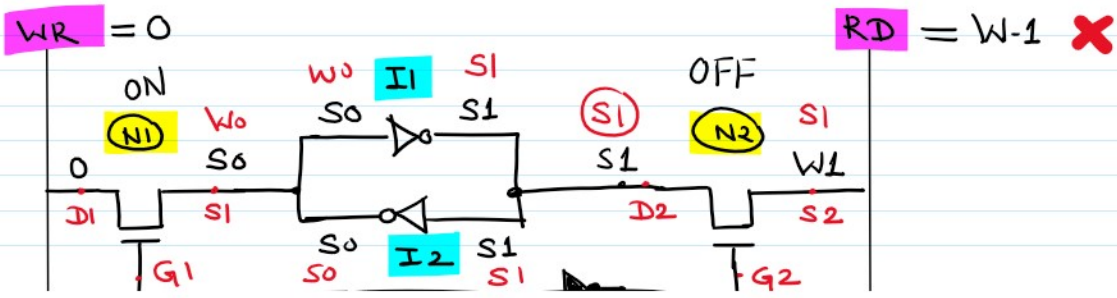
③ WRITE Line (To write Data) : WR

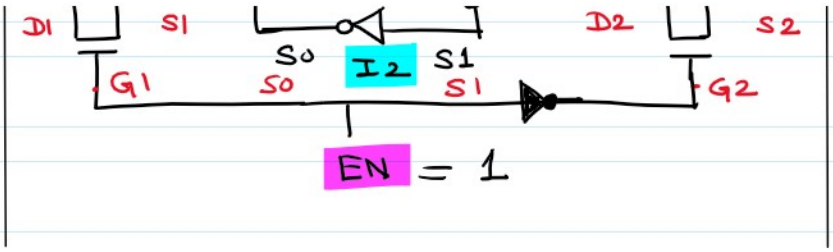
④ READ Line (To read Data) : RD

⑤ ENABLE : EN

⊛ 3.a (Using NMOS S/W)







⊛ The above circuit stores 1-bit of data, with foll. facts :-

⇒ It stores Logic-0 as Weak-1 (✗ Acceptable)

⇒ It stores Logic-1 as Strong-0 (✓ Acceptable)

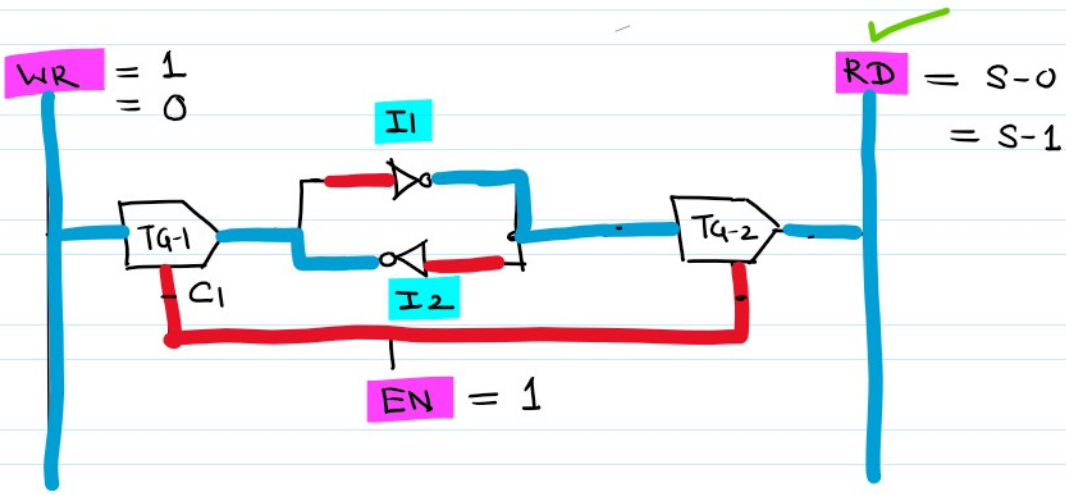
→ This is because '1' is passed through (N2) (NMOS S/W)

⊛ If we Replace (N1, N2) with PMOS S/W's (P1, P2)
we will get Strong-1, but a Weak-0

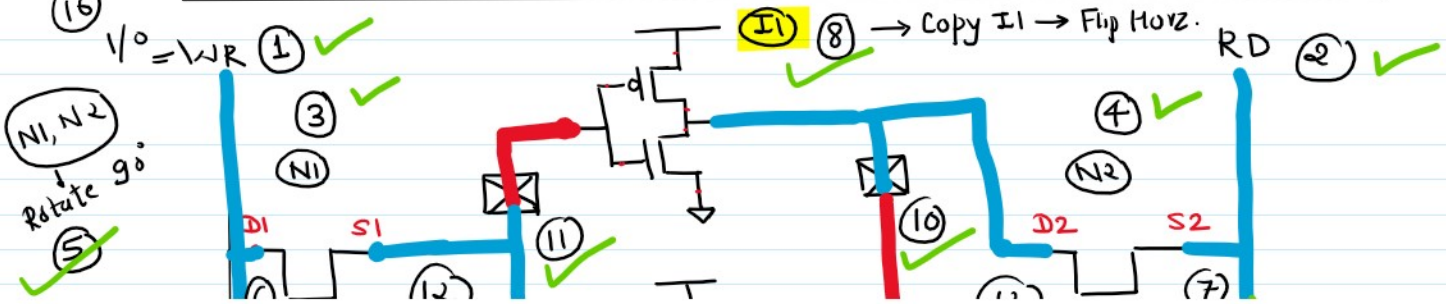
⊛ If we use dual combination (N1, P1) OR (P1, N1)
we will face mixture of above drawbacks

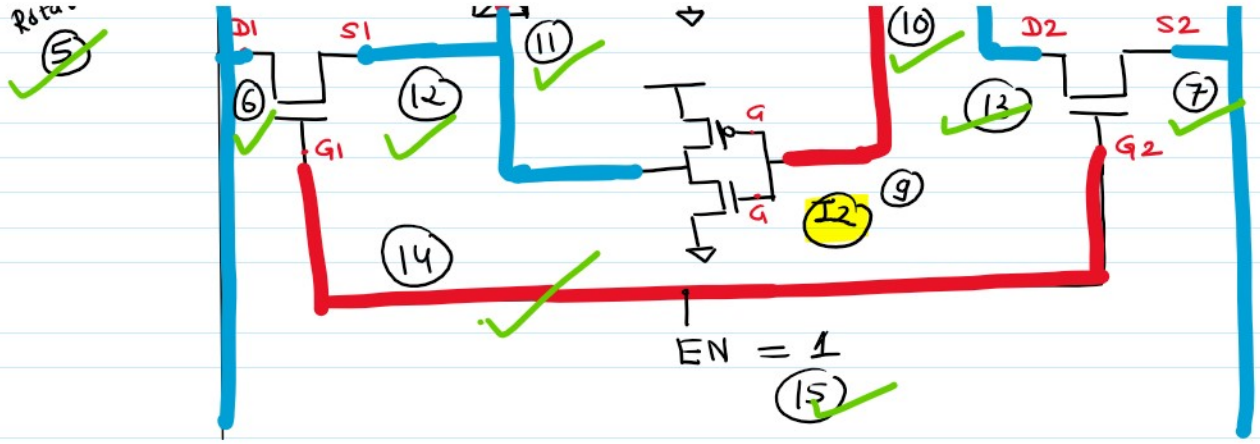
⇒ Solution is to use CMOS S/W's (TG) in place of (N1, N2)

3.b : (Using TG S/W)



⊛ MOSFET- Level Schematic of 1-bit SRAM cell (NMOS S/W) :



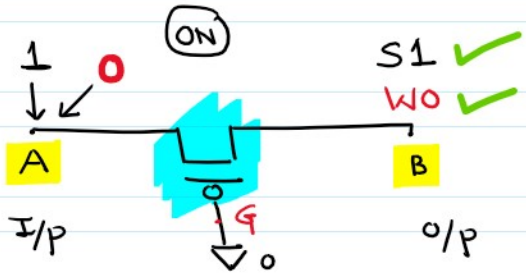


- I/ps are always STRONG (PURE) (S1/S0)
- O/ps can be STRONG/WEAK
- O/ps must be STRONG

1 → S1 / W1

0 → S0 / W0

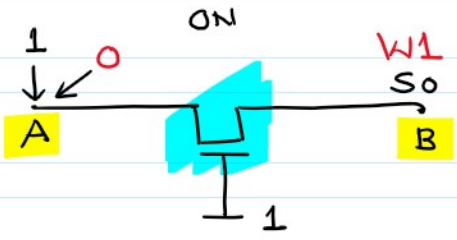
I/p's can never be weak, always strong



PMOS → S1 / W0

CMOS → PMOS + NMOS

W1	S0
W0	S1
S1	S0
S0	S1



NMOS → W1 / S0

I1, I2 ⇒ CMOS Inv'r

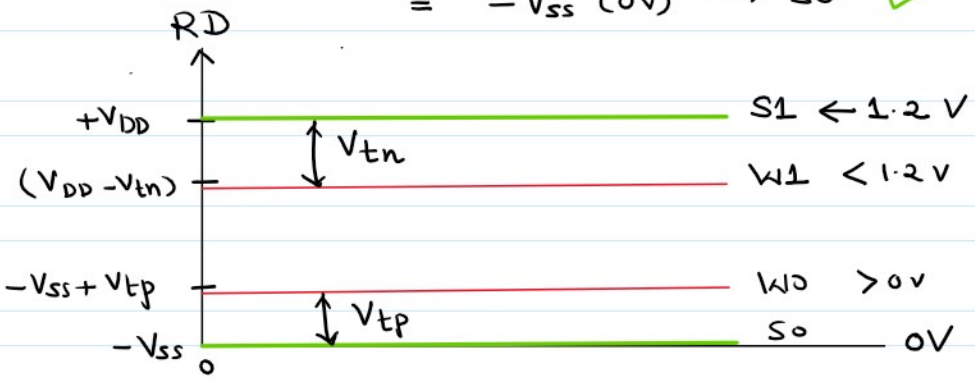
I1, I2 ⇒ cmos Jnv'r
(pmos, nmos)

Value of signal = $+V_{DD}$ ⟶ S1 ✓

= $(V_{DD} - V_{tn})$ ⟶ W1 ✗

= $(-V_{ss} + V_{tp})$ ⟶ W0 ✗

= $-V_{ss}$ (0V) ⟶ S0 ✓



For 90nm Tech; ∴ $V_{DD} = +1.2V$