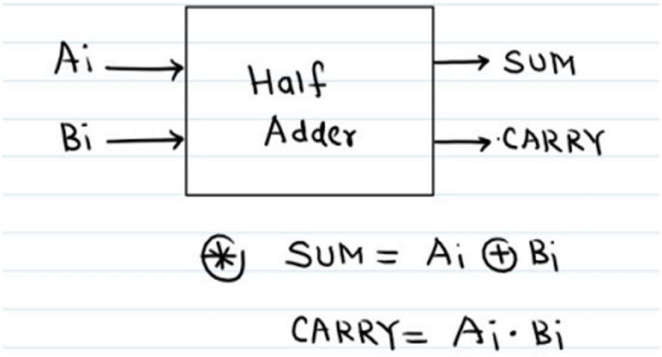
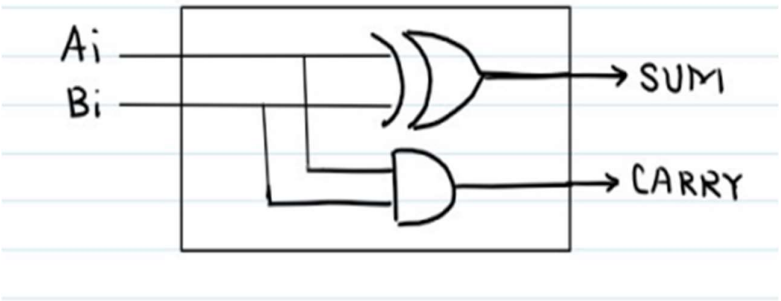
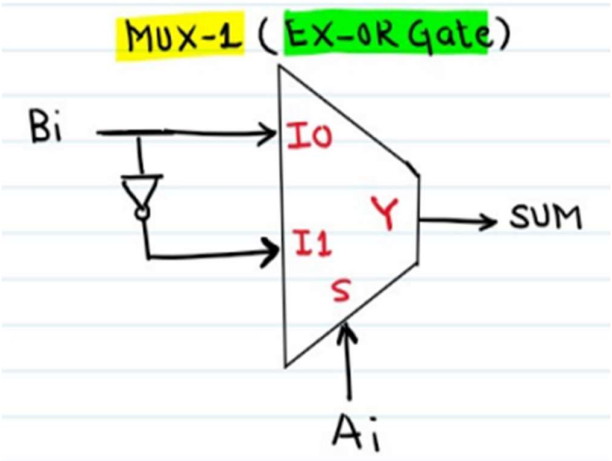
Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	B.2.a
Assignment Name	:	CMOS HALF-ADDER
Date Of Performance	:	

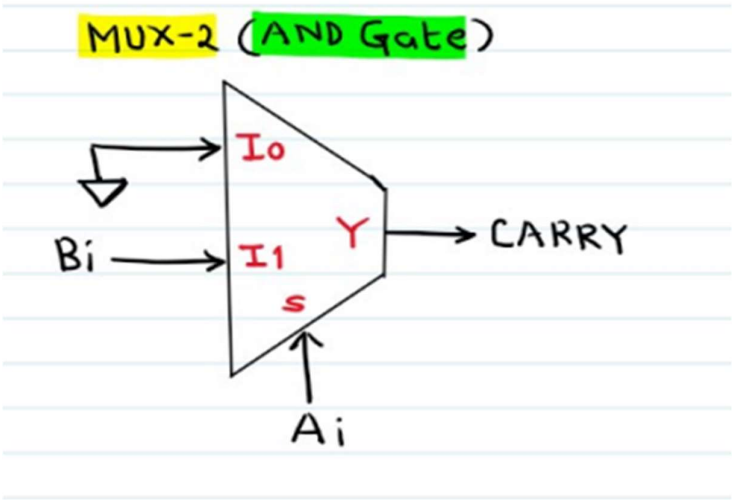
Block Diagram:-

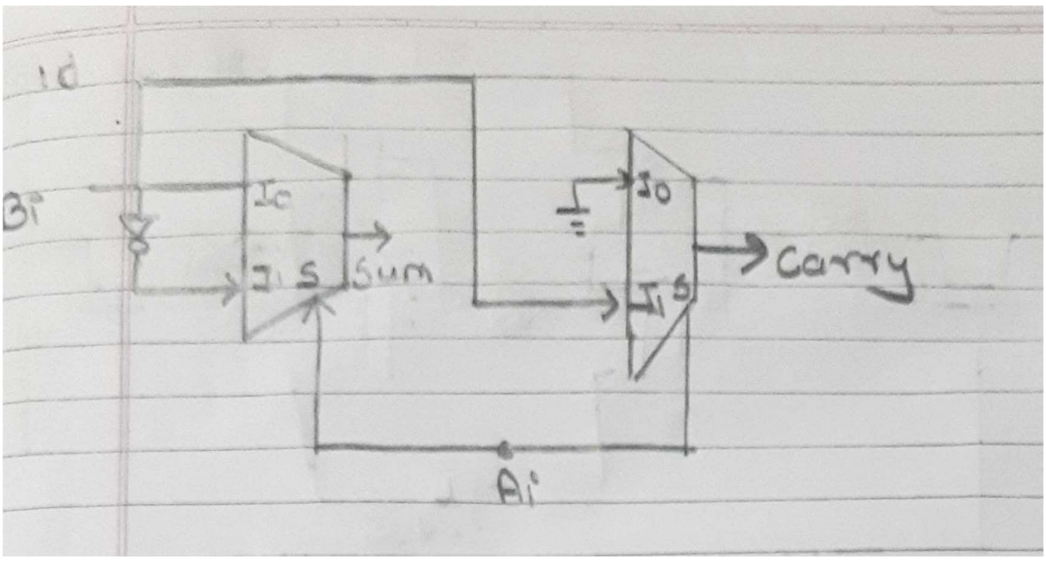


Gate-Level Schematic:-






MUX-2 (AND Gate)
Io
Bi
I1
Y
CARRY
S
Ai


Bi
Io
I1
S
Sum
Io
I1
S
Carry
Ai

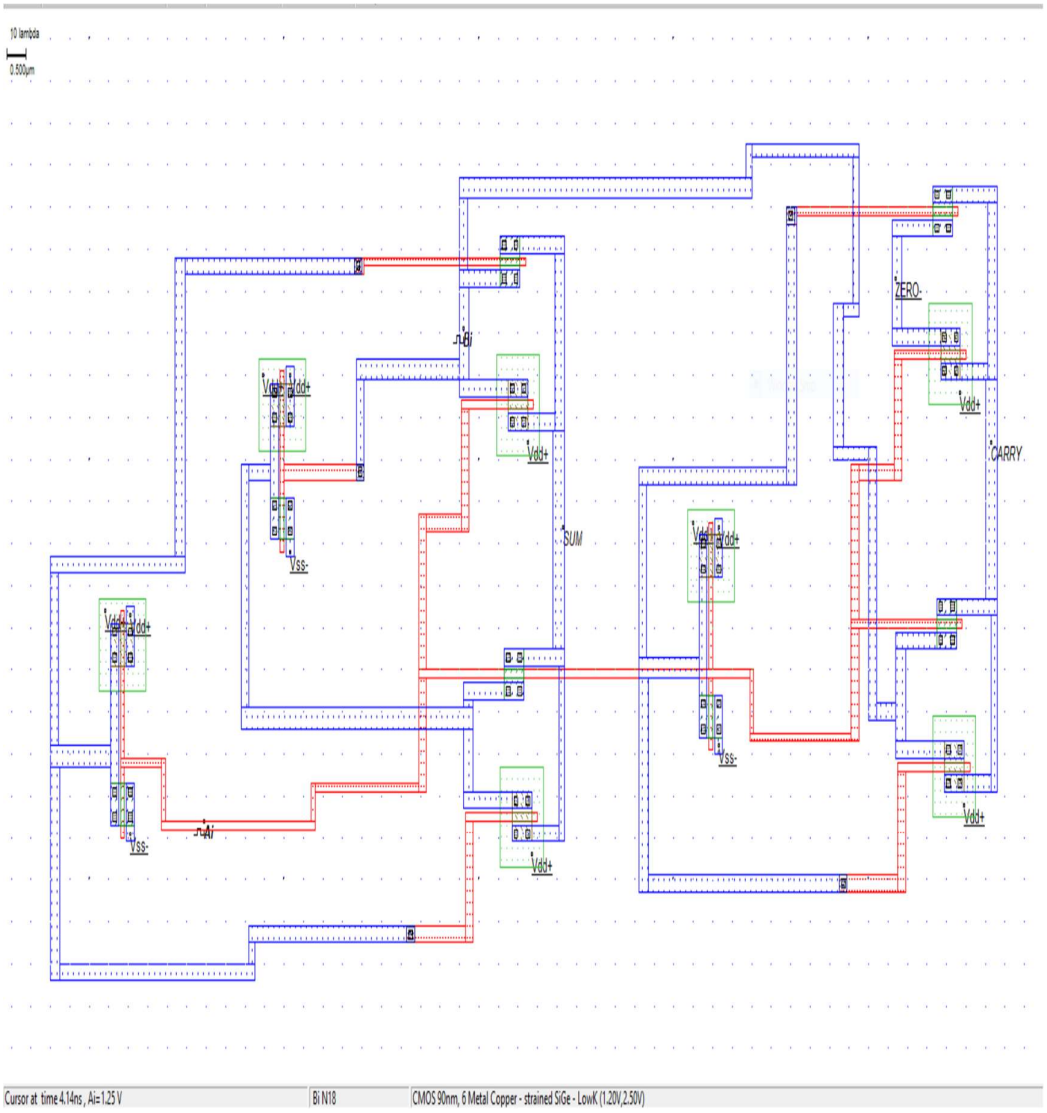
Truth Table:-

I/P's are ALWAYS STRONG

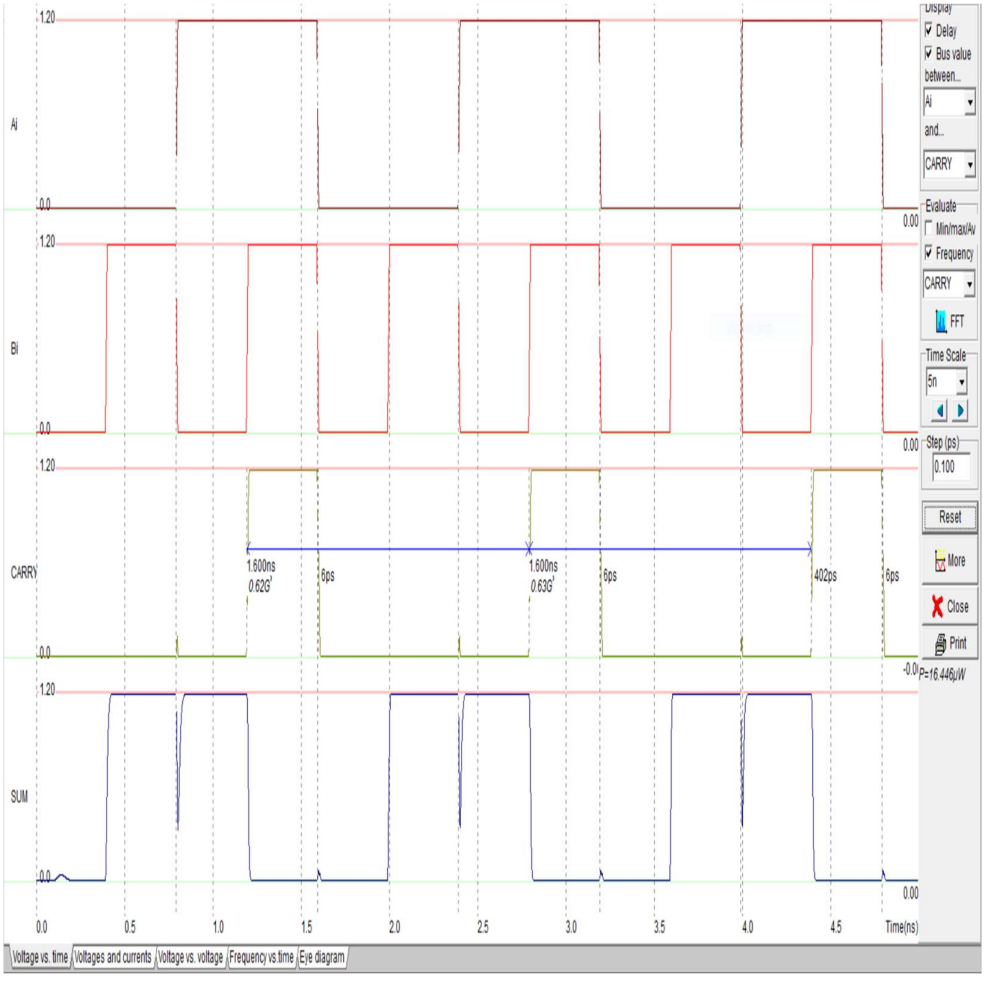
O/P :: S-1 = STRONG -1 , S-0 = STRONG - 0

Ai	Bi	SUM	CARRY
0	0	S-0	S-0
0	1	S-1	S-0
1	0	S-1	S-0
1	1	S-0	S-1

Layout (90 nm Foundry) : (V_{dd} = 1.2 V)



Waveform:


Ai
Bi
CARRY
SUM
1.20
0.0
1.600ns
0.62G
6ps
1.600ns
0.63G
6ps
402ps
6ps
Display
Delay
Bus value between...
Ai
and...
CARRY
Evaluate
Min/max/Av
Frequency
CARRY
FFT
Time Scale
5n
Step (ps)
0.100
Reset
More
Close
Print
P=16.446uW
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
Time(ns)
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram

Conclusion:-

1) Drawn the LAYOUT for CMOS HALF-ADDER using 90 nm Foundry.
2) MOSFET Count for HALF-ADDER using Conventional CMOS Logic would be 28 MOSFETs (22 for EX-OR Gate + 6 for OR Gate)
3) Using the TG → MUX , MUX → LOGIC-GATE Approach , we reduced the MOSFET count to just 14 MOSFETs as seen in the LAYOUT.
4) Kept Frequency of 1^{st} i/p (Ai) half that of frequency of 2^{nd} i/p (Bi).
5) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.
6) Being a **Pure-CMOS System** (PMOS // NMOS & CMOS INVERTER) , it gives both **S-1** & **S-0** as O/P.