

## AGENDA

COMMENCEMENT OF PART-B :

- 1) LIST OF ASSIGNMENTS
- 2) ORDER of Conduction
- 3) INSTALLATION of MICROWIND Tool
- 4) INSTALLATION of DSCH Tool
- 5) Know GUI OF MICROWIND
- 6) LAYOUT & Simulation of CMOS system :
  - 6.1 --Generic Steps
  - 6.2 --MEAD-CONWAY colors
  - 6.3 --Recognizing D , S , G terminals of MOSFET in LAYOUT
  - 6.4 --Distinguish between PMOS & NMOS on LAYOUT
- 7) Applying Point-6 to make LAYOUT of CMOS Inverter , Simulate , Analyze & Interpret the waveforms.
- 8) Appreciating mathematical model for P(dynamic) of CMOS system.

### ①,② List of Assignments & Order of conduction:-

① Aim :-

① To make layout of given CMOS system , Simulate the Layout ; Analyse the CS/F's , Interpret & conclude ; using MICROWIND Tool

② Learn the Schematic To Layout Flow using DSCH - Tool

**B. 1)**

Already performed while Teaching the Tool

**(B.1.a)** CMOS INVERTER ( $\rightarrow o \rightarrow$ )

$\Rightarrow$  Observe that  $V_{out} = \overline{V_{in}}$  ✓

$\Rightarrow$  Observe effect of changing values of  $f_{clk}$ ,  $C_L$ ,  $V_{DD}$  ; on  $P_{dynamic}$

**(B.1.b)**

CMOS NAND Gate  
CMOS NOR Gate  
CMOS AND Gate  
CMOS OR Gate

} Verify the Boolean expression for o/p Y

**(B.1.c)** Transmission Gate (TG)

$\Rightarrow$  Verify the functionality :  $Y = \text{STRONG-1} ; \text{for } I/O = 1$   
 $= \text{STRONG-0} \quad \text{for } I/O = 0$

**(B.2)** 2:1 MUX using TG :-

$\Rightarrow$  Verify the functionality :

$$\left. \begin{array}{l} Y = I_0, \text{ for } S=0 \\ = I_1, \text{ for } S=1 \end{array} \right\} \text{where } \begin{array}{l} I_0 = \text{HF clock} \\ I_1 = \text{LF clock} \\ S = \text{VLF clock} \end{array}$$

### (B.1.d) Half-Adder using MULTIPLEXER

⇒ Converting 2:1 MUX into Logic Gate

⇒ Converting 2:1 MUX → XOR Gate

⇒ Converting 2:1 MUX → AND Gate

⇒ combining Above 2 to form Half-Adder

### (B.3) 1-bit SRAM cell :-

#### (B.3.a): Using NMOS S/w

⇒ Justifying Drawback of the Implementation

as generating O/p = Weak-1 ; for Data-write = 0

#### (B.3.b) using TQ S/w

⇒ Justifying the Drawback of (B.3.a) is removed

by showing O/p = STRONG-1 ; for Data-write = 0

## ③,④ Installation of MICROWIND & DSCH Tools:-

③ { ⇒ There is No Installation, but "Invocation" for both Tools.

⇒ Tools open by simply clicking a particular \*.exe file

### ④.1 ⇒ For MICROWIND Tool:-

Double-click the file **Microwind31.exe** in the full. path:-

**Your-Drive/Microwind 3.1 Full/System**

### ④.2 ⇒ For DSCH Tool:-

Double-click the file **Dsch3.exe** in the full. path:-

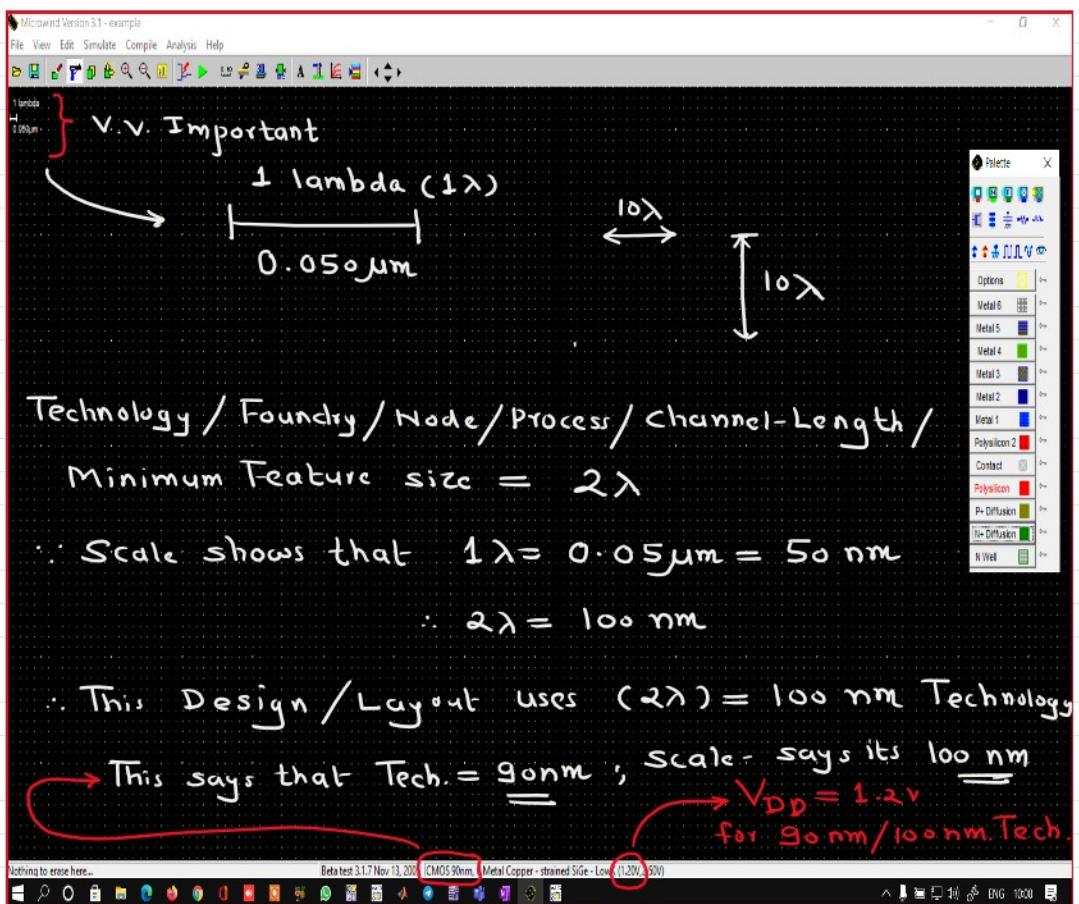
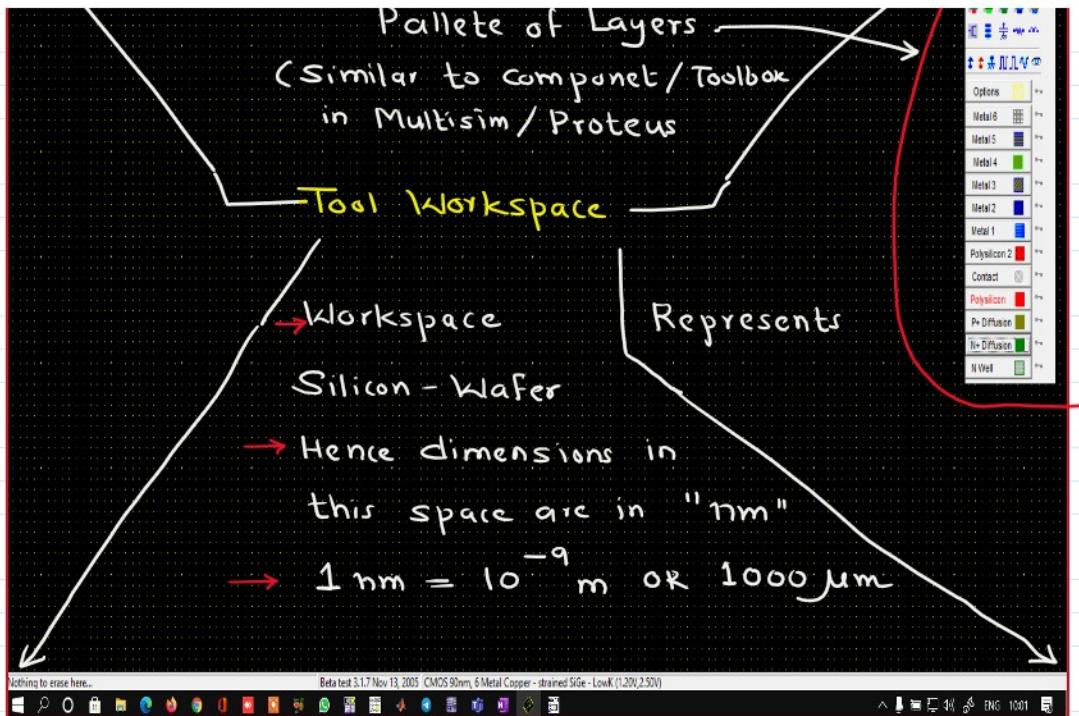
**Your-Drive/DSCH**

## ⑤ knowing the GUI of MICROWIND:-

⇒ open the Tool as mentioned in point **4.1**

⇒ The GUI will look as below:-

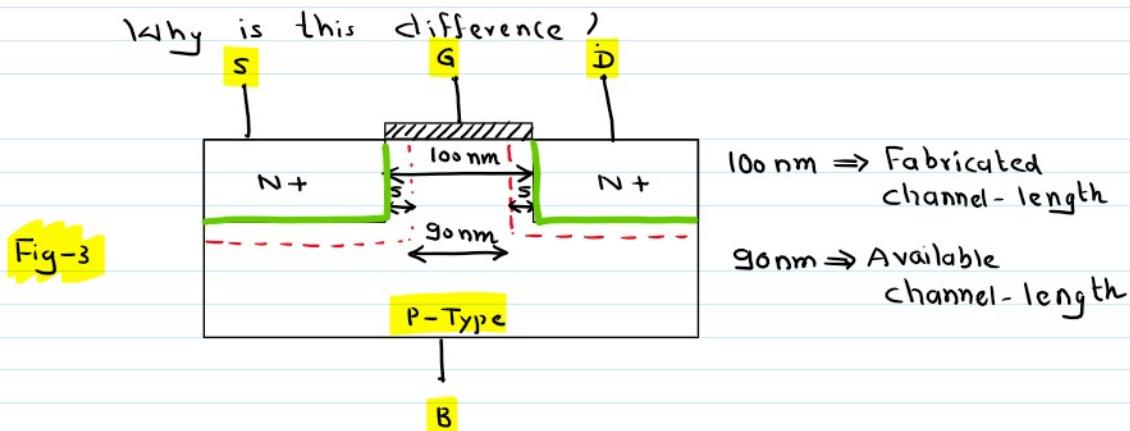




\* From Scale, we get Technology =  $2\lambda = 100 \text{ nm}$

But Task-bar says that Technology = 90 nm

Why is this difference?  
S G D  
1 1 1



\* If i use 180 nm Process/Technology; i will get

$$2\lambda = 200 \text{ nm}$$

Again this difference bet'n 180nm , 200 nm is due to Reduction owing to Depletion-Regions

⑥

⑥.1 Generic steps to make Layout of any CMOS system:-

Steps (S):

S.1) Correct Starting point (CSP) for making Layout is Transistor-Level Schematic  
 $\hookrightarrow$  MOSFET

S.2) Terminalise the circuit  $\Rightarrow$  Show D, S, G - Terminals of each MOSFET in the circuit

S.3) Place MOSFETs in Workspace using "Mos Generator" from PALLETE

S.4) Align the MOSFETs such that minimum-length connections will be needed to connect the terminals of one MOSFET to those of another

$\hookrightarrow$  Use stretch/move icon

S.5) Connect the MOSFETs to each other by connecting their terminals as per (S.2) (Refer Fig-5 for Rules)

S.6) Give  $+V_{DD}$ ,  $-V_{SS}$  supplies as per (S.2)  
 (Select & Drop from PALLETE onto the Terminal)

S.7) Connect "All N-Well's" to  $+V_{DD}$  supply

S.8) Apply Input signals (I/O / clock) to the correct nodes as per (S.2), from PALLETE

S.9) Define O/p Signals at the correct nodes as per (S.2)  
 (Drop "VISIBLE NODE" from PALLETE on O/p Node)

S.10) Run DRC (Design Rule Check)  
 (Click DRC on ICON-Bar)

S.11) If DRC reports ERRORS; correct them

If DRC reports "No Design Rule Error. Congratulations ---"  
 go to (S.12)

(S.12) Run the Simulation, observe O/p wfs vs I/p wfs

go to (S.12)

(S.12) Run the Simulation, observe O/p w/f's vs I/p w/f's  
(click ▶ from Icon-Bar)

(S.13) Verify the Functionality referring to Truth-Table

(S.14) Note the value of Pdynamic (Dynamic power Dissipation)

(S.15) To measure  $t_{rise}$ ,  $t_{fall}$  (Use Delay  ) } In w/f  
To measure frequency (Use frequency  ) } window

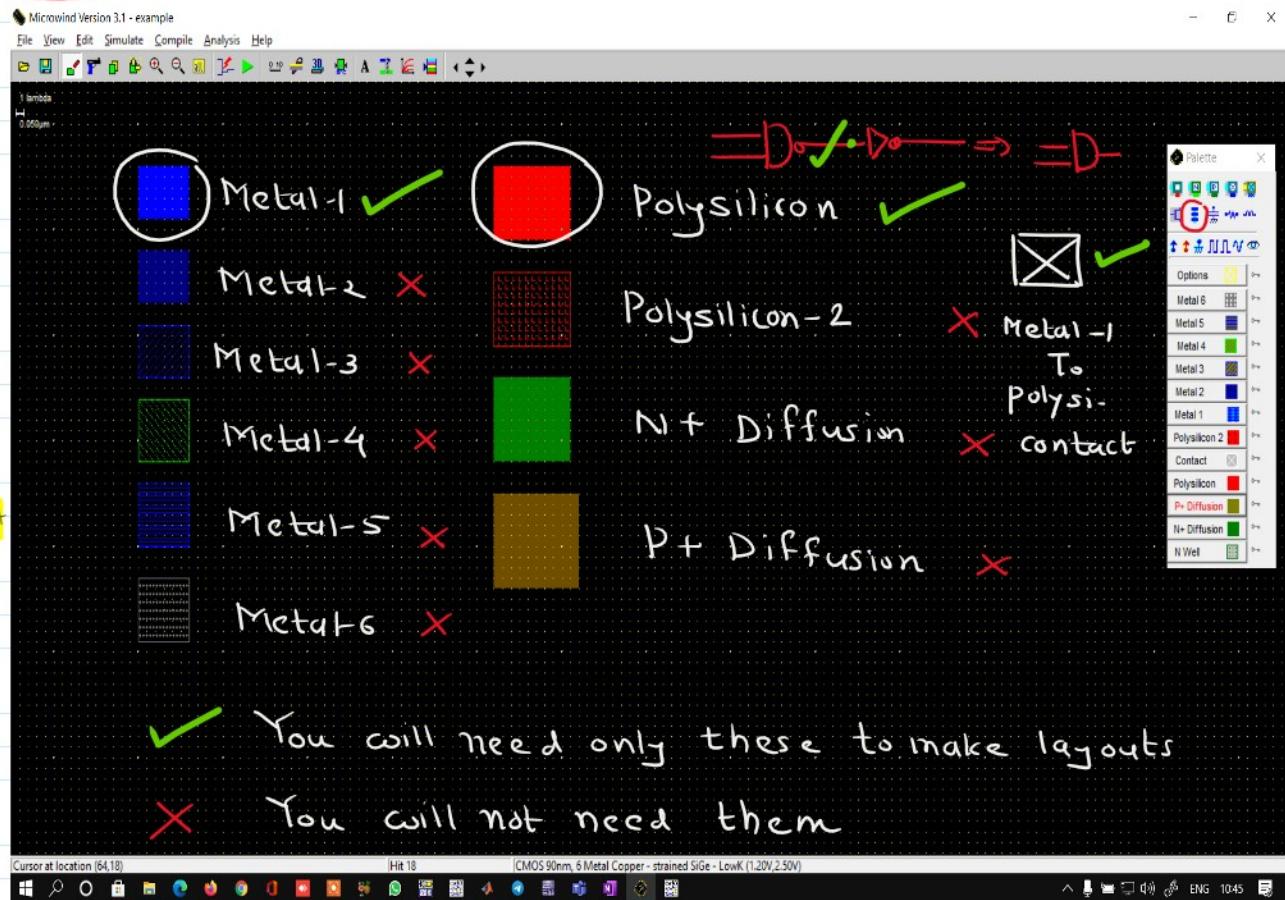
## 6.2 MEAD-COMWAY colours.

⇒ 2 Scientists "Mead" & "Conway" observed a fabricated chip under Electron-Microscope; when exposed to WHITE light

⇒ Different parts of chips reflected diff. wavelengths

⇒ N+  
P+  
polysilicon  
Metal-1  
Metal-2  
:  
Metal-6 } All layers appeared in diff  
                  colours  
                  (Fig-4)

## 6.2

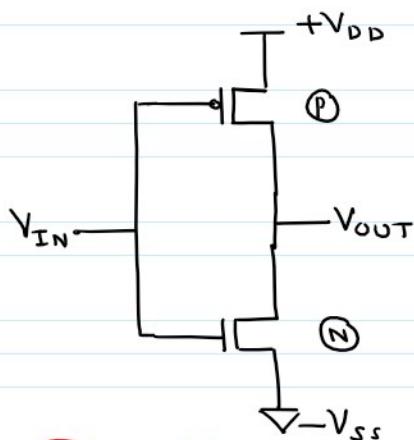


## (S.1) MOSFET- Level Schematic:

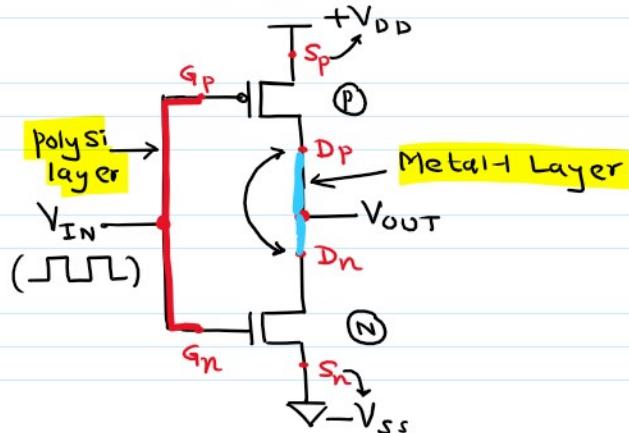
$$V_{IN} \rightarrow V_{OUT} = \overline{V_{IN}}$$

$V_{IN}$	$V_{OUT}$
0	1
1	0

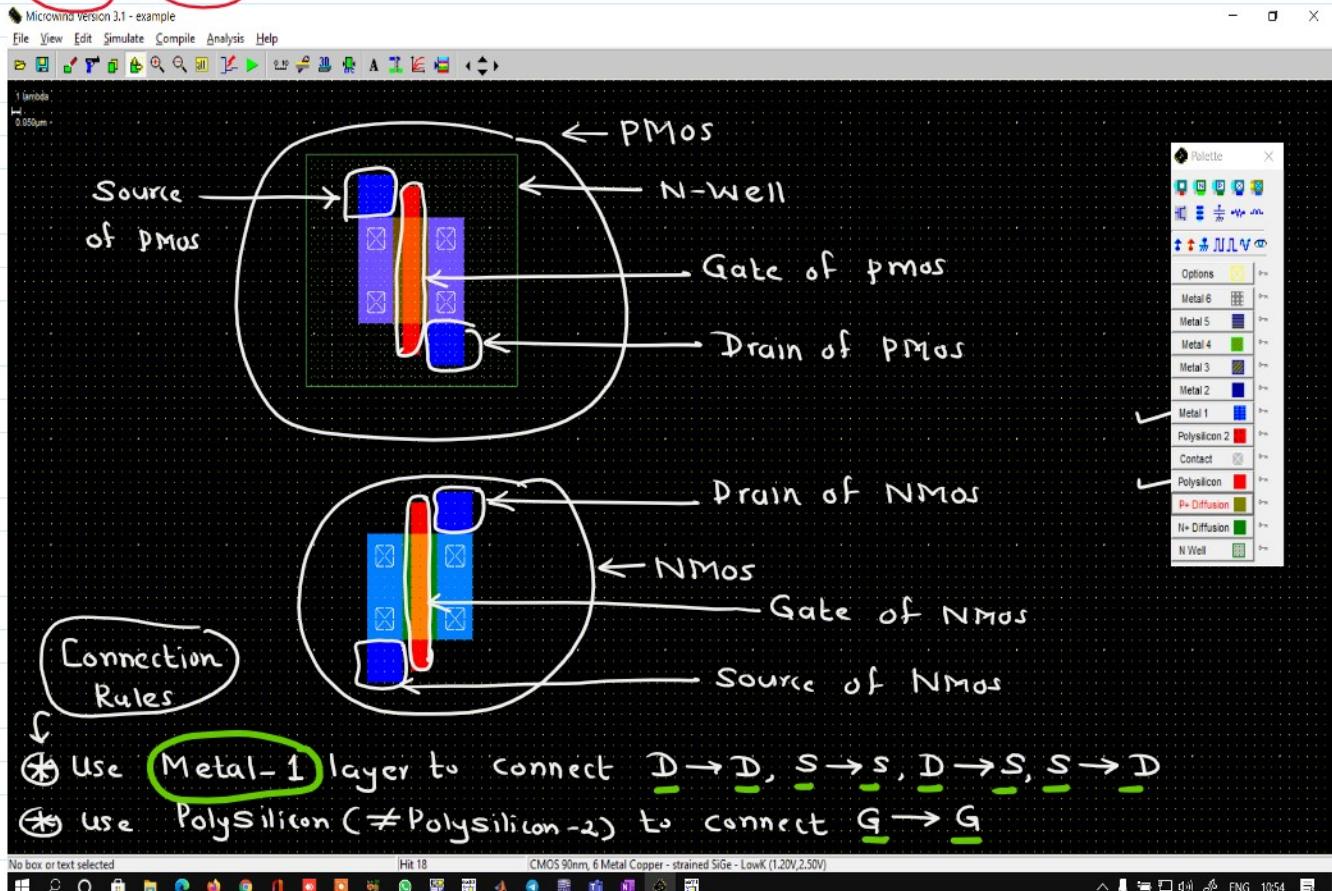
(S.1)



(S.2)



(6.3) & (6.4)



No box or text selected Hit 18 CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V, 2.50V)

ENG 1054

Windows 10 Start Taskbar

File View Edit Simulate Compile Analysis Help

1 Lambda: 0.050μm

Run simulation Add

S = Source, D = Drain, P = pmos, N = nmos,  $D_p$  = Drain of pmos...  
 $S_n$  = Source of nmos...

Fig-5

DRC

Microwind Version 3.1 - example.MSK

File View Edit Simulate Compile Analysis Help

1 Lambda: 0.050μm

Run simulation Add

Palette

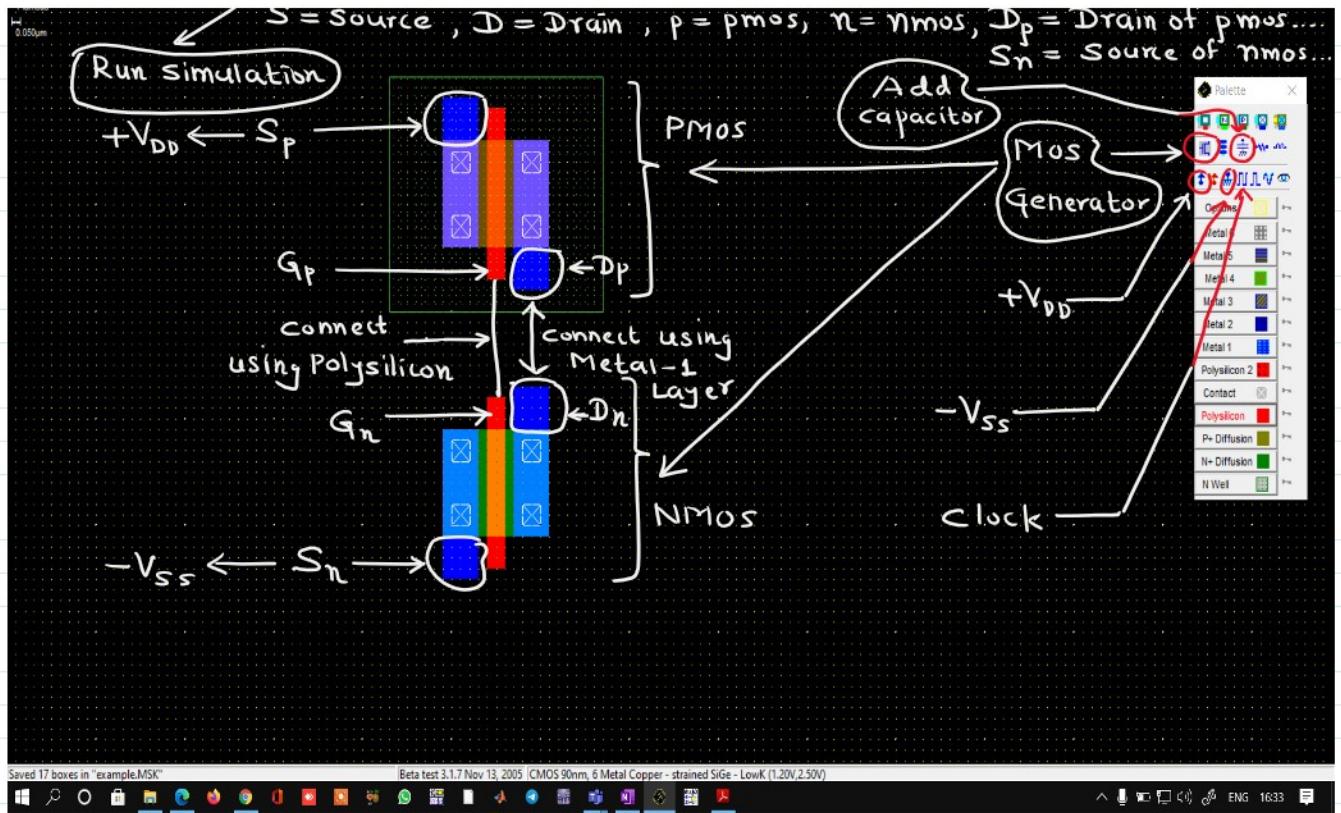


Fig-6

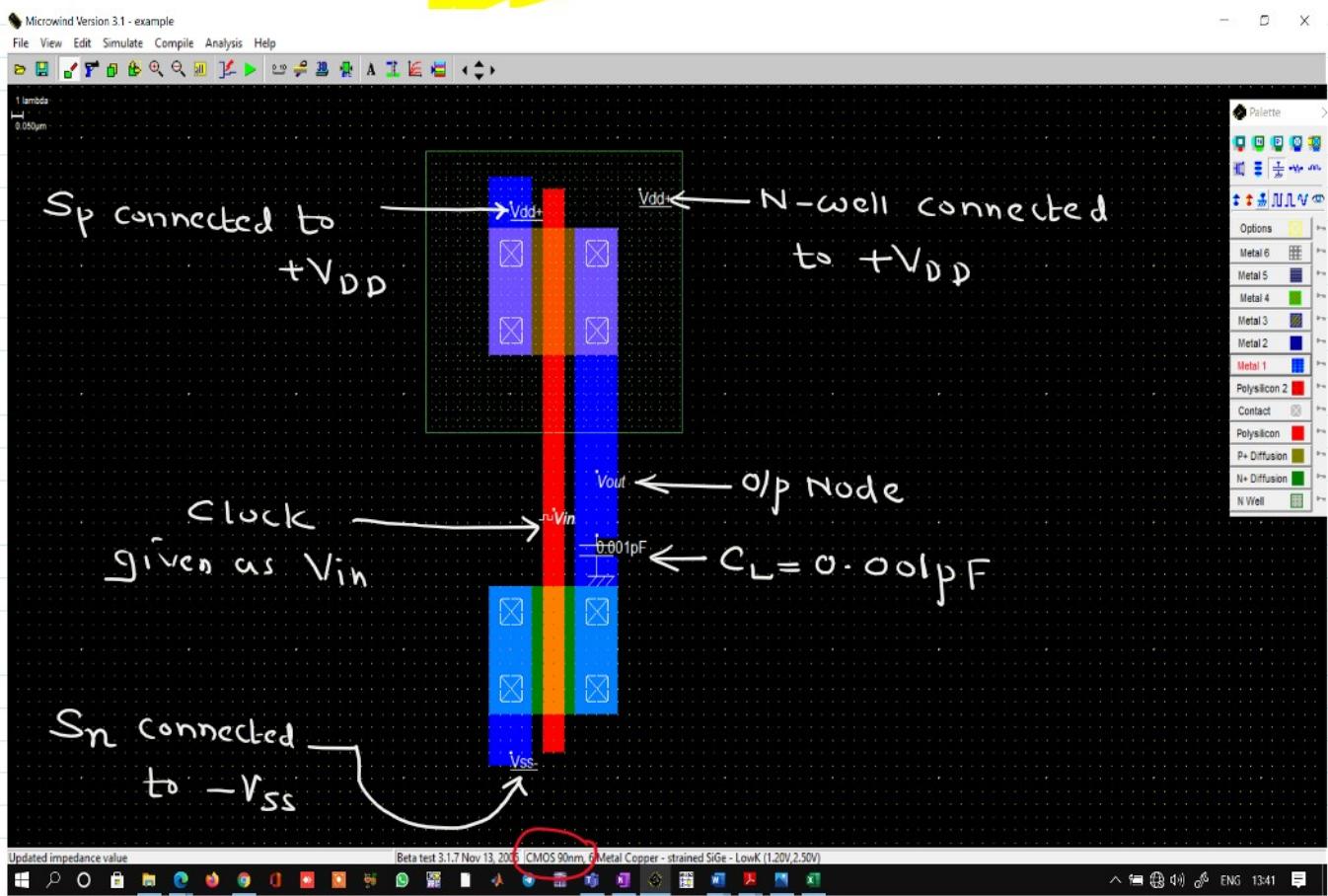


Fig-7 90nm Process CMOS Inverter Layout



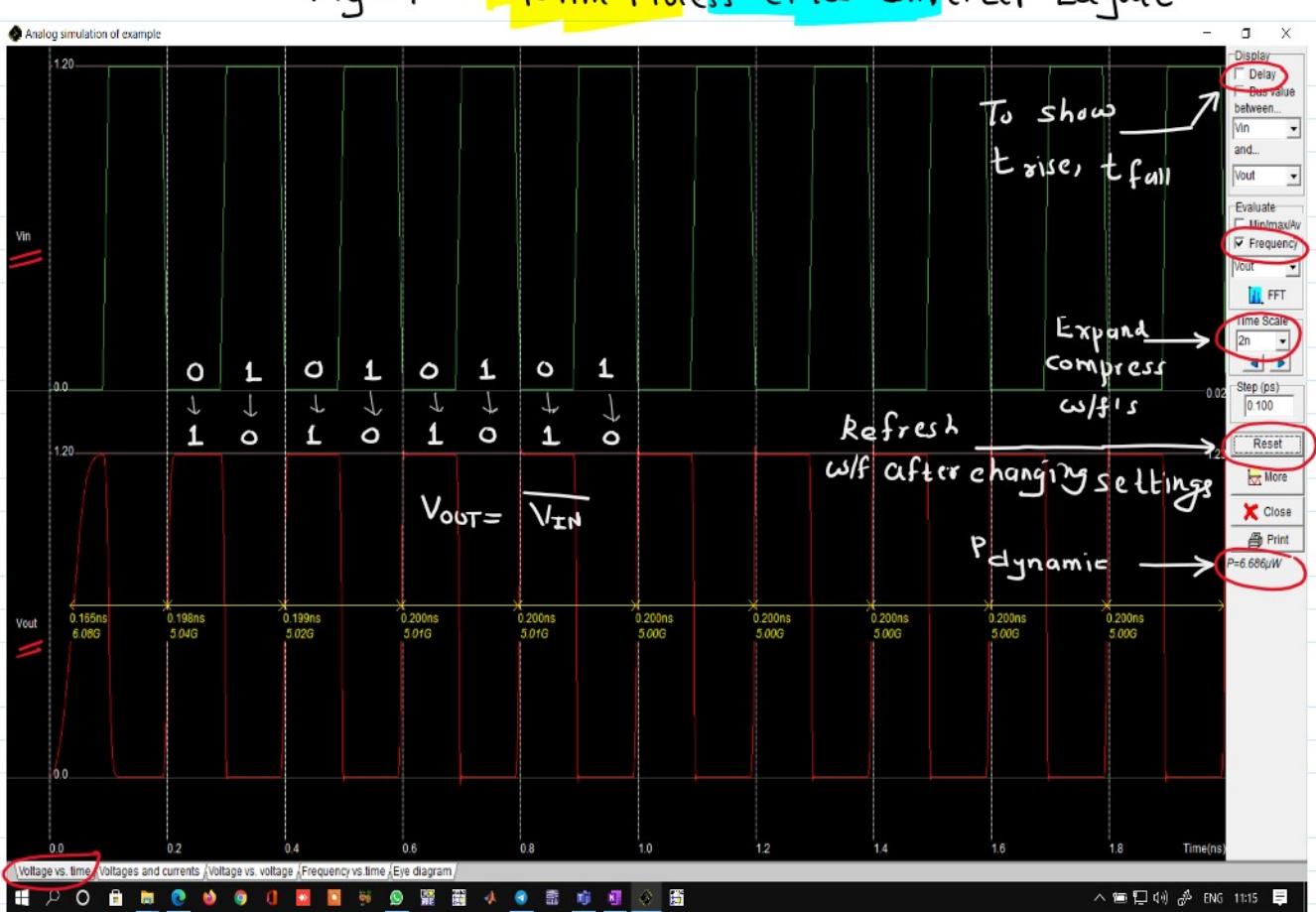


Fig-8 Simulation

⑧ Appreciating the Mathematical model for  $P_{\text{dynamic}}$  of CMOS system:-

$$\Rightarrow P_{\text{dynamic}} = C_L * f_{\text{clk}} * (V_{DD})^2$$

$$\Rightarrow C_L = \text{Load capacitance} = 0.001 \text{ pF}$$

$$\Rightarrow f_{\text{clk}} \approx \frac{1}{t_{on} + t_{off} + t_r + t_f} = \frac{1}{(g_0 + g_0 + l_0 + l_0) \text{ ps}} = 5 \text{ GHz}$$

$\uparrow \quad \uparrow \quad 0.01 \text{ ns} \quad 0.01 \text{ ns}$

$$t_{(\text{high})} = t_{(\text{low})} = 0.09 \text{ ns}$$

$$\Rightarrow V_{DD} = 1.2 \text{ V} \text{ (Standard for } 90 \text{ nm foundry)}$$

$\curvearrowleft$  Remains constant for this foundry  
Cannot be changed manually

$$\begin{aligned} \Rightarrow P_{\text{dynamic}} &= (0.001 \text{ pF}) * (5 \text{ GHz}) (1.2)^2 \\ &= 10^{-15} \times (5 \times 10^9) \times 1.44 \\ &= (7.2 \times 10^{-6}) \\ &= 7.2 \mu\text{W} \text{ (Theoretical)} \end{aligned}$$

## — $T_{\text{L}} \leftarrow \mu\text{W}$ (Theoretical)

④ Showing effect of changing  $C_L$ ,  $f_{\text{clk}}$ ,  $V_{\text{DD}}$  :-

① Effect of  $C_L$  :- Currently  $C_L = 0.001 \mu\text{F}$

$\Rightarrow$  Keep  $f_{\text{clk}} = 5 \text{ GHz}$ ,  $V_{\text{DD}} = 1.2 \text{ V}$  (constant for 90 nm foundry)

$\Rightarrow$  Double value of  $C_L$ , Halve value of  $C_L$

Sr.No.	$C_L (\mu\text{F})$	$P (\mu\text{W})$
1	$0.002 \rightarrow 2 * C_L$	?
2	$0.001 \rightarrow C_L$	?
3	$0.0005 \rightarrow C_L/2$	?

② Effect of  $f_{\text{clk}}$  :- currently  $t_{(\text{High})} = t_{(\text{Low})} = 0.09 \text{ ns}$  (90 ps) ← (Add a clock) dialog box

$\Rightarrow$  Keep  $C_L = 0.001 \mu\text{F}$ ,  $V_{\text{DD}} = 1.2 \text{ V}$  (constant for 90 nm foundry)

$\Rightarrow$  Double value of  $f_{\text{clk}}$ , Halve the value of  $f_{\text{clk}}$

Click "Faster"

in "Add a clock" dialog-box

Click "slower"

in "Add a clock" dialog-box

Sr.No.	$f_{\text{clk}} (\text{GHz})$	$P (\mu\text{W})$
1	$10 \rightarrow 2 * f_{\text{clk}}$	?
2	$5 \rightarrow f_{\text{clk}}$	?
3	$2.5 \rightarrow f_{\text{clk}}/2$	?

③ Effect of  $V_{\text{DD}}$  :- Currently  $V_{\text{DD}} = 1.2 \text{ V}$ ; as foundry = 90 nm.

$\Rightarrow$  We cannot have any value of  $V_{\text{DD}}$ , other than 1.2 V as long as we are using 90 nm foundry.

$\Rightarrow$  Let us use 180 nm foundry and make new CMOS Inverter

$\Rightarrow$  Steps :-

$\Rightarrow$  File  $\rightarrow$  New : Opens a new Workspace

$\Rightarrow$  File  $\rightarrow$  Select Foundry

Select  $\text{cmos018.rul}$

$\Rightarrow$  Note Scale changes to 1 lambda = 0.100  $\mu\text{m}$  (100 nm)

$\Rightarrow$  Note in Taskbar : CMOS 0.18  $\mu\text{m}$ -6 Metal (2.00V, 3.30V)

$\downarrow$   
 $V_{\text{DD}}$

⇒ Build the CMOS Inverter

⇒ Keep  $f_{clk} \Rightarrow t_{(high)} = t_{(low)} = 0.09 \text{ ns}$   
 $t_r = t_f = 0.01 \text{ ns}$

⇒  $C_L = 0.001 \mu\text{F}$

⇒ Run Simulation (After DRC)

Sr.No.	V <sub>DD</sub> (V)	P (μW)
1	1.2	12.74
2	2	?

What to expect?

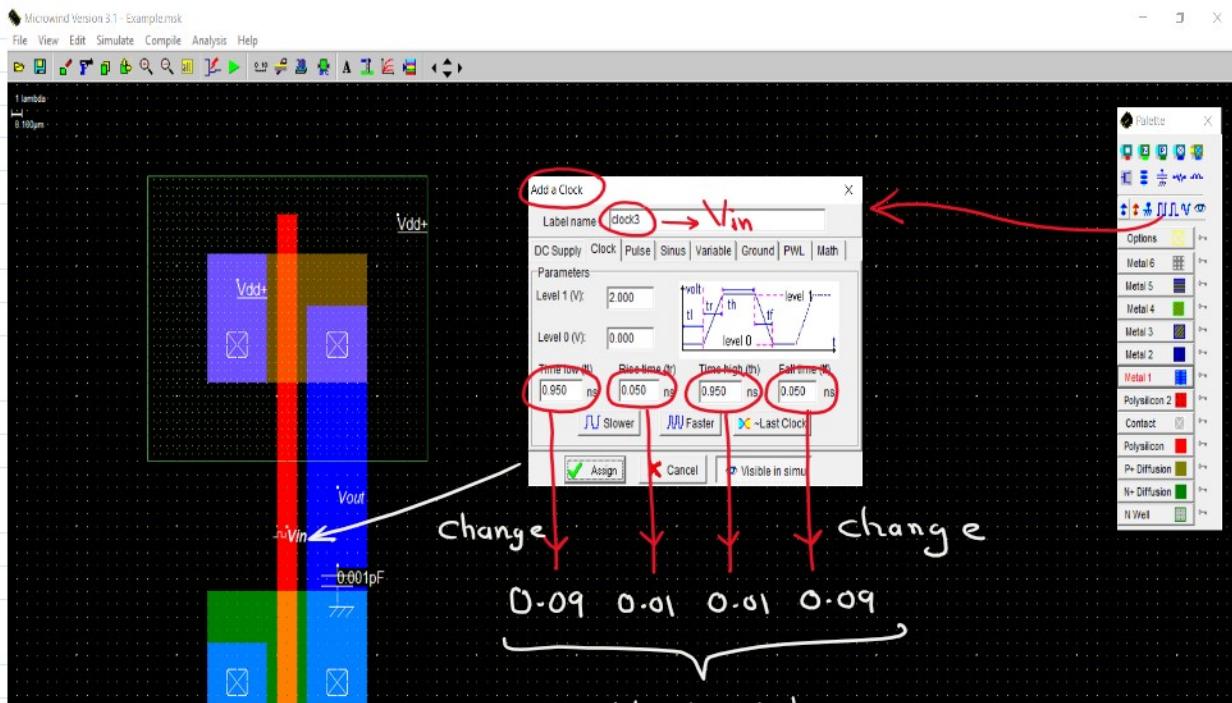
\*  $P_{dynamic} \propto (V_{DD})^2$

∴ The old-value of  $P_{dynamic}$  should get scaled up by

$$\left(\frac{2}{1.2}\right)^2 = 2.78 \quad (\text{Ideally})$$

⇒ The value obtained after simulation may not exactly match the scale-up factor of 2.78 ; due to parasitic-capacitances in the Layout

⇒ But ; you should get an ↑ in value of  $P_{(dynamic)}$



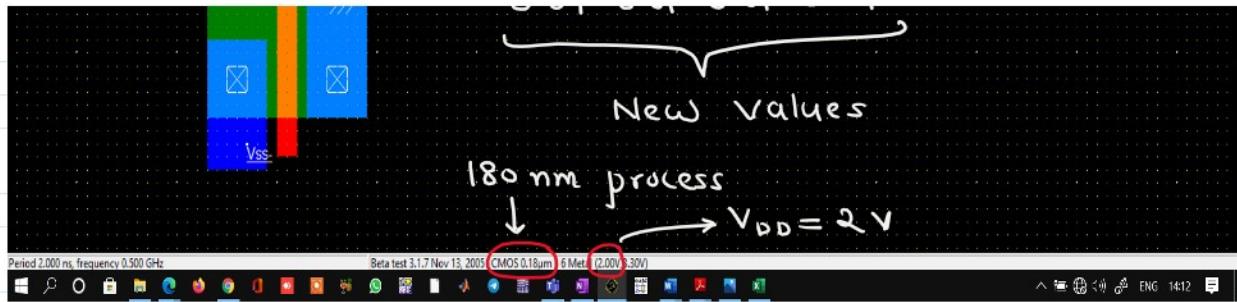


Fig:- 9: 180 nm Process CMOS Inverter Layout