Q8_08-10-21

09:37

⊛ Assignments :- B.1.b (using 90nm Foundry)

Ⓘ B.1.b :-

a) 2 i/p NAND

b) 2 i/p NOR

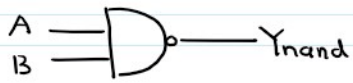
c) 2 i/p AND

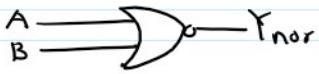
d) 2 i/p OR

⊛ 2 i/p NAND, 2 i/p NOR Gates:-

2 i/p NAND | **2 i/p NOR**

Symbols:



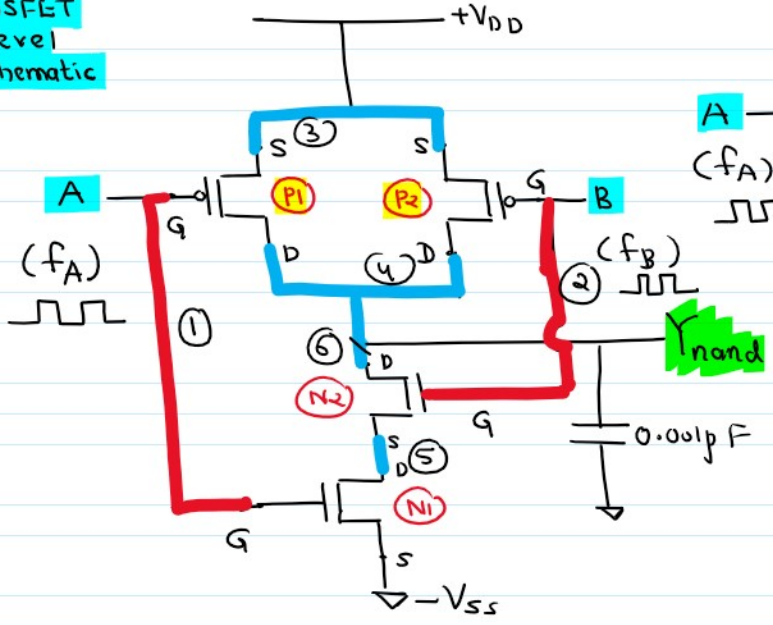


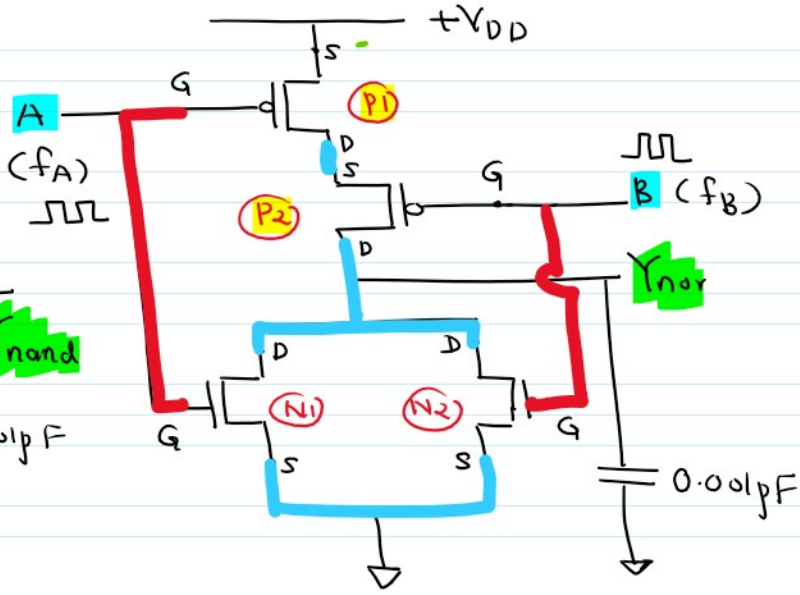
Expression:

$Y_{nand} = \overline{A.B}$ — (P1//P2), (N1–N2)

$Y_{nor} = \overline{A+B}$ — (P1–P2), (N1//N2)

MOSFET Level Schematic





$f_A = \frac{1}{2} \cdot f_B$

$f_A = \frac{1}{2} f_B$

TA TB
A B Ynand

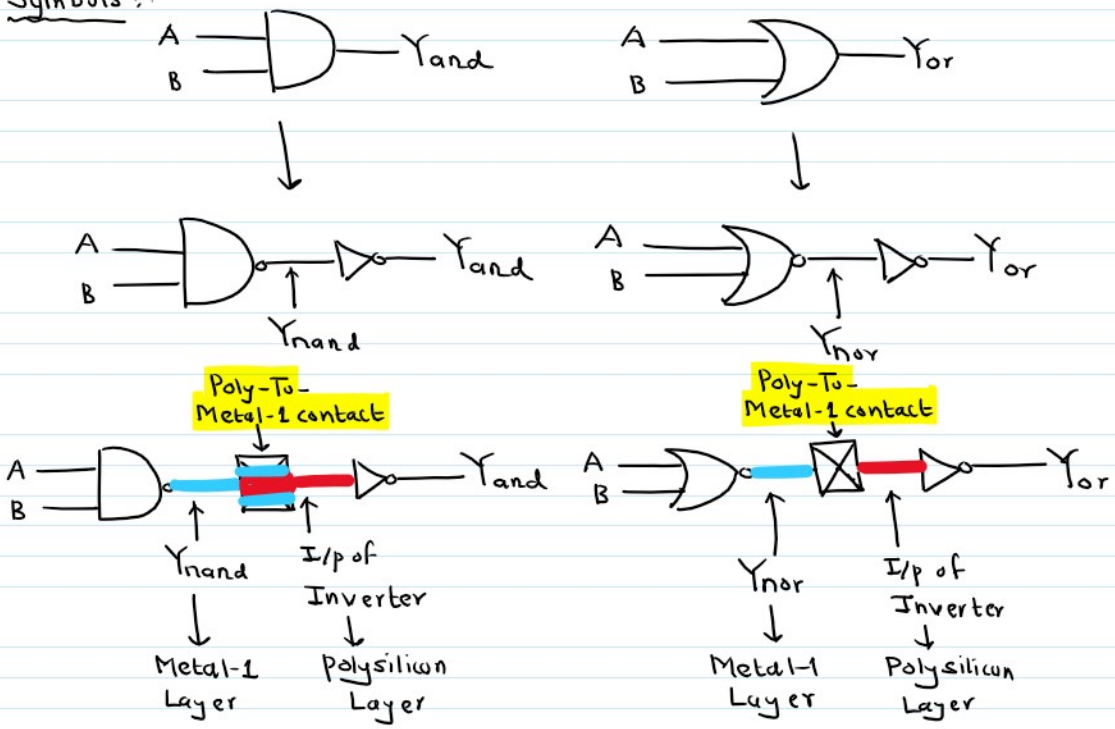
A B Ynor

T_A	T_B	
A	B	Y_{nand}
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y_{nor}
0	0	1
0	1	0
1	0	0
1	1	0

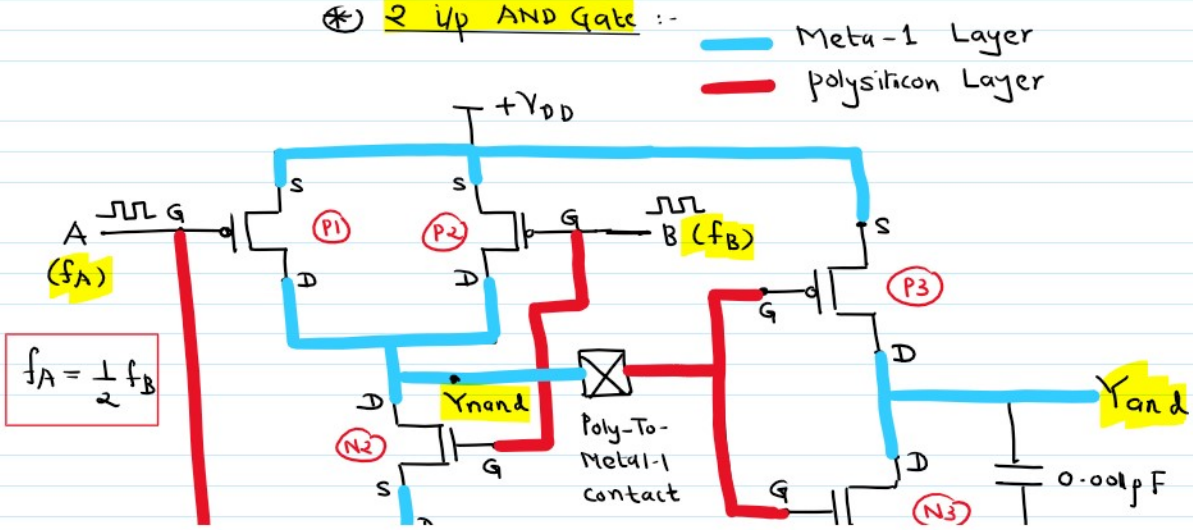
✱ 2 i/p AND, 2 i/p OR Gate:

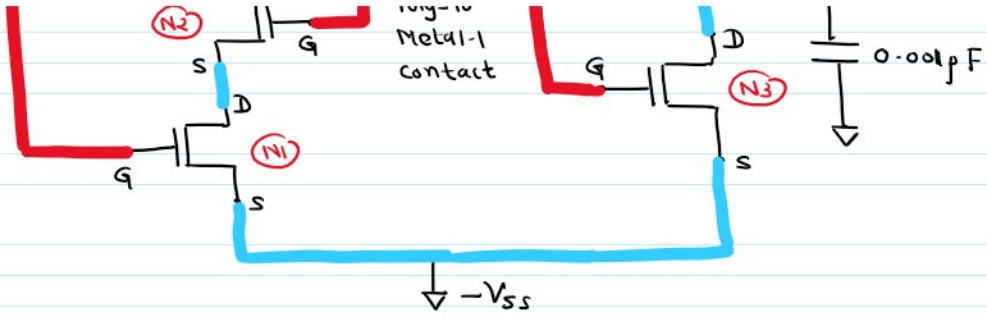
Symbols:



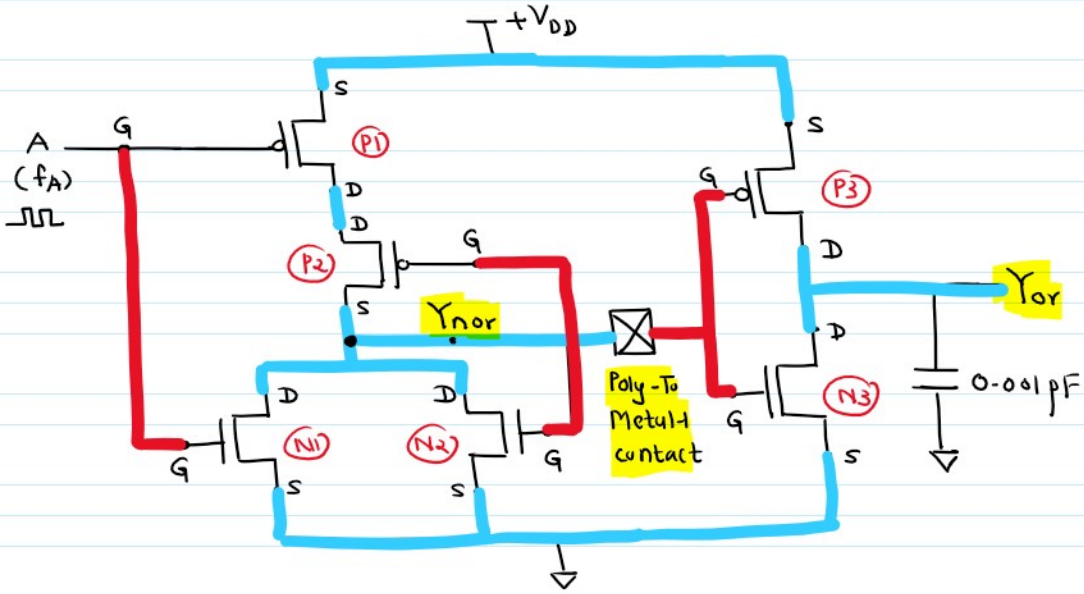
✱ MOSFET-Level Schematics for 2 i/p AND, 2 i/p OR Gate:-

✱ 2 i/p AND Gate:-




N2
G
S
D
Metal-1
contact
N1
G
S
G
D
N3
S
0.001pF
$-V_{SS}$

⊛ 2 ip OR Gate :-


$+V_{DD}$
A
(f_A)
G
S
P1
D
D
P2
G
S
Y_{nor}
D
D
N1
N2
G
S
S
G
Poly-To
Metal-1
contact
S
G
P3
D
Y_{or}
D
N3
G
S
0.001pF