R8_29-07-21

29 July 2021 08:49

Agenda :-

(1) Understanding the Hardware (PLDs)

✓ a) ⇒ Classification of PLDs

✓ b) ⇒ Types of PLD vendors

✓ c) ⇒ Product Line of XILINX Incorporation

✓ d) ⇒ Target Technology for PART-A Assignments

✓ e) ⇒ Detailed Explanation of IC-Number of Target Technology

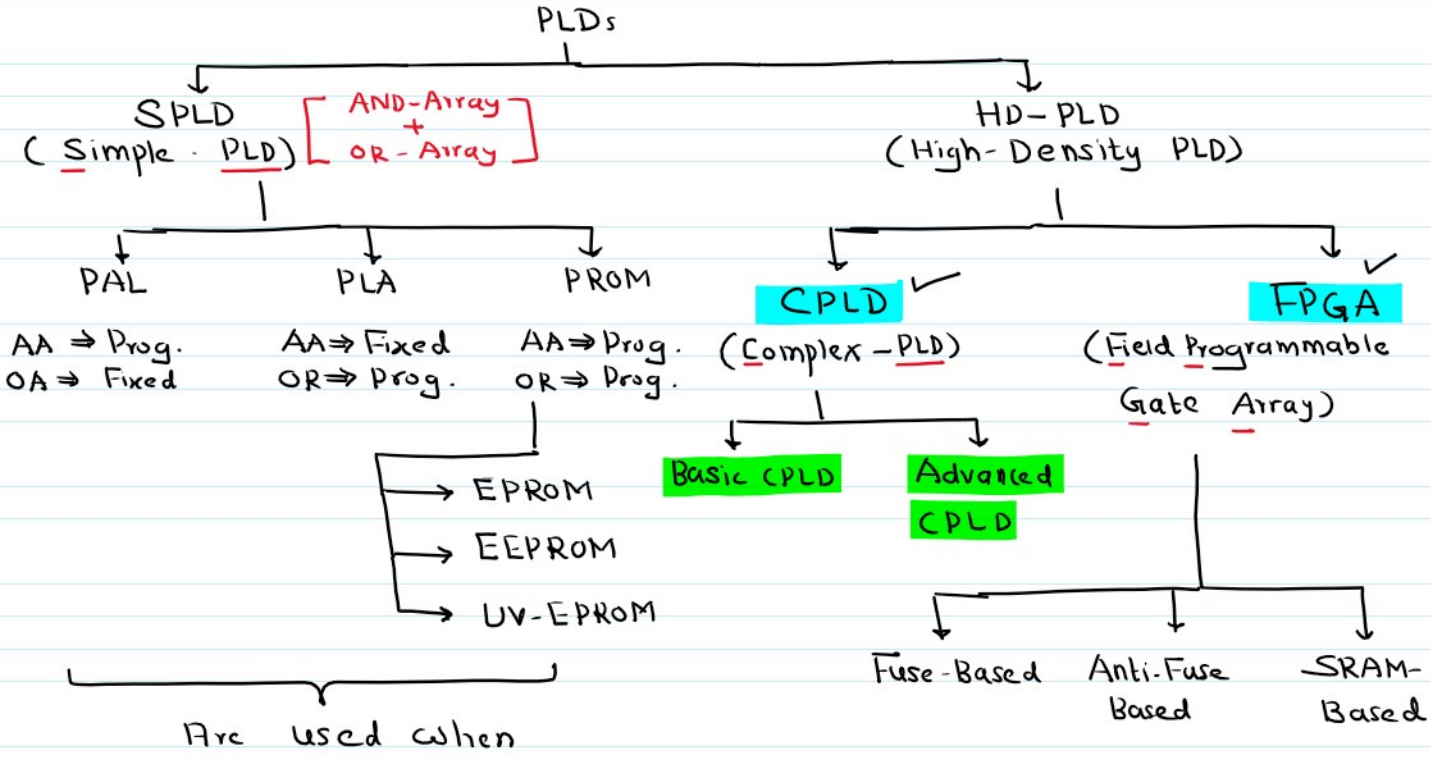
(2) Hands-ON Tool flow for FPGA Prototyping of 2 i/p Logic Gate

a) ⇒ Synthesis of Main VHDL Model

b) ⇒ Simulation of TestBench VHDL Model

(1.a) Classification of PLDs:-

⇒ PLD ⇒ Programmable Logic Device



$\leq$ (I/ps, O/ps) $\leq$ 32

(1.b) Types of PLD-Vendors:-

⊛ Companies which create only H/w :-

⇒ PC / Laptop :-

Only H/ω ⇒ INTEL (i3, i5, i7, i9), AMD (RYZEN), APPLE (M1)

Only S/ω ⇒ MICROSOFT (Windows), LINUX, APPLE (MAC-OS)

⇒ SMARTPHONE :-

Only H/ω ⇒ Qualcomm (SnapDragon); MediaTek (Helio, Dimensity)

Only S/ω ⇒ Google (Android), Oxygen-OS

⇒ PLDs :-

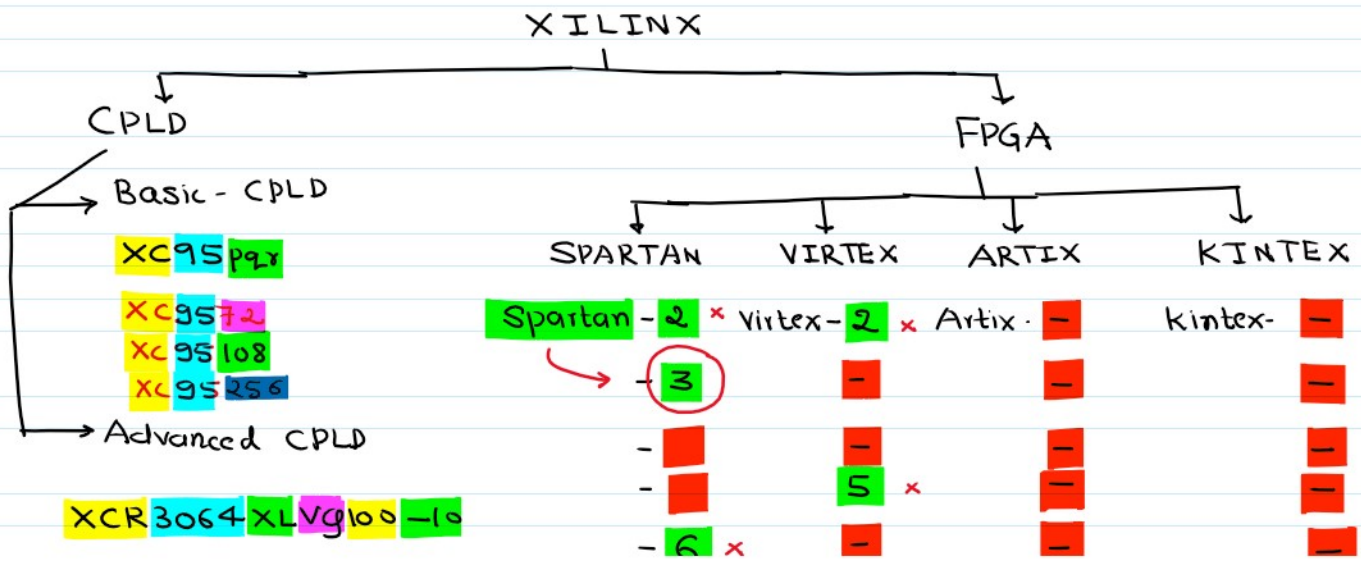
Only H/ω :- NONE

Only S/ω :- Synopsys, Mentor-Graphics
(Synthesis Tools)

H/ω + S/ω :- XILINX, INTEL (Formerly ALTERA)

S/ω :- XILINX ISE, VIVADO, VITIS — QUARTUS-II

(1.c) Product-Line of XILINX Inc. :-



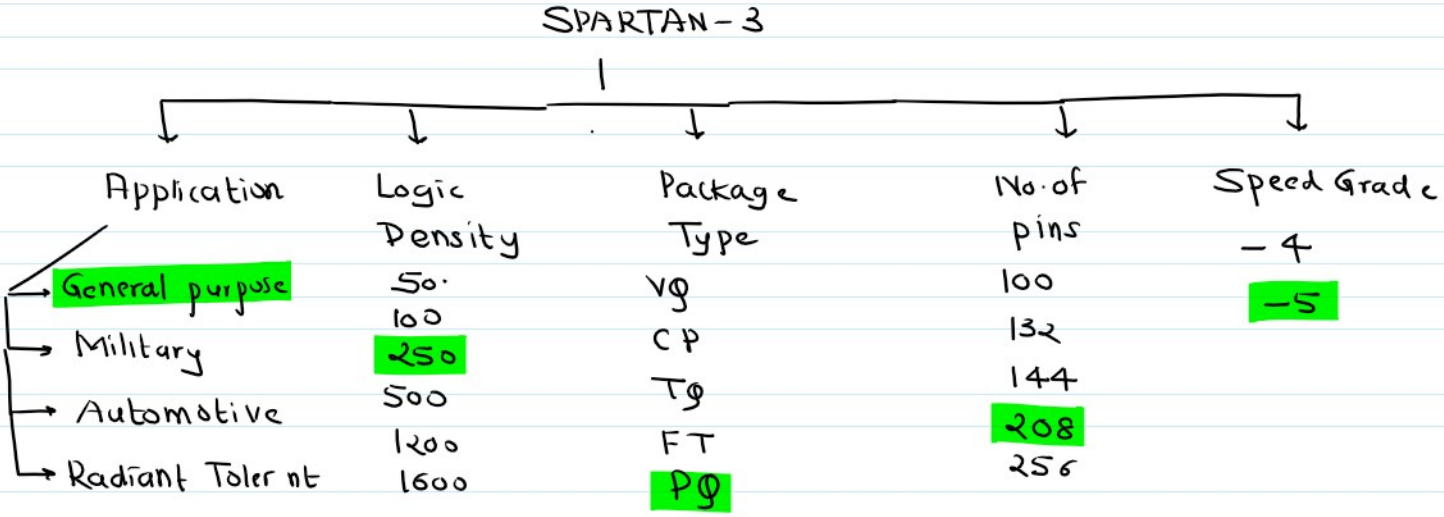
XCR3064XLVQ100-10

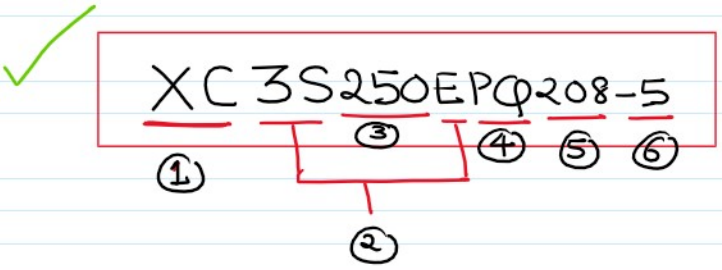
Spartan-6	6S
Virtex-2	2V
virtex-7	7V
Artix-7	7A
kintex-7	7K

(1.d) Target Technology for PART-A Assignments:

⇒ Target Technology (TT) = Hardware into which we will realise our PDS

= PLD which we will program to realise our PDS





Field-No:	Details	Meaning
1	XC	Xilinx Corporation
2	3S, E	S ⇒ SPARTAN, 3 ⇒ Member E ⇒ Variant
3	250	(250 x 1000) Equivalent 2 i/p ⩵
4	PQ	PQFP = Plastic Quad Flat Pack
5	208	No. of pins on IC
6	-5	Speed Grade

-3 > -4 > -5 > -6

$-3 > -4 > -5 > -6$

Faster Slower

(2.a) Synthesis (1) of Main VHDL Model (2) of 2 i/p Logic Gate (3) :-

(1) Task

(2) One of the 2 models

(3) PDS

⇒ In each Assignment of PART-A

⇒ We have 2 VHDL-Models :-

⇒ 1st VHDL Model ⇒ MAIN Model (To be SYNTESIZED) (XST)

- → Library statements (LS)
- → Defining i/p & o/p signals (ED)
- → Relating i/p & o/p signals (AB)

⇒ 2nd VHDL Model ⇒ Test-Bench Model (To be SIMULATED) (ISim)

⇒ STEP-1 :- SYNTHESIS

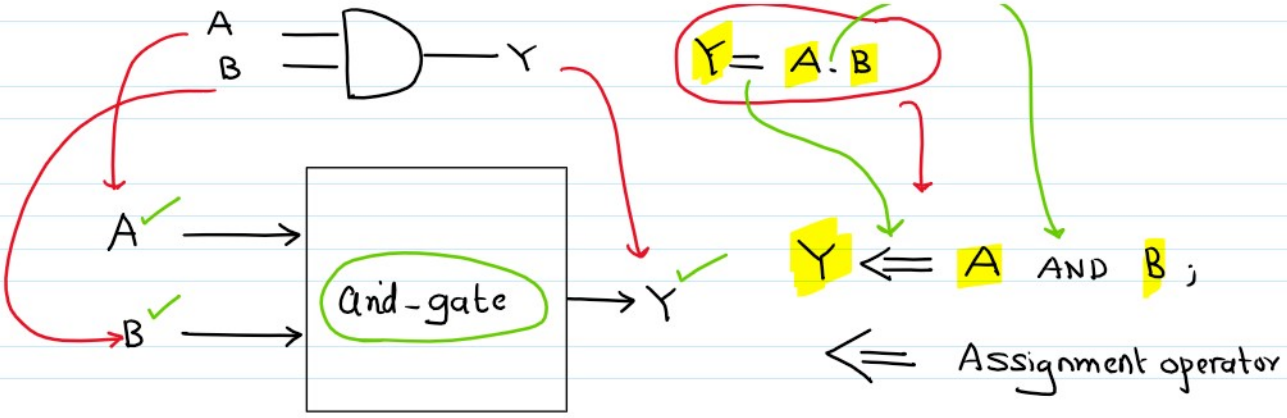
CSPs (Correct Starting Points)

⇒ Draw the Correct Block-Diagram (BD) showing all i/p and o/p signals with Valid Signal names

⇒ Express the Logical Relationships bet'n i/p & o/p signals in one of the following ways :-

- ⇒ Boolean Expression ✓
- ⇒ Truth-Table
- ⇒ State-Diagram
- ⇒ Excitation-Table
- ⇒ Algorithm

⇒ Consider 2 i/p  as our P.D.S :-



Write Entity Name inside the Box

Valid

- Cannot be same as keyword in VHDL
- Cannot start with Numeral
- Cannot have special character other than "_"

Y <= A AND B ;

Logical And'ing bet'n Signal A, Signal B is Assigned to O/p signal Y