PART-A_THEORY (Compiled by Mr.H.S.Thakar)

30 November 2020 17:31

(I) List of Assignments :-

* Refer to PART-A Sample Assignment.pdf for Order of contents in soft-copy

Assignment Number	Assignment-Title	① ② ← Assignment Contents → ⑧ ⑨ ⑩
		BD | TT | MM | RTL-S | T-S | DUS | T-SUM | TBM | Sim | UCF
1	4-bit ALU	* Order of contents:- ① → ⑩
2	4-bit USR	* All 10 compulsory for all 4
3	FIFO / Memory	
4	FPGA - LCD I'face	

Contents :- ① → ⑩ abbreviations elaborated :-

① BD = Block Diagram

② TT = Truth-Table / Function Table

③ MM = Main (VHDL) Model

④ RTL-S = RTL Schematic

⑤ T-S = Technology Schematic

⑥ DUS = Device Utilisation Summary

⑦ T-SUM = Timing Summary

} These are contained in Synthesis Report

⑧ TBM = TestBench (VHDL) Model

⑨ Sim = Simulation W/f's

⑩ UCF = User Constraint File

* Theory Section of PART-A Assignment

(II) Assignment-wise BD's & TT's / FT's :-

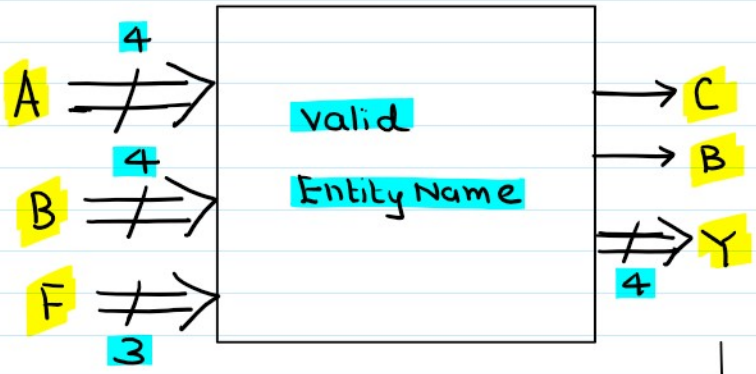
* Signal-names in BD are just for Illustration *

(II) Assignment-wise BD's & TT's / FT's :-

(*) Signal-names in BD are just for Illustration (*)

(1) 4-bit ALU (Arithmetic Logic Unit) (2 Arithmetic, 6 logical operations)

BD



(*) A, B : 4-bit operands

(*) F : 3-bit Function Bus (8 operations)

(*) Y : 4-bit SUM/Difference/ Logic O/p

(*) C : Carry

(*) B : Borrow

FT

Function Bus F(2)	F(1)	F(0)	Operations
0	0	0	• 2 Arithmetic
0	0	1	Addition
0	1	0	Subtraction
0	1	1	
1	0	0	• 6 Logical
1	0	1	
1	1	0	
1	1	1	

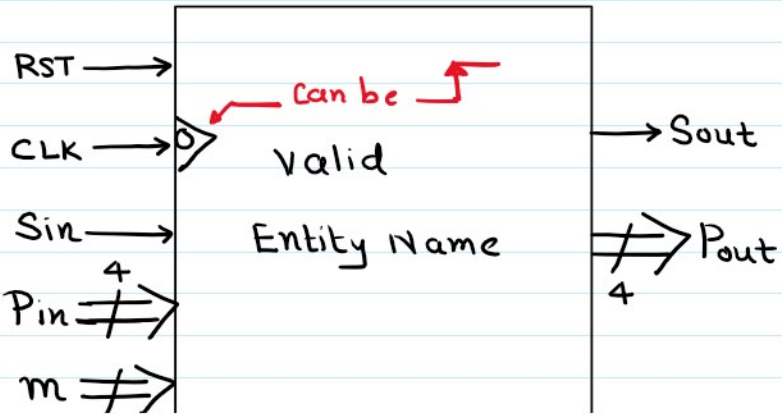
(*) There is Freedom of choice and order in 6 Logical operations

(*) But all 8 operations cannot be Logical.

(2) 4-bit USR (Universal Shift Register) :-

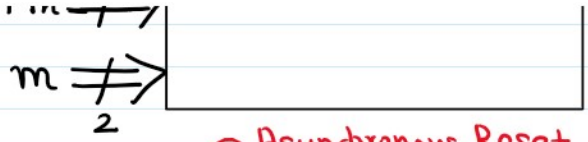
(4 operations ; Shifting can be RIGHT/LEFT)

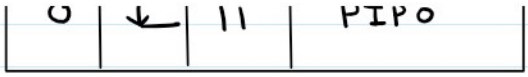
BD



FT

RST	CLK	m	Outputs / mode
1	x	x	Sout = 0 Pout = 0000
0	↓	00	SISO
0	↓	01	SIPO
0	↓	10	PISO
0	↓	11	PIPO





⊛ Asynchronous Reset

⊛ Mode Latency (No. of clock cycles)

⊛ Power Hierarchy:-

Highest
RST
CLK
MODE
↓
Lowest (Equal)
Sin, Pin

SISO = 4 + 4 = 8
SIPO = 4 + 1 = 5
PISO = 1 + 4 = 5
PIPO = 1 + 1 = 2

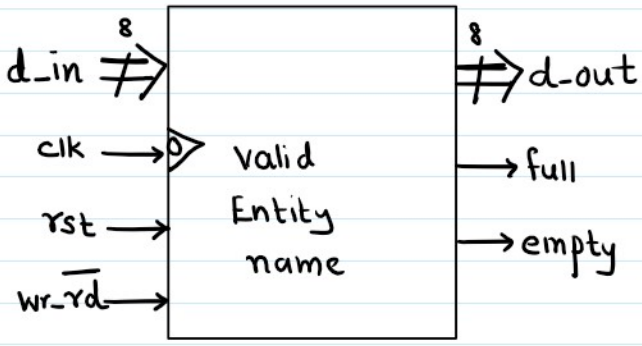
(3) FIFO / 32-bit Memory (Organised as 4 x 8) :-

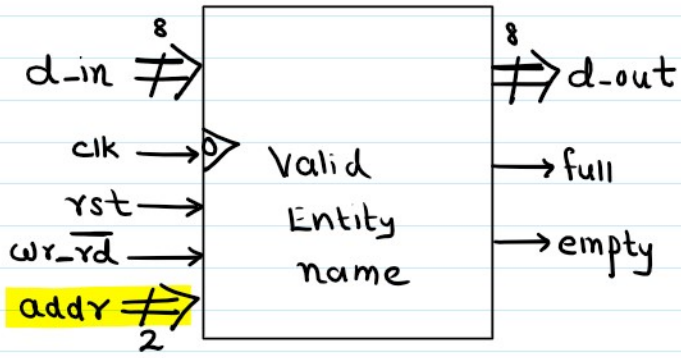
⊛ Can be a True FIFO (uses memory pointers, No address)

OR

⊛ Byte-Addressable Memory which can store 32-bits of data in form of 4 words, each 8-bit long (uses Address)

BD





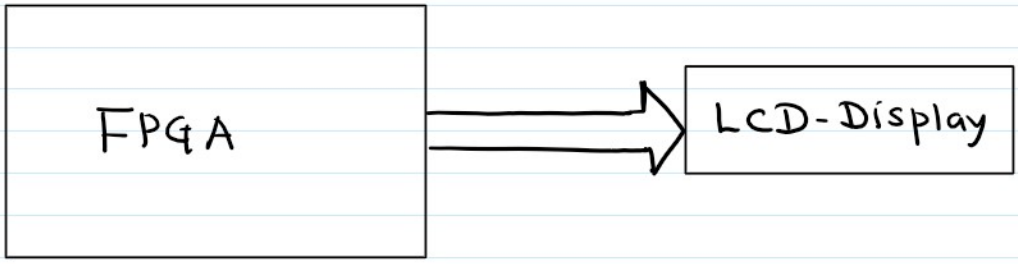
FT

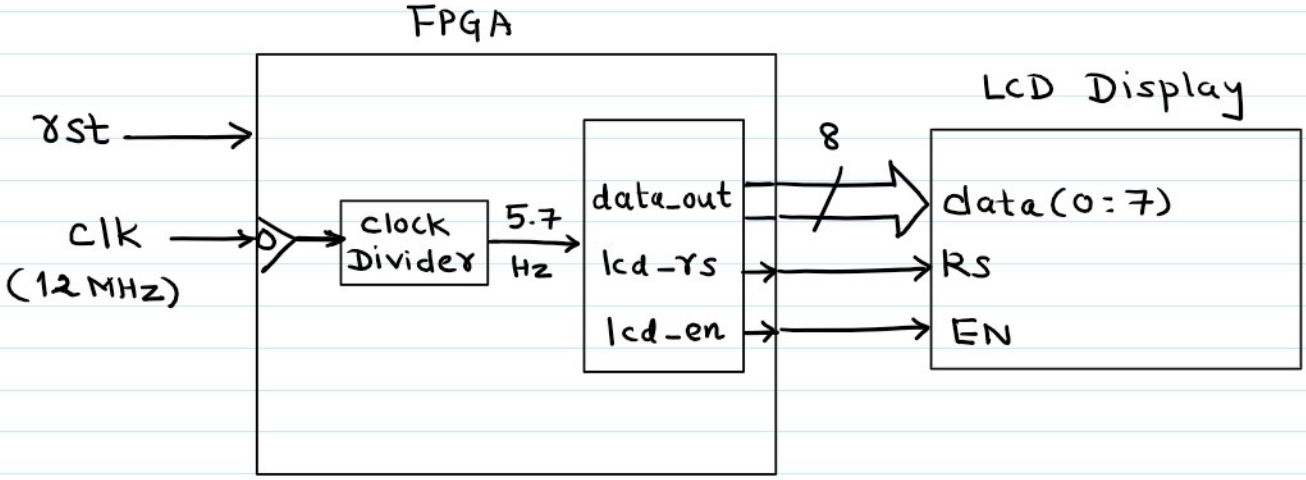
WRITE, READ are Active-High, Active-Low Resp.

rst	clk	wr_rd	d_out	full	empty
1	x	x	$(00)_{16}$	0	1
0	↓	1	NA	0→1	0
0	↓	0	d_in	0	0

rst	clk	wr_rd	addr	d_out	full	empty
1	x	x	x	$(00)_{16}$	0	1
0	↓	1	$(00)_2$ ↓	NA	0→1	0
0	↓	0	$(11)_2$	d_in	0	0

④ LCD - FPGA Interfacing :-





Pin Assignment (UCF Location) for LCD:

Signal Name	XC3S250E-PQ208	XCS6LX9-TQG144
LCD_RS	P48	P74
LCD_EN	P49	P72
LCD_Data0	P47	NC
LCD_Data1	P41	NC
LCD_Data2	P39	NC
LCD_Data3	P35	NC
LCD_Data4	P33	P66
LCD_Data5	P31	P61
LCD_Data6	P29	P59
LCD_Data7	P24	P58

Table 2.1: Pin Assignmnet (UCF) for LCD