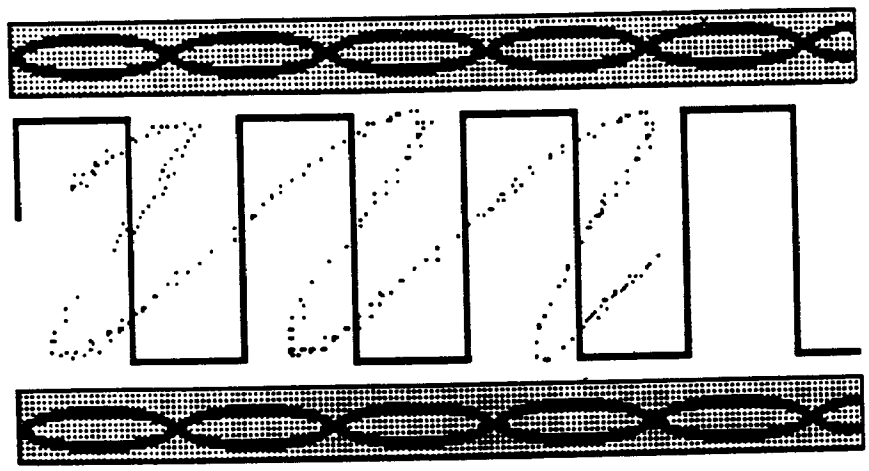
ISDN Burst Transceiver Circuit
IBC

Data Sheet
TM 6/89



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1. Introduction

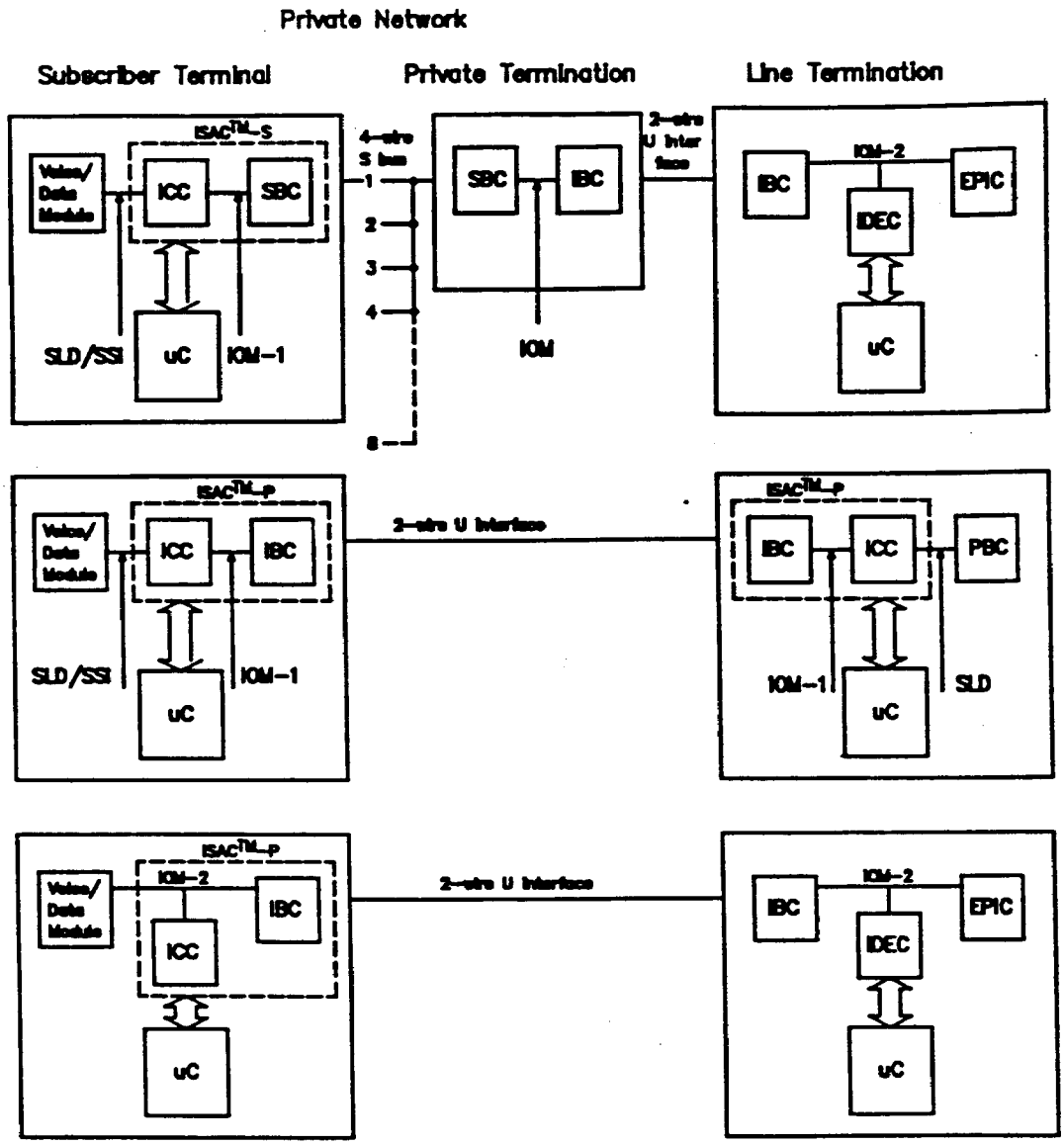
1.1. Device Overview

The PEB 2095 ISDN burst transceiver circuit (IBC) is a full duplex transceiver for the 2-wire transmission line (CCITT U-reference point). Full duplex transmission is achieved using a time compression multiplex (ping-pong) technique. Furthermore the device links the 2-wire transmission line to the ISDN Oriented Modular (IOM™) interface and hence to the powerful Siemens ISDN device family. From the point of view of the OSI Communications Protocol model, the device manages layer 1 of the interface protocol and can communicate with other layer 1 or layer 2 devices over the IOM interface. Figure 1.1 illustrates the possible applications of the IBC within IOM architecture.

As an alternative a second device, PEB 2090 ISDN echo cancellation circuit (IEC), may also be used at the U-reference point. The device chosen depends on the application. The IBC proves more cost -effective for shorter range transmission applications (2 - 3.5 km), especially PABX.

It is available as a 24 pin CMOS device.

The device operates from a single 5 V power supply. The maximum power consumption is 100 mW.



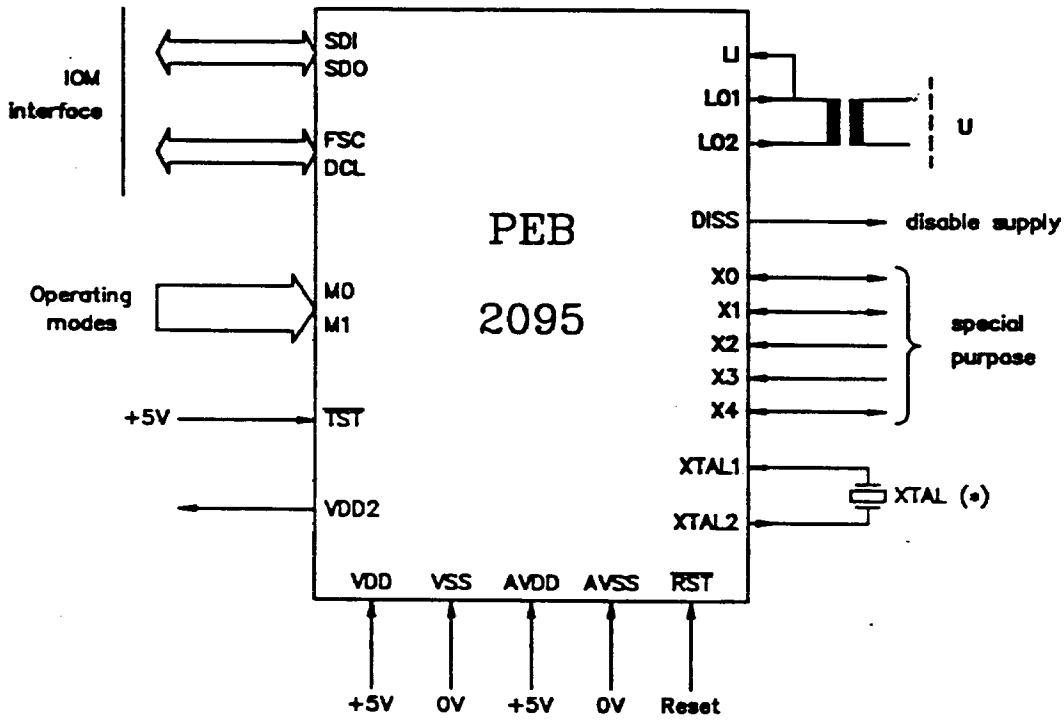
PEB 2050	Peripheral Board Controller	PBC
PEB 2070	ISDN Communication Controller	ICC
PEB 2080	S Bus Interface Circuit	SBC
PEB 2085	ISDN Subscriber Access Controller (S Bus)	ISAC™-S
PEB 2090	ISDN Echo cancellation Circuit	IEC
PEB 2095	ISDN Burst Transceiver Circuit	IBC
PEB 20950	ISDN Subscriber Access Controller (PABX, U Interface)	ISAC™-P
PEB 2055	Enhanced PCM Interface Controller	EPIC™
PEB 2075	ISDN D-channel Exchange Controller	IDEC™

Fig. 1.1: ISDN Oriented Modular (IOM) Architecture

1.2. Features

* Half duplex burst mode 2-wire U-interface transceiver
* Mode configurable to function at both ends of the line
* 144 kbit/s user bit rate (2B + D)
* 384 kHz line clock rate
* IOM-1 and -2 compatible
* Clock and frame recovery
* Adaptive line equalization and amplification at receiver
* Implementation of activation/deactivation procedures
* Built-in wake-up function for activation from power- down state
* Switching of test loops
* Typical length of loop:up to 3.5 km with 0.6 mm diameter wire
* Advanced CMOS technology
* Low power consumption: 13 mW power down
  100 mW power up (maximum)

1.3. Logic Symbol



(*) An external oscillator can also be used as a clock input to XTAL1. In this configuration XTAL2 is not connected.

Fig. 1.2: Logic Symbol of IBC PEB 2095

1.4. Pin Configuration

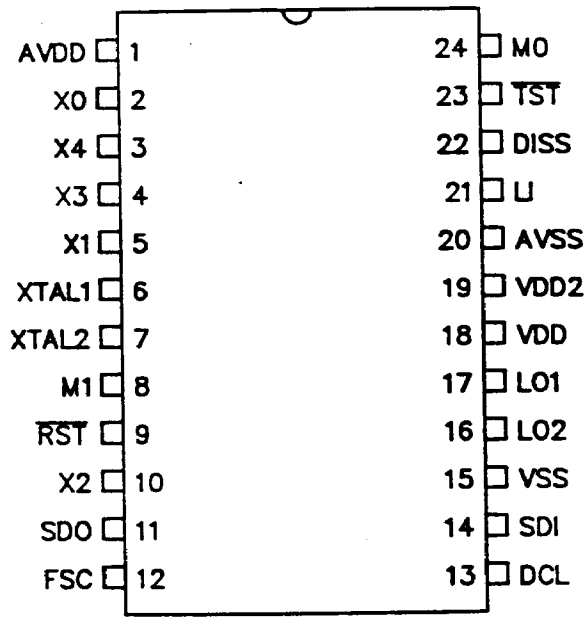


Fig. 1.3: Pin Configuration

SDO,I	- serial data out/in (IOM™)
DCL	- data clock
FSC	- frame synchronization
M0,1	- operating mode
X0,1,2,3,4	- special purpose
XTAL1,2	- external crystal
XTAL1	- external oscillator[1)]
LO1,2	- line transmitter output
LI	- line receiver input
$\overline{TST}$	- device test: tie high
DISS	- disable supply: output
$\overline{RST}$	- reset, active low
VDD	- digital supply
VSS	- digital ground
AVDD	- analog supply
AVSS	- analog ground
VDD2	- reference voltage output

Note [1)] XTAL2 not connected when external oscillator is used

1.5. Functional Block Diagram

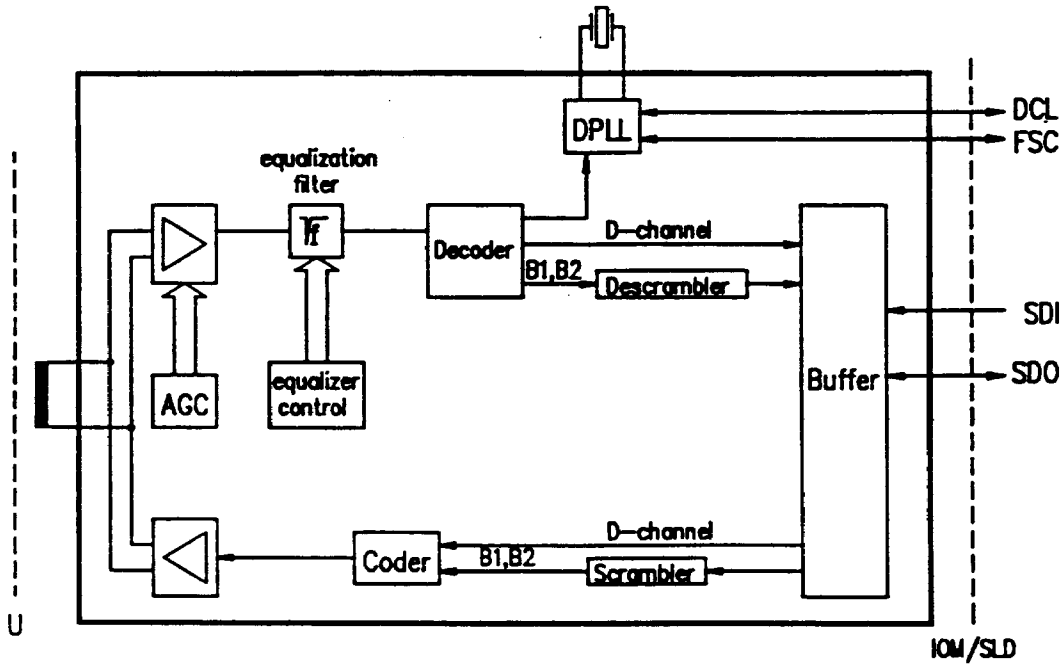


Fig. 1.4: IBC Functional Block Diagram

1.6. System Integration

Figure 1.1 illustrates the uses of the IBC in IOM architecture. These constitute the 3 basic operating modes:

LT: Line Termination i.e. in the Local Exchange/PABX

TE: Terminal Equipment i.e. in the Subscriber Terminal

PT: Private Termination

In Figure 1.5, two examples of LT mode are illustrated, one connected directly to the terminal, one connected to a Private Termination. In the latter case the terminal is connected over the S-interface to the Private Termination. Because of the multiplexing facility on the S-bus up to eight terminals may be connected to one Private Termination and hence to one subscriber line. In the former case (without a Private Termination) only one terminal per subscriber line is possible.

In the LT mode the IBC manages layer 1 functions and communicates over the IOM.interface with the ICC (ISDN Communication Controller) which handles most layer 2 functions. A microprocessor (handling higher layer functions) controls and communicates with the ICC. A similar configuration is required in the TE mode, employing the same division of tasks (Fig. 1.1).

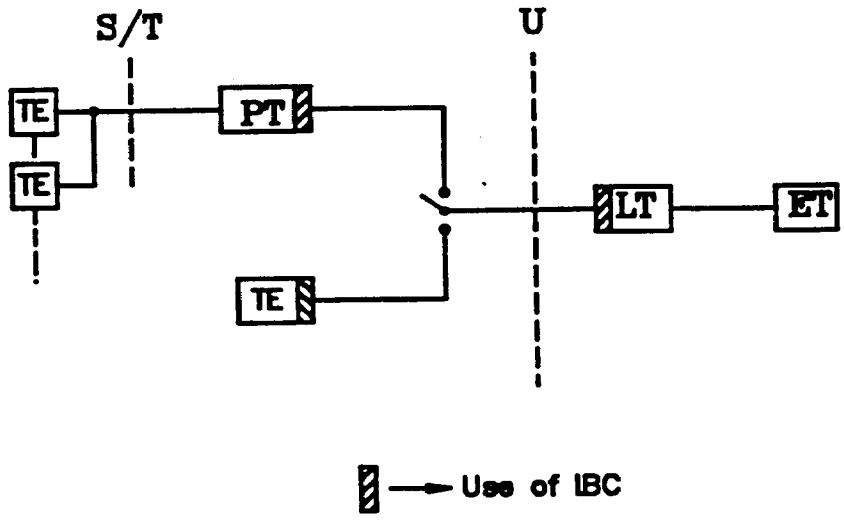


Fig. 1.5: Basic IBC Modes

PT refers to a simple layer 1 translation between the U-interface and the S/T- interface. This is achieved by the simple pairing of the IBC with an IOM compatible S-bus interface circuit (e.g. the SBC PEB 2080), as illustrated in the first example in figure 1.1.

In this configuration no ICC or microprocessor is required because layer 2 and higher are passed transparently through PT. The IOM-interface acts as an intermediate interface common to both devices.

2. Functional Description

2.1. IBC Device Architecture and General Functions

The ISDN burst transceiver circuit (IBC PEB 2095) performs the layer 1 functions of the time-division multiplex implementation of the U-interface. This is a half duplex technique (ping-pong) involving transmission by only one device at any one time. Furthermore the IBC acts a link between the U-interface to the IOM interface and hence to other layer 1 or layer 2 devices within the system. Figure 2.1 depicts the device architecture.

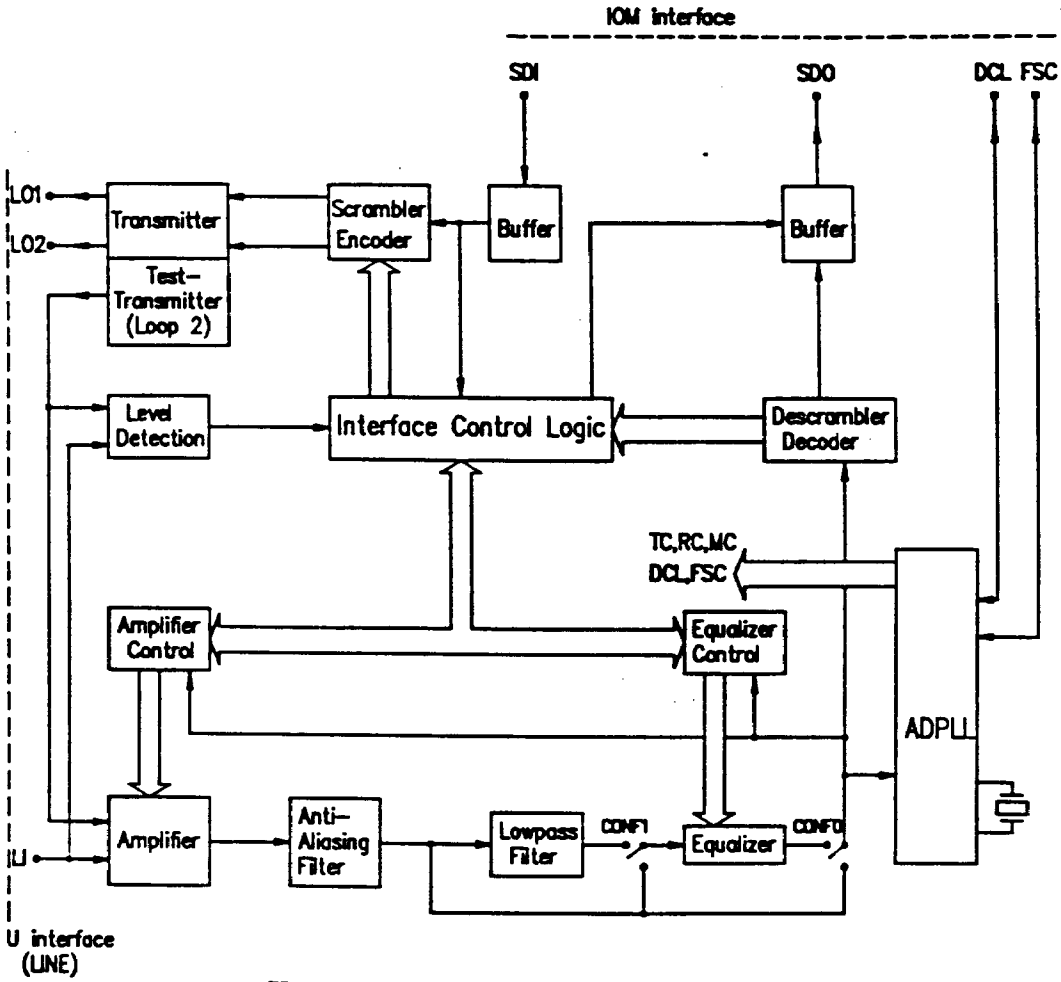


Fig. 2.1: IBC Device Architecture

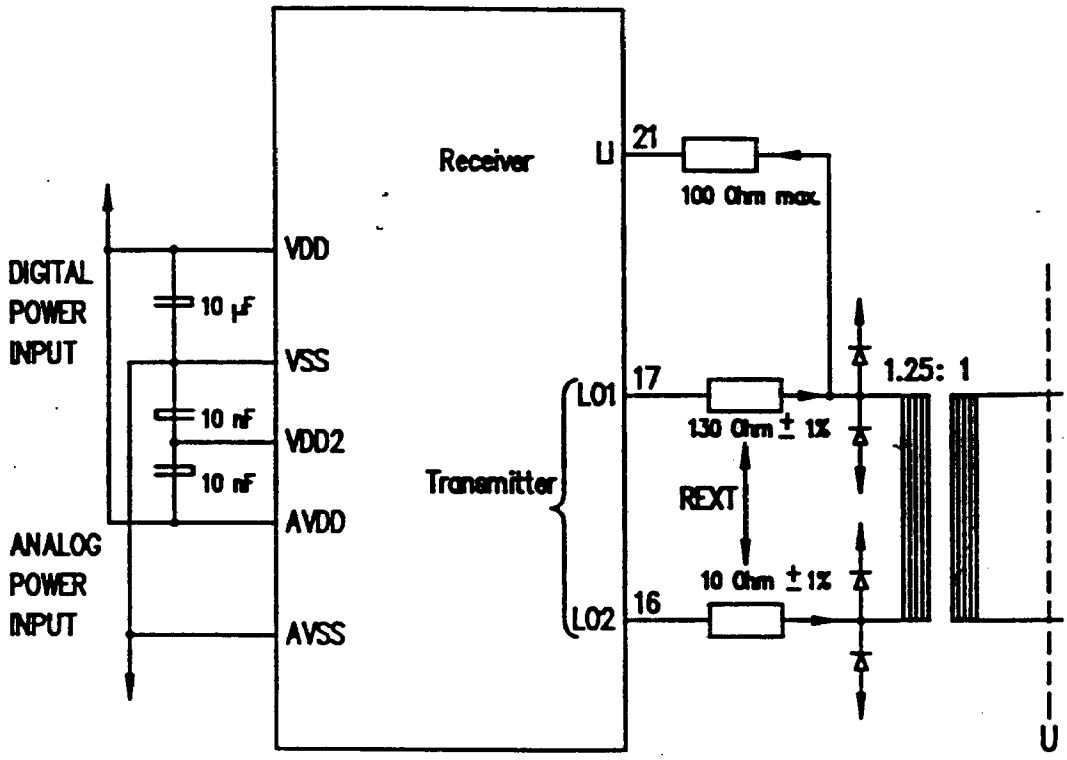
Some of the relationships between the blocks of the device architecture and the IBC functions outlined below can be traced at this stage. This section, however, will deal in more detail with these relationships.

The following are the main functions of the IBC:

- Activation/Deactivation procedures. Activation may be initialised by either infos from the line or primitives from the IOM-interface
- To increase the quality of signal receivedfrom the line, the receiver stage contains both an adaptive amplifier and equalizer
- Synchronous timing must be maintained on both sides of the device. All internal clocks are synchronized to the upstream data clock (system clock). All generated downstream clocks are synchronized, in turn, to these internal clocks.
- Testing and Diagnostic functions: Testloops may be closed, test signals may be generated

Furthermore the IBC must also link 2 contrasting interfaces, the IOM interface and the U-interface. To do this transparently, the IBC must compensate for the following main differences between them:

- The U-interface is a burst mode interface while the IOM-interface is continuous
- The frame structure and data transmission techniques on both interfaces are different
- The B channels are scrambled on the U-interface and unscrambled on the IOM-interface
- The clock rates are different and are transmitted in a different manner. In the U-interface the clock is implicit in the data stream; in the IOM-interface 2 separate clocks, DCL and FSC, must be provided.



Note: VDD2 is a 2.5V reference output

Fig. 2.2: IBC Analog Connections

2.1.1. Analog Functions

Figure 2.2 depicts the analog and power connections to the IBC. Both analog and digital power may be connected to a single power source. The reference voltage VDD2 must be linked by two 10 nF capacitors to VSS and AVDD. External to the transmitter and receiver a transformer (ratio 1.25:1) and external resistance (REXT = 140 Ohms ± 1%) are connected as shown. Voltage overload protection is achieved by splitting REXT into 130 Ohms and 10 Ohms (for current limitation) and adding clamping diodes. If required a resistor (100 Ohm max.) may be added to the line signal input for overvoltage current limitation.

The transmitter stage is realized as a voltage source with an internal resistance Ri = 15 Ohms ± 40%. It delivers a pulse of amplitude 2 V ± 10% (0-to-peak). Assuming a transformer winding resistance of the order of 1 Ohm, the output resistance seen from the U-interface will be 100 Ohms.

Referring again to figure 2.1, the receiver input stages can be seen. They consist of a variable gain amplifier, to compensate for signal losses on the line (dynamic range 30 dB). This is followed by an anti- aliasing filter and a switched capacitor low pass filter. Finally a switched capa-

citor equalizer suppresses the out-of-band noise, which has passed the (anti-aliasing) filter stage, while keeping the pulse distortion low (dynamic range 15.36 dB).

Both the amplifier and the equalizer are adaptive. The amplifier has 128 possible settings and the equalizer 8 (in this sense they are digital). The adaptive logic can be stopped by externally setting the amplifier and equalizer over the IOM interface (cf table4.3). Once set in this way the settings remain constant. The Monitor Channel can also be used to program some other functions.

The level detection block monitors the receive line and informs the interface logic when an incoming signal is present. It also monitors the test transmitter to perform a similar function during test loop implementation.

2.1.2. Digital Functions

The DPLL circuitry works with an external oscillator or crystal of 15.36 MHz ± 100 ppm. This is used to synchronize all bit and frame clocks with the incoming system clock (i.e. from upstream). In the LT mode the system clock is supplied over the IOM-interface. Generation of half-bauded AMI pulses for the line is accomplished by deriving a synchronous transmitter clock using the DPLL. At the PT/TE end of the line the data clock of 384 kHz is implicitly received in the data stream and is extracted by the IBC. From this all synchronous clocks are derived with the aid of the DPLL.

An incorporated finite state machine controls ISDN layer 1 activation/deactivation. This includes wake signal recognition in the "deactivated" state.

Due to the burst nature of U-interface communication and the continuous nature of communication on the IOM-interface a buffer memory is required to compensate for timing differences.

The digital control logic also sets the adaptive coefficients on the AGC amplifier and the SC equalization filter.

2.1.3. Scrambler/Descrambler

B channel data on the U-interface is scrambled to give a flat continuous power density spectrum and to ensure enough pulses are present on the line for a reliable clock extraction to be performed at the downstream end.

The IBC therefore, contains a scrambler and descrambler, in the transmit and receive directions respectively. The basic form of these are illustrated in Fig. 2.3 and Fig. 2.4.

The form is in accordance with the CCITT V.27 scrambler/descrambler and contains supervisory circuitry which ensures no periodic patterns appear on the line.

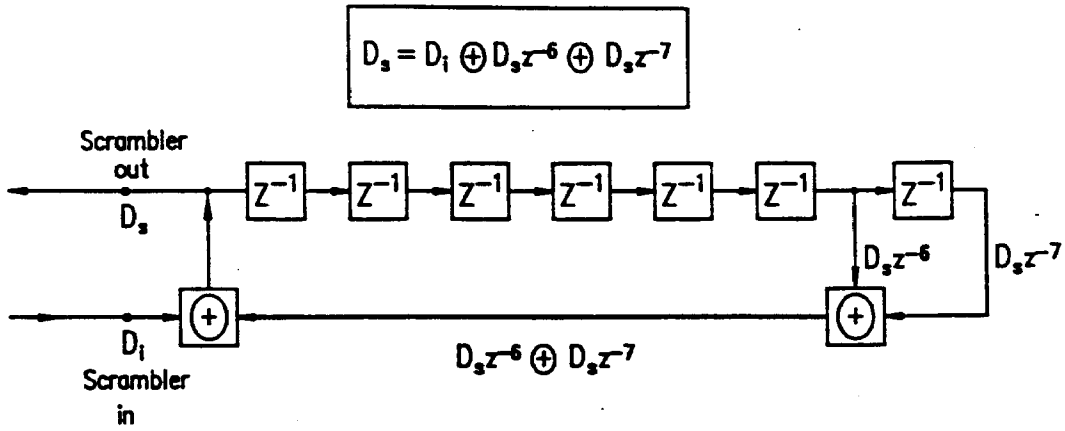


Fig. 2.3: IBC Scrambler

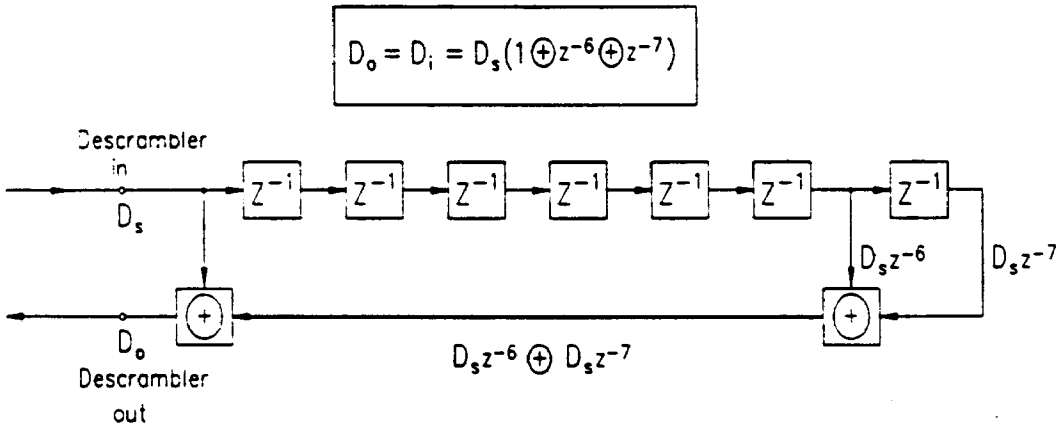


Fig. 2.4: IBC Descrambler

2.2. Interfaces

The IBC operates 2 interfaces:

- U-interface
- IOM-interface

2.2.1. U-interface

Figure 2.5 demonstrates the general principles of the U-interface burst mode communication technique. A frame transmitted by the exchange (LT) is received by the terminal equipment (TE) after a given propagation delay. The terminal equipment waits a minimum guard time (5.2 µs) while the line clears. It then transmits a frame to the exchange. The exchange will begin a transmission every 250 µs (known as the burst repetition period). However, the time between the reception of a frame from the TE and the beginning of transmission of the next frame by the LT must be greater than the minimum guard time. Communication between an LT and a PT follows the exact same procedure.

Within a burst, the data rate is 384 kbit/s and the 38 bit frame structure is as shown in figure 2.5. The framing bit (LF) is always logical '1'. The frame also contains the user channels (2B + D). Note that the B channels are scrambled. It can readily be seen that in the 250 µs burst repetition period, 4 D bits, 16 B1 bits and 16 B2 bits are transferred in each direction. This gives an effective full duplex data rate of 16 kbit/s for the D channel and 64 kbit/s for each B channel.

The final bit of the frame is called the M bit. Four successive M bits, from four successive U-frames, constitute a superframe (figure 2.5). Three signals are carried in this superframe. Every fourth M bit is a code violation (CV) and is used for superframe synchronization. This can be regarded as the first bit of the superframe. From this reference, bit 3 of the superframe is the service channel bit (S). The S channel bit is transmitted once in each direction in every fourth burst repetition period. Hence the duplex S channel has a data rate of 1 kbit/s. It conveys test loop control information from the LT to the TE/PT and reports of transmission errors from the TE/PT to the LT. Bit 2 and bit 4 of the superframe are T bits. These constitute the 2 kbit/s T channel which extends the T channel of the IOM frame (figure 2.8) onto the U-interface.

In order to decrease DC offset voltage on the line after transmission of a CV in the M bit position, it is allowed to add a DC balancing bit to the burst. The IBC transmits this DC balancing bit in LT-mode, when transmitting INFO 4, and when line characteristics indicate potential decrease in performance. However this DC balancing bit may generally be switched on by programming CONF1 to ZERO (cf. 4.2).

Note that the guard time in TE is always defined with respect to the M bit, whereas AMI coding includes always all bits going in the same direction.

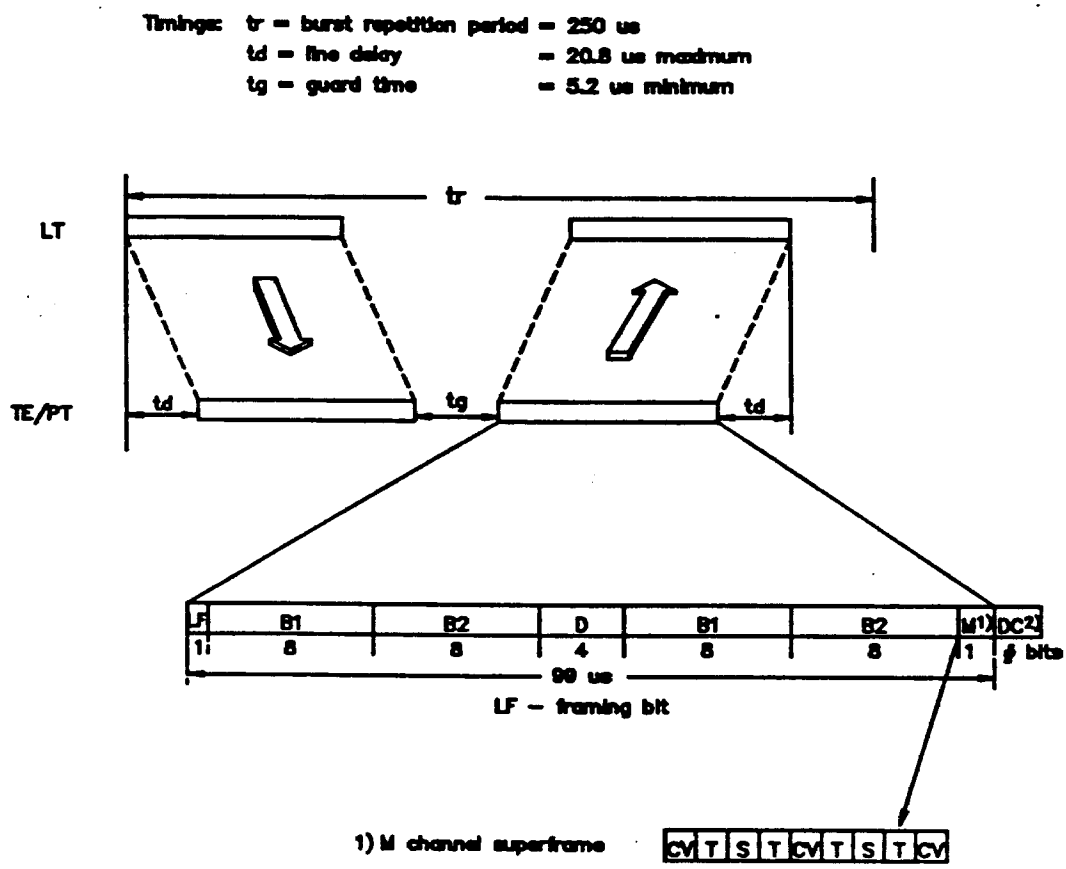


Fig. 2.5: U-Interface Transmission/Reception

The coding technique used on the U-interface is half-bauded AMI code (i.e. with a 50% pulse width). Figure 2.6 illustrates the code. As can be seen, a logical '0' corresponds to a neutral level, a logical '1' is coded as alternate positive and negative pulses. The figure also illustrates how a code violation may beachieved (CV); either two successive positive (as shown) or negative pulses.

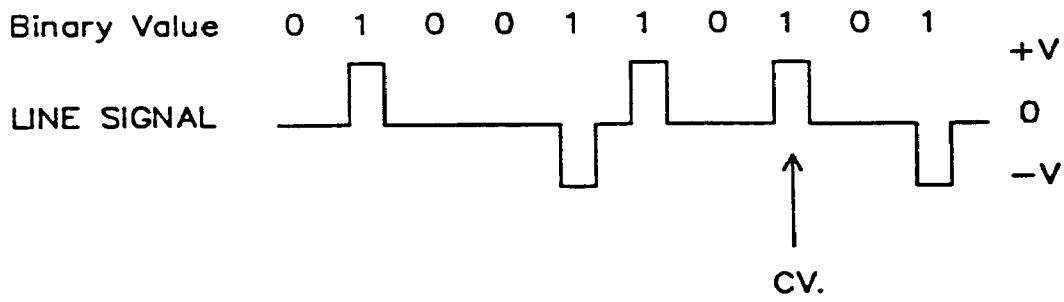


Fig. 2.6: Half-Bauded AMI Code

2.2.2. IOM-Interface

The IBC is provided with a digital interface, the IOM™ interface, for communication with other ISDN devices, in other words with units realizing OSI layer 1 functions (such as the ISDN S-bus Transceiver SBC PEB 2080) or layer 2 functions (such as the ISDN Communication Controller ICC PEB 2070). (See Fig. 2.7)

The IOM-interface consists of 2 clocks; DCL (data clock) and FSC (Framd Synchronization Clock), and 2 data lines; data out and data in. The data in both directions is synchronous and in-phase.

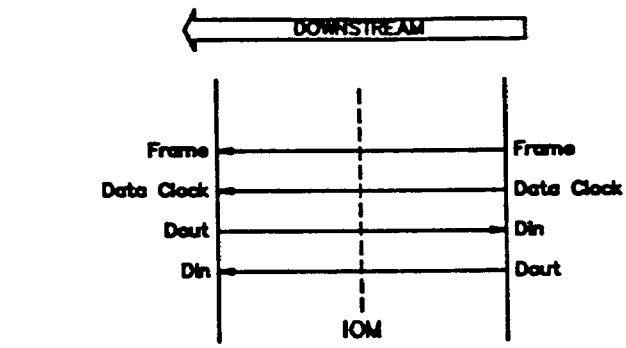


Fig. 2.7: IOM-Interface of IBC

The IOM frame structure is illustrated below. It contains the 2B + D channels, transmitted transparently over the interface at 144 kbit/s. In addition, it is necessary to interchange control information for activation and deactivation of OSI layer 1, for switching of test loops etc. This is transfered through the so-called B* channel. The B* channel is in fact made up of four channels:

- D: The D channel (2 bits)
- C/I: The Command and Indication Channel (4 bits) is used to convey control information across the IOM-interface. This information refers directly to OSI model layer 1 - layer 2 communication. Chapter 4 lists the possible C/I codes.
- T: The "Transparent" bit
- MX: The "Monitor Transmit" bit

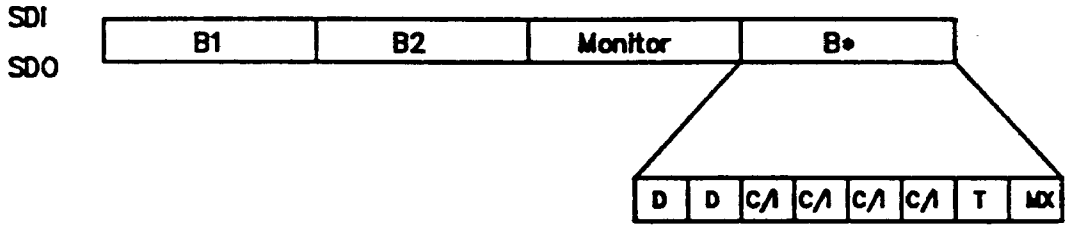


Fig. 2.8: IOM Frame Structure

The 8 bit monitor channel handles information exchange between the layer 2 and layer 1 devices not covered by OSI e.g. AGC coefficient setting. Its use, however, may be restricted by the ICC MODE register's configuration. For a complete description of available monitor codes and their use, refer to section 4.

Section 1.6 outlined the three basic operating modes of the IBC (LT, TE and PT) and their relationship to the system architecture. But, as will be seen, the IBC has seven operating modes. This is due to the existance of timing modes:

- IOM1 Mode
- IOM2 Mode
- Inverted Mode.

The different modes only effect the timing of the IOM interface and will now be discussed in detail. Section 2.3 will describe the seven operating modes in more detail.

2.2.2.1. IOM-1 Mode

This timing mode is applicable in all three basic operating modes of the IBC.

Nominal bit rate of data (SDI and SDO):	256 kbit/s
Nominal frequency of DCL:	512 kHz
Nominal frequency of FSC:	8 kHz

Transitions of the data occur after even-numbered rising edges of DCL. Even-numbered rising edges of the clock are defined as the second rising edge following the rising edge of FSC and every second rising edge thereafter.

The frame is earmarked by the rising edge of FSC. Figure 2.9 shows the position of the IOM frame with respect to the clocks.

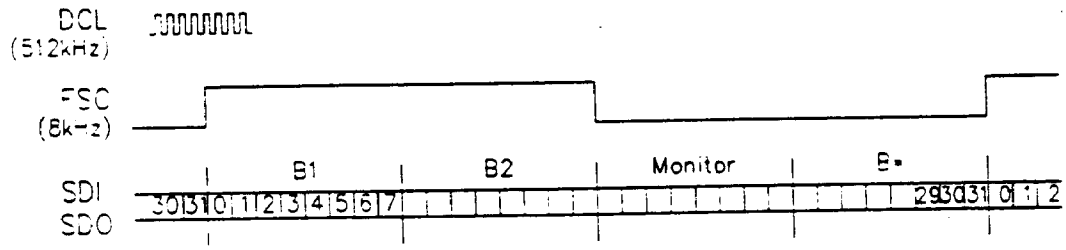


Fig. 2.9: Timing of Data and Clocks of IOM in the IOM-1 Mode

2.2.2.2. IOM-2 Mode

This timing mode is applicable only in TE and LT operating modes.

Nominal bit rate of data bursts (SDI and SDO)	2048 kbit/sec in LT mode 768 kbit/sec in TE mode
Nominal frequency of DCL	4096 kHz in LT mode 1536 kHz in TE mode
Nominal frequency of FSC	8 kHz

The data at the input SDI is valid on the odd-numbered falling edges of DCL. Transitions of the data on SDO occur after even-numbered rising edges of DCL. The rising edge earmarked by the frame strobe is an even- numbered rising edge of DCL. The following falling edge is an even-numbered falling edge.

The IBC sends an IOM frame in the form of a burst, 1/8 or 1/3 of an FSC period long. Hence, in LT application up to 8 IBCs can be multiplexed on the SDO and SDI lines. Each IBC is allocated a time slot, by the static inputs X0(TS0), X1(TS1) and X2(TS2). The IBC will both transmit and receive data in this time slot. Table 2.1 indicates the allocations.

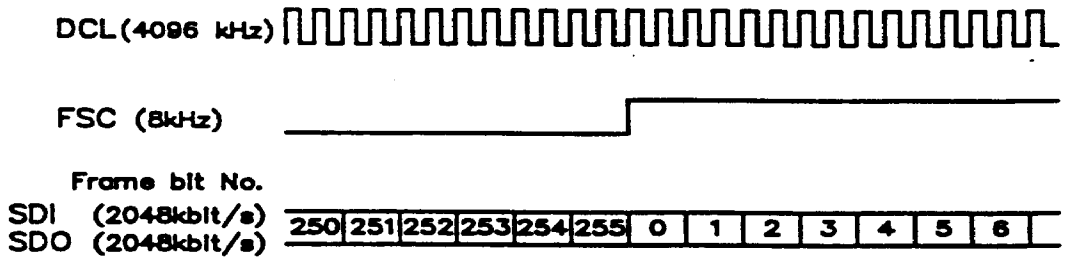


Fig. 2.10: Timing of Data and Clocks of IOM in the IOM-2 Mode

Time slot no.	TS2	TS1	TS0	bit. no.		
0	0	0	0	0	...	31
1	0	0	1	32	...	63
2	0	1	0	64	...	95
3	0	1	1	96	...	127
4	1	0	0	128	...	159
5	1	0	1	160	...	191
6	1	1	0	192	...	223
7	1	1	1	224	...	255

Tab. 2.1: Allocation of Time Slots

In TE mode, the IBC uses the first third of the FSC period to transmit the 256 kbit/s. The remaining two thirds of the period can be used by other devices.

2.2.2.3. Inverted Mode

This timing mode is only applicable in TE and LT operating modes.

Nominal bit rate of data bursts (SDI and SDO) — 2048 kbit/sec in LT mode; 256 kbit/sec in TE mode

FSC is not a signal with 50% duty cycle but rather an active low pulse, one DCL clock period long, which occurs in the middle of the fourth bit of B*, of the last 256 kbit/sec channel of a frame.

Transitions of data occur after even-numbered falling edges of DCL. Even-numbered falling edges are defined as the second falling edge following the rising edge of FSC and every second falling edge thereafter.

2.3. Operating Modes

The IBC may be configured for 3 basic operating modes.

- TE mode: ISDN terminals
- PT mode: ISDN Private Termination
- LT mode: ISDN Line Termination

Furthermore in each of these operating modes further timing mode possibilities may be open (see 2.2.2.).

Configuration is achieved by pinstrapping (pins M0, M1 and sometimes X2). Both the IOM clock signals (DCL, FSC) and the multifunctional pins (X0, X1, X2, X3) have mode dependent functions (refer table 2.2).

	application						
	TE	TE	TE	PT	LT	LT	LT
operation of IOM interface	inverted mode	IOM-1 mode	IOM-2 mode	normal mode	IOM-1 mode	inverted mode	IOM-2 mode
M1 M0	0 0	0 0	0 RST	0 1	1 0	1 1	1 1
DCL	o:512kHz* 1:1	o:512kHz* 1:1	o:1.536 MHz* 1:1	o:512kHz* 1:1	i:512kHz	i:4096kHz	i:4096kHz
FSC	o:8kHz* 63:1	o:8kHz* 1:1	o:8kHz 1:2	o:8kHz* 1:1	i:8kHz	i:8kHz 511:1	i:8kHz
X4	o:2.56MHz 1:2 o:7.68MHz* 1:1	o:2.56MHz 1:2 o:768MHz* 1:1	o:2.5MHz 1:2 o:7.68MHz* 1:1	o:7.68MHz* 1:1	i:PFOFF	i:PFOFF	i:PFOFF
X3	i:$\overline{\text{ENCK}}$	i:$\overline{\text{ENCK}}$	i:$\overline{\text{ENCK}}$	i:$\overline{\text{ENCK}}$	i:MPF	i:MPF	i:MPF
X2	i:1	i:0	i:0	i:$\overline{\text{SCP}}$	i:0	i:TS2	i:TS2
X1	o:1.536MHz *1:1	o:1.536MHz* 1:1	o:768kHz* 1:1	i:$\overline{\text{SSP}}$	o:15.36MHz 1:1	i:TS1	i:TS1
X0	o:3.84MHz	o:3.84MHz	o:3.84MHz	i:1	o:CONF4	i:TSO	i:TSO

*: synchronized to U i: = input o: = output

Tab 2.2: IBC Operation Modes and Mode Specific Pin Configurations

Notes:

1. SDI-(IOM-interface)
   - the pin is connected to an internal pull-up resistor in TE and LT IOM-1 modes.
2. SDO -(IOM-interface)
   - open drain output in IOM-2 modes and LT inverted mode.
   - open drain output with internal pull- up resistor in PT-mode
   - push-pull otherwise
3. The following clock outputs are derived from the 15.36 MHz crystal/external oscillator:(i.e. unsynchronized)

   15.36 MHz
   3.84 MHz
   2.56 MHz

4. The following clock outputs are synchronized to the line

   7.68 MHz
   1.536 MHz
   768 kHz
   512 kHz
   8 kHz

5. Switching from 2.56 MHz output at pin X4 in TE mode is done by programming CONF to zero.
6. Distinction between LT IOM-2 and LT inverted mode is performed automatically, dependant on the FSC signal delivered. Distinction between TE IOM-1 and TE IOM-2 mode is performed using the rising edge of the RST-signal to sample the M0 input. During RST = Low, the IBC is always in IOM-1 mode.

Figure 2.11 illustrates how all operating modes may be applied. Note that the figures given within brackets refer to the mode quoted in brackets (e.g. DCL = 4096 kHz refers to the LT-Mode: IOM interface multiplex).

In all modes the system clocking is supplied by the upstream device to the downstream device. Hence, in some modes, the IBC provides DCL and FSC and in others, it receives DCL and FSC externally.

The multifunctional pins are also mode dependent and can be seen as having the following functions:

- auxiliary mode selection (X2 only)
- auxiliary input pins (Table 5.5)
- auxiliary clock outputs (some synchronizd to the line, some not)

The clock outputs act as external oscillators for other devices. For example in figure 2.11 (PT Mode), the SBC uses the 7.68 MHz synchronized output from the IBC as an external oscillator. Further possible applications include:

- 15.36 MHz (LT) - external oscillator for other IBCs
- 1.536 MHz (TE) - CODEC clock supply
- 768 kHz (TE) - single bit clock for IOM-2 interface slave devices

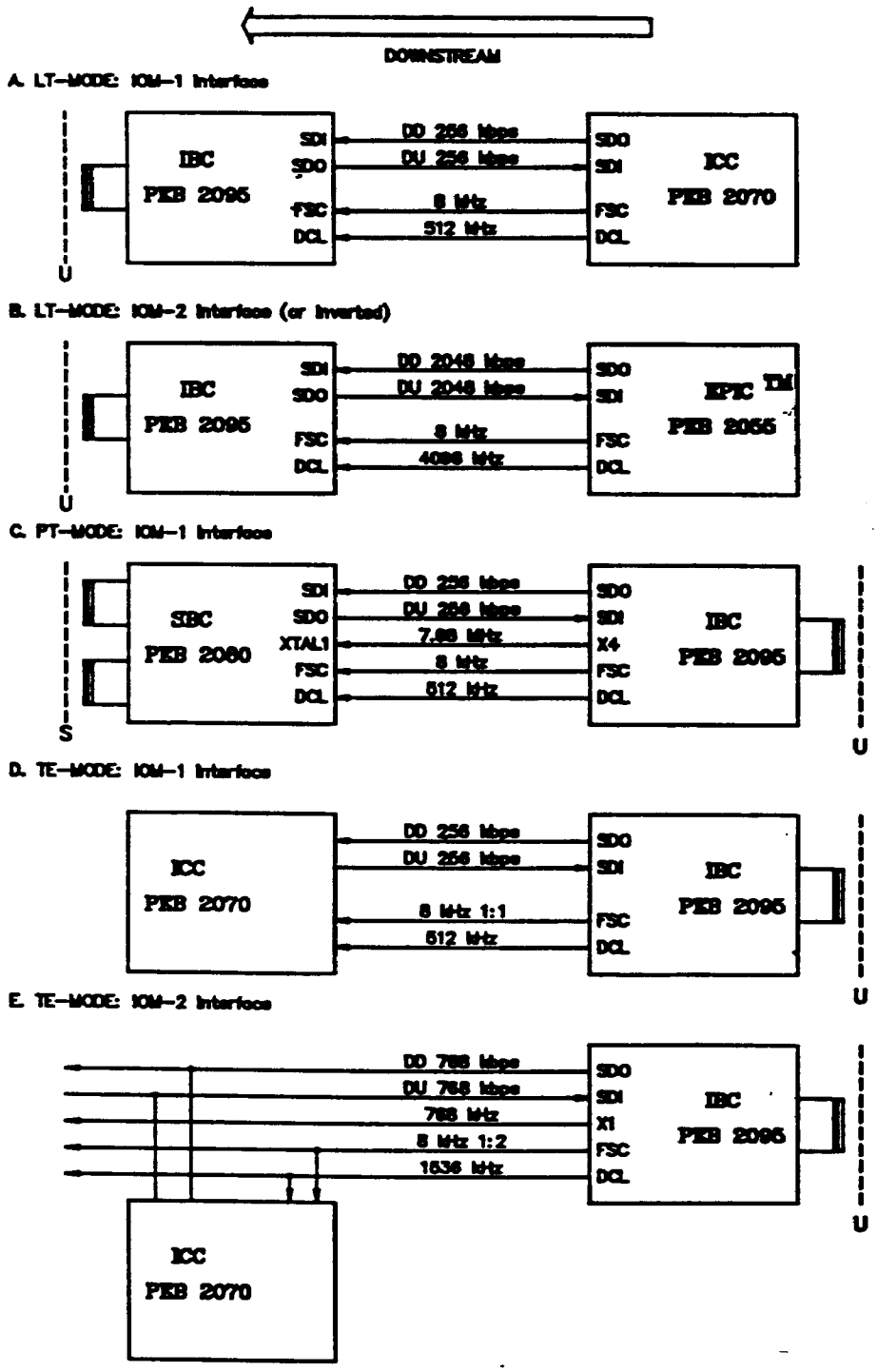


Fig. 2.11: IBC Applications

2.4. Test Functions

2.4.1. Test Loops

Three types of test loops may be closed in the IBC, depending on the operating mode. In all test loops, all 3 channels B1, B2 and D are looped back. In a "Transparent" loop the data is sent forward unmodified as well as being looped back. In a "non-transparent" loop the forward data path is blocked. In both cases, however, the incoming data path is blocked and only the looped data is received.

Figure 2.12 illustrates these test loop configurations and also shows where in the system test loops would occur.

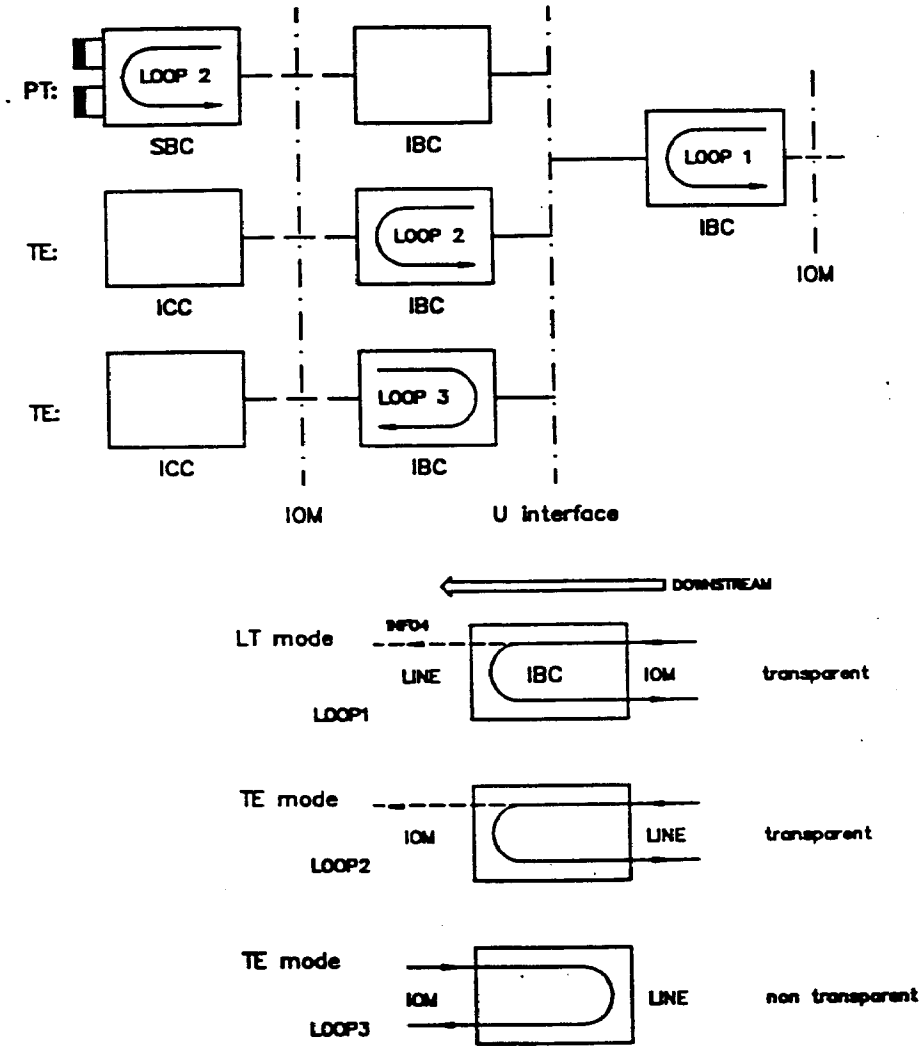


Fig. 2.12: IBC Test Loops

Loop 1 and loop 3 are closed in the IBC itself, as close as possible to the line input/output. However activation of these loops will proceed normally whether the line is actually present or not. Loop 2 in the TE mode is closed within the IBC as close as possible to the IOM interface.

Both loop 1 and loop 3 are local loops, initiated by the local layer 2 device (ICC in Fig. 2.12) with an activate local loop command. In loop 1 all line signals are ignored but the looped infos are transmitted on the line simultaneously. In loop 3 the IBC doesn't transmit any looped data. It does however monitor the line and reports the presence of any signal to the layer 2 device by means of a RSYD indication. Only the layer 2 device can terminate the looping condition.

Loop 2 is initiated by the LT. Section 3 explains the activation of the U-interface by the LT both with and without loop 2. The S-bit (service bit) on U-interface frame, sent by the LT, determines whether loop 2 is requested (S = 1) or not (S = 0). If the downstream IBC is in TE mode then it will activate loop 2 while S = 1. If the downstream IBC is in PT mode it does not have a loop 2 mode. In this case, loop 2 should be closed as close as possible to the S-interface within the S-bus Transceiver Circuit (the SBC in Fig. 2.12). Hence, the presence of S = 1 during U-interface activation will cause the PT IBC to send an activate loop 2 request to the SBC which causes the latter to close the loop.

2.4.2. Test Signals

Two test signals can be sent by the IBC; send continuous pulses (also known as Test Mode 1) and send single pulses (Test Mode 2). In both cases half-bauded AMI coding is used, but only one of the IBCs at either end of the U-interface line transmits. Hence burst mode transmission is abandoned. In the first case a one is transmitted at 384 kbit/s. However, because of the alternate positive-negative nature of the coding, the signal on the line has a frequency of 192 kHz. In the second case, a one is transmitted at 4 kbit/s, yielding a signal of 2 kHz on the line.

2.4.3. Code Violation Monitoring

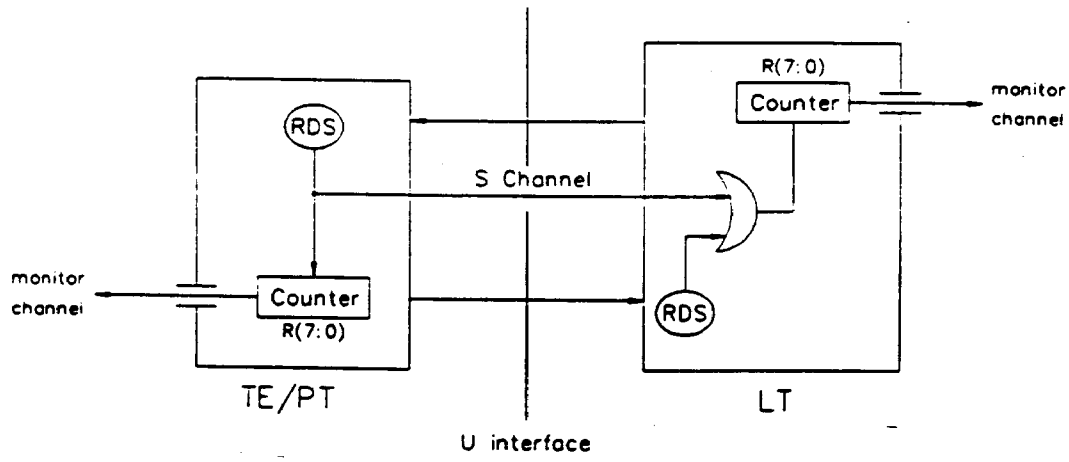


Fig. 2.13: RDS: Running Digital Sum Operation

Once synchronization has been achieved, code violations are monitored on the line. This is achieved by means of the Running Digital Sum (RDS). The RDS is enabled in the synchronized state when the LT indication is RDS and the TE/PT indication is ARD. Both the code violation in the framing bit of info 1 and info 2 and the one used for superframe synchronization are ignored by the RDS (since they don't constitute errors).

In the TE/PT the RDS updates a counter (R7:0) every 1ms; incrementing it if an error has occured in that period. Similarly in the LT the RDS monitors the incoming signal and updates a counter. This update is OR'ed with the S bit of the U-interface frame which contains the TE/PT update. Hence, the TE/PT counter indicates code violations from the LT to TE/PT and the LT counter indicates code violations in both directions. Note that because of the low frequency of the update neither counter contains an error count, only an indication that errors have occured. If the count reaches 255 (the maximum) it does not reset. It is reset only after a hardware/software reset or after the register itself is read. The counter is accessible over the Monitor Channel in all modes.

2.5. Power Supply Monitoring

In LT modes the IBC can be used to monitor and control the power supply. In effect the IBC stands between the power supply and the higher OSI layer devices and through it the higher layers control the power supply. However the power supply must be able to communicate with the IBC in the following manner:

Pin X3, on the IBC, functions as the MPF (main power feed) pin in LT modes. A "supply current equivalent" byte derived from the power supply can be read into register I(7:0) through the MPF pin. This read is synchronous to the B1 channel of the IOM frame (in time slot 0 if LT mux mode is used). The I(7:0) register can in turn be read by the ICC over the monitor channel. The ICC can use the information it contains to control the power supply. If the current value is too high the software issues a DIS command. Pin DISS on the IBC goes high and, if properly connected, this pin can be used to disable the power supply. The IBC then goes into a reset state. If the power feed device is disabled either by DISS or by some overload condition (short circuit) it indicates this to the IBC by putting pin PFOFF on high. The IBC hands this information over to layer 2 device by putting the HI indication in the C/I channel.

The full operation of DISS pin in the LT mode is governed by the following conditions:

DISS: output set = DIS + Hardware Reset.
DISS: output reset = Software Reset.

It acts as a flipflop output, once set it remains set until the occurance of one of the reset conditions. In the TE and NT modes a high on pin DISS indicates that the device is in the deactivated state and that the IOM clocks are disabled.

Some or all of the above functions may be employed depending upon requirements. Alternatively Siemens also produce a power controller for the LT which can be directly controlled by a microprocessor (PEB 2025, the ISDN Exchange Power Controller).

3. Operational Description

3.1. Internal State Machine

The internal finite state machine of the IBC controls the activation/deactivation procedures, switching of test loops and transmission of special pulse patterns. Such actions can be initiated by signals on the U transmission line (info's) or by control (C/I) codes sent over the IOM interface.

Once initiated such procedures normally involve passing through several states. Each successive state is entered on receiving a particular info (U-interface) or command (IOM-interface) and results in a particular info (U-interface) or indication (IOM-interface) being transmitted.

In the IBC there are three possible state machines corresponding to the three basic operating modes: LT, TE and PT. In this section the interworkings of these mode dependant state machines will be focused on in detail.

Section 4.1 lists the codes corresponding to the various commands and indications refered to in this chapter.

3.1.1. Info Structure

The signals controlling the internal state machine on the U-interface are called infos. In effect, these pass information regarding the status of the sending IBC to the IBC at the other end of the line. They are based upon the same format as the U-interface frames described in section 2.2.1 and their precise form is shown in table 3.1.

When the line is deactivated info 0 is exchanged by the IBCs at either end of the line. Info 0 effectively means there is no signal sent on the line in either direction.

When the line is activated info 3 upstream and info 4 downstream are continually exchanged. Both info 3 and info 4 are effectively normal U-interface data frames containing user data and exchanged in normal burst mode.

Note that the structure of info1 and info2 are the same, they only differ in the direction of transmission. Similarily info 3/info 4 and info 1w/info 2w also constitute info pairs. This will be important when considering looped states.

As we will see, the other infos are exchanged during the various states which occur between activation and deactivation of the line.

NAME	DIRECTION	DESCRIPTION
info 0	Upstream Downstream	No signal on the line
info 1W	Upstream	Asynchronous Wake Signal 2 kHz burst rate F000100010001000100010101010001011111 1 Code violation in the framing bit (F)
info 1	Upstream	4 kHz burst rate F000100010001000100010101010001011111M [1] DC [2] Code violation in the framing bit
info 2W	Downstream	Synchronous Wake Signal 2kHz burst rate F000100010001000100010101010001011111 1 Code violation in the framing bit Only used for loop 1
info 2	Downstream	4 kHz burst rate F000100010001000100010101010001011111M [1] DC [2] Code violation in the framing bit
info 3	Upstream	4 kHz burst rate No code violation in the framing bit User data in B, D and M channels B channels scrambled, DC-bit [2] optional
info 4	Downstream	4 kHz burst rate No code violation in the framing bit User data in B, D and M channels B channels scrambled, DC-bit [2] optional

Notes: 1) The M channel superframe is semitransparent:
S bits transparent [1kbps channel]
T bits set to one [2kbps channel]

2) DC balancing bit

Tab. 3.1: U-Interface Info Signals

3.1.2. State Diagrams

The state diagrams (Figures 3.2 to 3.5) describe and define the state machine for each of the modes in an easily understandable manner.

Figure 3.1 illustrates the notation used

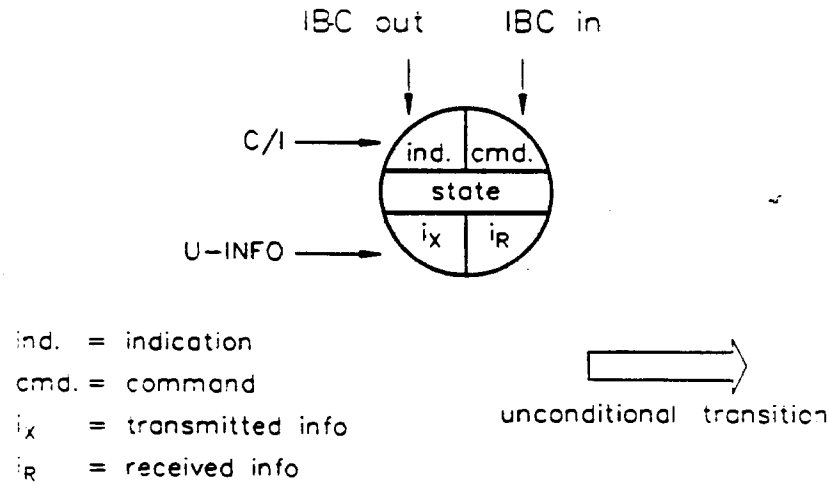
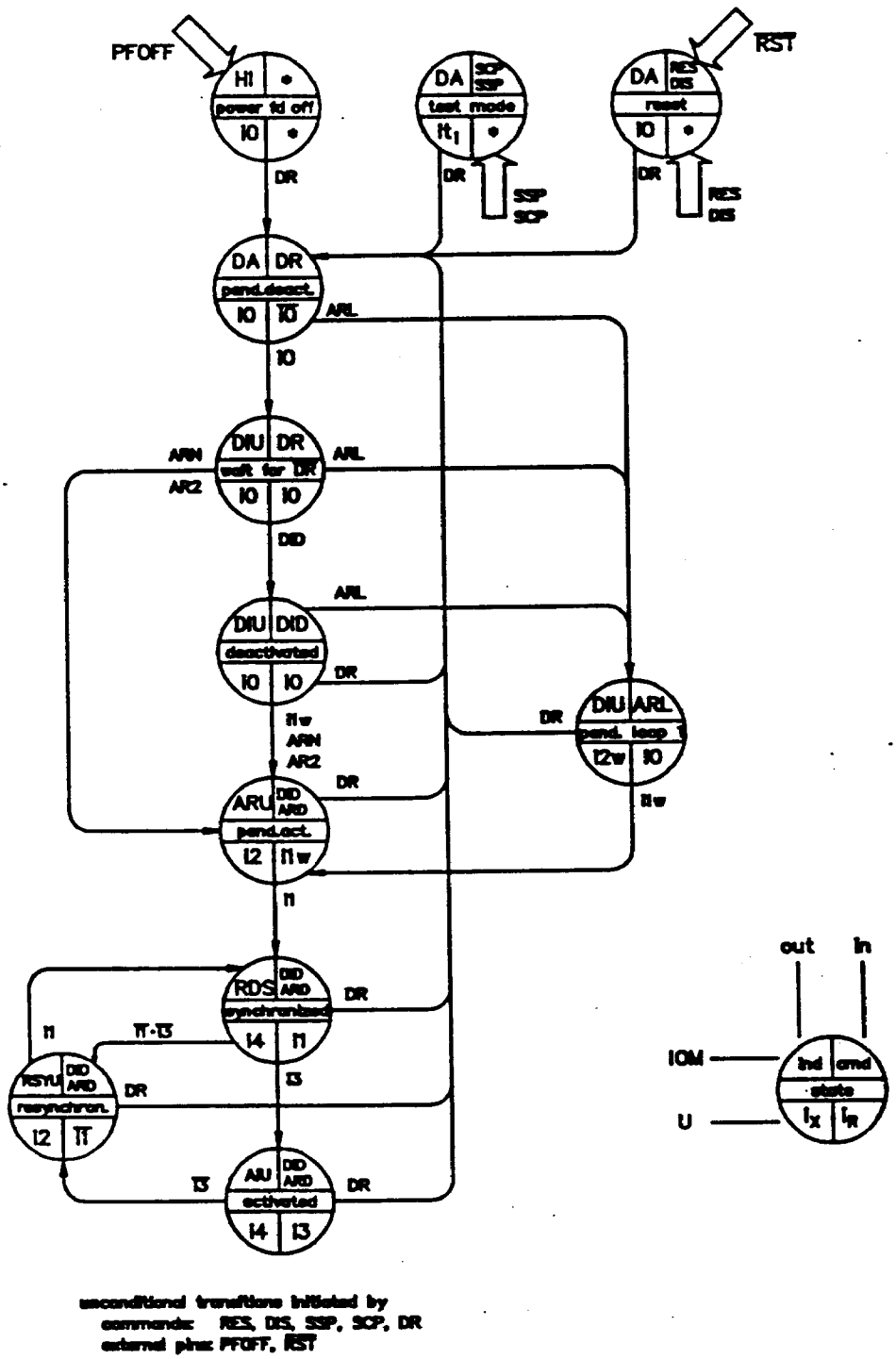


Fig. 3.1: State Diagram Format

When in a particular state, the IBC will continually output the relevent C/I indication and info. When considering the inputted C/I command the IBC operates a double last look criterion. This means that a new code is only considered valid if it is found in two consecutive IOM frames.

Finally for each mode there are some events which cause unconditional transitions to some particular state, regardless of the current state. Such an event may be a specific C/I Command or an active signal being present on an external pin.

A detailed description of the state machine for each of the modes now follows:



unconditional transitions initiated by
commands: RES, DIS, SSP, SCP, DR
external pins: PFOFF, RST

Fig. 3.2: LT State Diagram

3.1.2.1. **LT mode**

Refer to figure 3.2 (State Diagram)

Unconditional States:

Reset

This state is entered unconditionally after a low appears on the $\overline{RST}$ pin or after the receipt of command RES (software reset) or DIS (disable power supply). The analog section is disabled (transmission of info 0) and the U-interface awake detector is inactive. Hence, activation from PT or TE is not possible.

Test Mode

The test signal (it_i), sent to the U-interface in this state, is dependant on the command which originally invoked the state. SSP causes single alternating pulses to be transmitted (it_2); SCP causes continuous alternating pulses to be transmitted (it_1) (For signal description see section 2.4.2). The burst mode technique normally employed on the U-interface, is suspended in this state and the test signals are transmitted continuously.

Power Feed Off

When a high appears on the PFOFF external pin the phantom power supply is switched to high impedance. This is indicated to the layer 2 device by a HI indication.

Pending Deactivation

To access any of the conditional states from any of the above unconditional states the pending deactivation state must be entered. This occurs after the receipt of a DR command. In this state the awake detector is activated and the state is exited only when the line has settled (i.e. info 0 has been detected for 2ms).

Although , for clarity, DR is shown as a normal command it is in fact an unconditional command: No matter which state the LT is in, the reception of a DR command will always result in the pending deactivation state being entered.

Conditional States:

Pending Loop 1

The receipt of ARL (activate request local loop) when in either the deactivated state, the pending deactivated state or the wait for DR state causes this state to be entered. Info 2w is sent out on the line and also looped back into the receiver where eventually it is recognized as info 1w (i.e. the format is the same, the direction has simply changed). From here the IBC moves into the pending activation state. The loop however remains closed and, hence, every info sent will become its own response and the device will self- activate. Note that the trans-

mitted infos also appear on the line itself.

Wait for $\overline{DR}$

This state is entered from the pending deactivation state once info 0 has been identified. From here the line may be either activated, deactivated or a test loop may be entered.

Deactivated

This is the power down state of the physical protocol. Power consumption is cut to a minimum. The awake detection is active and the device will respond to an info 1w (wake signal) by initiating activation.

Pending activation

This state results from a request for activation of the line, either from the terminal (info 1w) or from the layer 2 device (ARN or AR2). In the case of info1w a delay of 1.5 ms is implemented before this state is entered to allow error-free level detect and prevent accidental activation. Info 2 is then transmitted and the LT waits for the responding info 1 from the remote device.

Synchronized

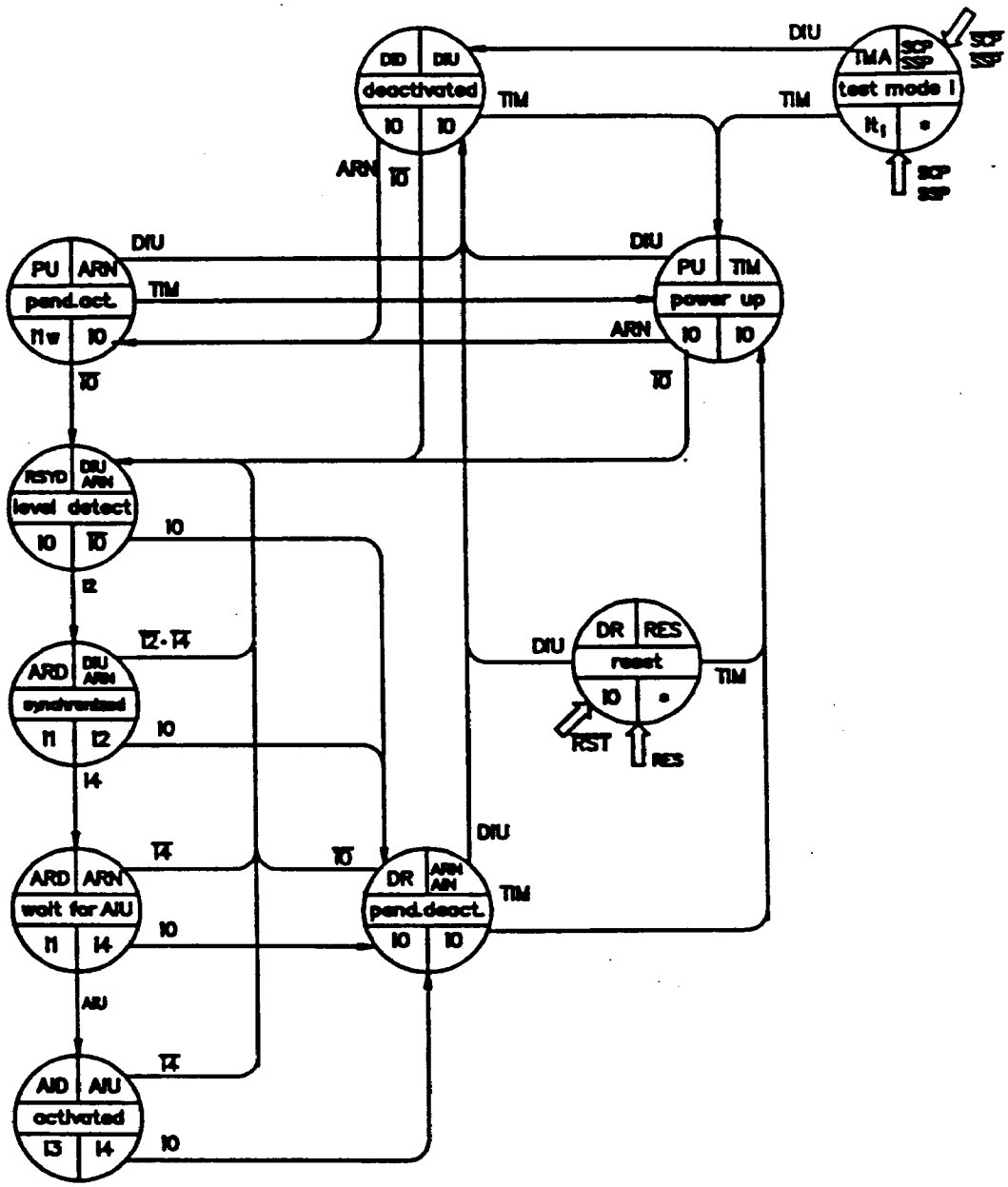
Upon receipt of info 1 the LT must synchronize itself to the signal. To this end, both the equalizer and gain settings adapt to improve the quality of the incoming signal. This process takes at most 80 ms after which the LT supplies info 2 to the remote. The remote then synchronizes to the LT.

Activated

Info 1 has a code violation in the framing bit (F-bit) whereas info 3 has none. Upon the receipt of 2 frames without a code violation in the F-bit, the LT enters the activated state and outputs info 4. The line is now activated; the LT sends info4 to the remote, the remote sends info3 to the LT.

Resynchronization

If the LT fails to recognize info 3, for whatever reason, it will attempt to resynchronize. Entering this state it will output info 2. This is similar to the original synchronization procedure in the pending activation state (the indication given to layer 2 is different). However as before recognition of info 1 leads to the synchronized state.



KEY: ARD ⇒ activation request downstream – either ARN or AR2
AID ⇒ activation indication downstream – either AIN or AI2
unconditional Transitions initiated by
commands: RES, SCP, SSP
external pins: RST, SCP, SSP

Fig. 3.3: PT: State Diagram

3.1.2.2. PT Mode

Refer to figure 3.3 (State Diagram)

Unconditional States

Reset

This state is entered unconditionally after a reset; this may be a software reset (RES) or a hardware reset applied to the RST pin.

Test Mode

The test signal (it_i) outputted to the U-interface in this state is dependent upon the command which originally invoked the state. SSP causes single alternating pulses to be transmitted (it_2); SCP causes continuous alternating pulses to be transmitted (it_1). During this state the test signal is transmitted continuously over the U-interface (burst mode is suspended).

Conditional States

Deactivated

The physical interface is in a low power state. The IOM clocks are disabled (if ENCK = 1) and power consumption is cut to a minimum. The receive line awake detector unit is active.

Power up

This state is identical to the deactivated state outlined above, except that the IOM clocks are running and the power consumption is higher. This state is entered after the TIM command (0000) has been recognized and the S bus layer 1 device can now communicate with the IBC over the IOM interface. This mechanism is described in section 3.2.

Note that monitor channel communication is not possible in this state.

Pending Activation

The reception of an ARN command indicates that a device on the S bus wishes to activate the link to the LT. The PT passes this signal on to the LT in the form of info1w (awake signal).

Level Detect

When the LT responds to info 1w or when it wishes to activate the link of its own accord, it sends info 2. This is initially detected at the PT as simply a line signal. After 1.5ms the PT goes to the level detect state and stops transmitting anything on the line (i.e. if it had been in pending activation). This allows it to synchronize to the incoming signal.

Note that monitor channel communication is not possible in this state.

Synchronized

Once the PT has identified the line signal as info 2 it is synchronized (this detection takes less than 80 ms). If the S-bit (service bit) in info 2 is set then the LT wants loop 2 activated as close as possible to the S interface and hence not in the IBC (see 2.4.1). The IBC simply passes this information on to the S-bus layer 1 device by sending indication AR2 (activation request loop 2) over the C/I channel. If the S-bit in info2 is zero then normal activation is assumed and the indication ARN (activation request no loop) is sent.

Wait for AIU

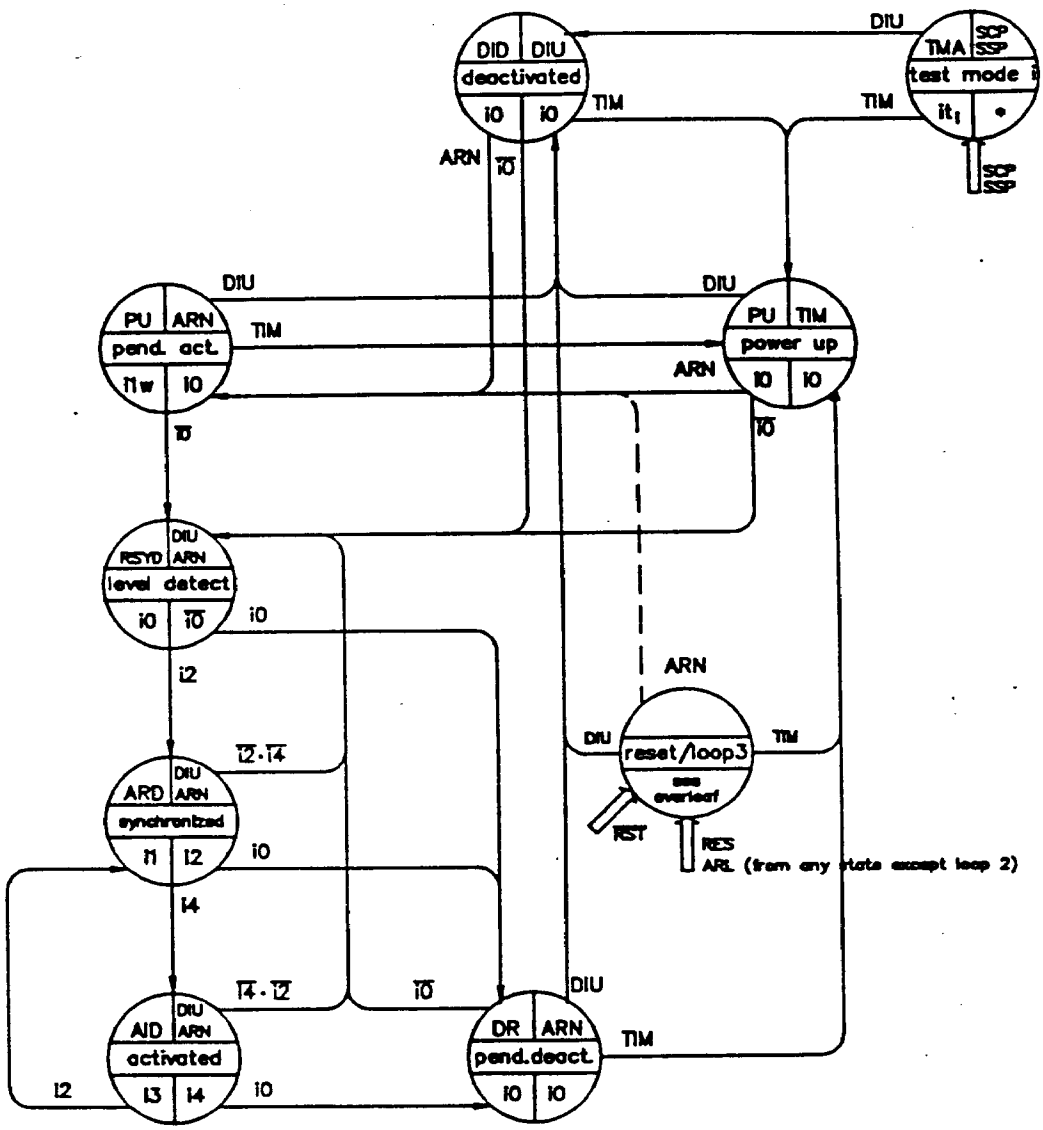
This state is entered upon receipt of info 4 from LT (implying that the LT has synchronized with info 1). Nothing new is outputted. The indication on the C/I channel again depends on the S-bus state. The PT must wait for confirmation of S-bus activation before fully activating the U-interface. It must wait for AIU.

Activated

Confirmation of successful S-bus activation comes, in the form of an AIU command, from the S-bus layer 1 device. Only now will the PT transmit info 3 to the LT, thereby activating the U-interface. An activation indication is sent downstream; either AIN, Activation Indication Noloop (S-bit of info4 = 0) or AI2, Activation Indication Loop2 (S-bit of info4 = 1).

Pending Deactivation

If during an activation procedure the PT, for some reason, "looses" the info it has been receiving from the line, one of two things happen. If it detects that there is a signal still on the line but it doesn't recognize what it is, it returns to the level detect state. If it sees no signal at all, it then assumes info 0 is being transmitted and interprets this as a deactivation request. The pending deactivation state is entered and the S-bus layer 1 device is sent a deactivation request DR. The PT transmitts info 0 on the line. Only a DIU command from the SBC (indicating that the S-bus has been deactivated) will cause the PT to enter the deactivated state.



KEY: ARD ⇒ activation request downstream - either AR1 or AR2
AID ⇒ activation indication downstream - either AI1 or AI2
unconditional Transitions initiated by
commands: RES, ARL (except from loop2), SP, SCP
external pins: RST

Fig. 3.4: TE: State Diagram

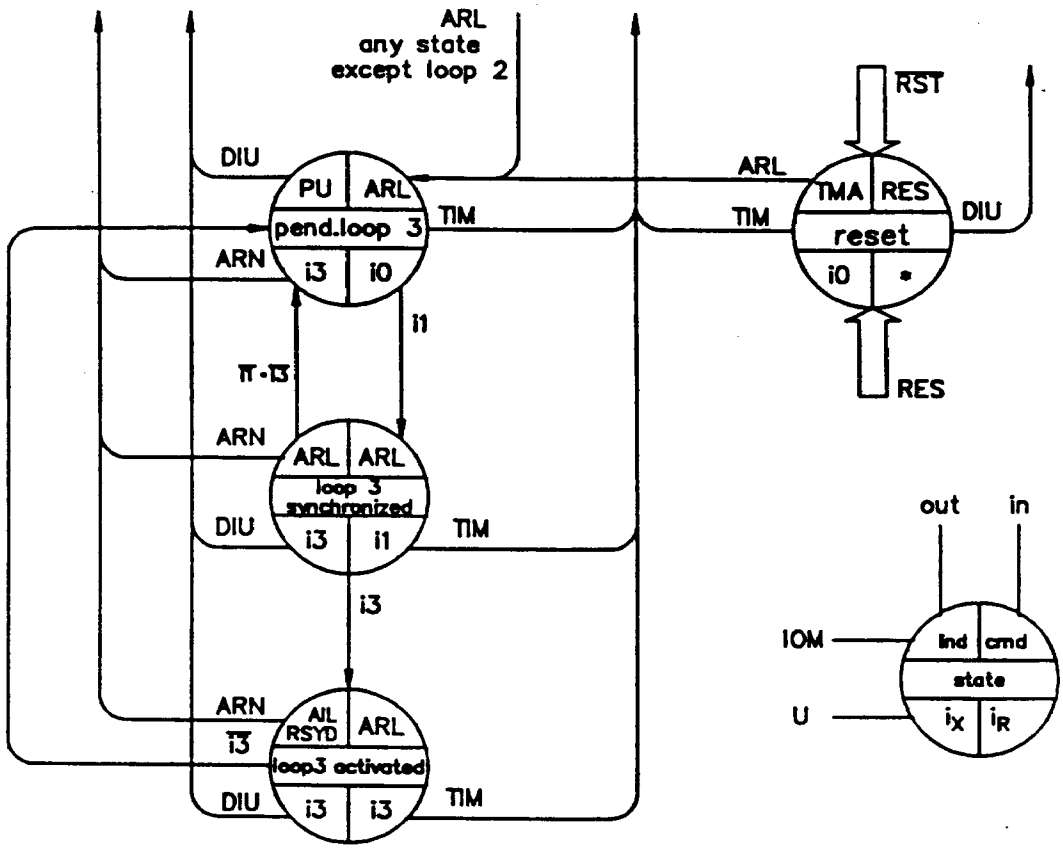


Fig. 3.5: TE: State Diagram; Reset/Loop3

3.1.2.3. **TE Mode**

Refer to Figures 3.4 and 3.5. These two figures are in fact one diagram. Fig. 3.5 shows in detail what is referred as the "reset/loop3 state" in figure 3.4.

Unconditional States

Test mode

This state results from the recognition of C/I commands SCP or SSP. After SCP continuous alternating pulses are outputted on the line (it_1); after SSP single alternating pulses are outputted (it_2) (see 2.4.2) for the signal description). The burst mode is suspended during this mode

and the test signal is sent continuously.

Reset

This state is entered after a RES (software reset) or after pin RST is brought low (hardware reset). Both the transmitter and the awake detector are disabled and activation from the LT is not possible.

Conditional states

Deactivated

This is the power down state of the physical protocol. The receive line awake unit is active. Clocks are disabled if ENCK = 1. The power consumption in this state is cut to a minimum.

Power up

This state is identical to the deactivated state except for the indication and the fact that the clocks are enabled regardless of the status of the ENCK pin. It is envoked by the TIM (0000) command and its significance will be explained further in section 3.2.

Note that monitor channel communication is not possible in this state.

Pending activation

In response to an ARN command from the layer 2 device the TE initiates activation on the line by sending info 1w to the LT.

Level detect

If the TE, in certain states, detects a signal on the line other than info 0, for longer than 1.5 ms, it enters this state. This happens if the LT initiates an activation of a deactivated link, or the TE itself has requested an activation and the LT has responded. In both cases, the TE must synchronize to the incoming signal and in the latter case the TE ceases transmitting info 1w to increase the quality of the incoming signal. After at most 80 ms, synchronization is achieved and info 2 is recognized.

Note that monitor channel communication is not possible in this state.

Synchronized

Detection of info 2 allows the TE to synchronize itself to the line. If the LT had initiated the activation it could request either normal activation (ARN) or activation of loop 2 at the TE (AR2). If the S-bit in the U-interface frame is set, then loop 2 is initiated at the TE; info 1 is transmitted on the U-interface and AR2 is sent to the layer 2 device. If the S-bit is zero, ordinary activation is initialized; info 1 is transmitted on the U-interface and ARN is sent to the layer 2 device.

Activation

Once the LT synchronizes to info 1 it sends info 4. Info 2 contains a code violation in the framing bit (F- bit) and Info 4 does not. After detection of two frames without code violations in the F-bit, the TE concludes that info 4 is now being received and that the LT is synchronized. It then sends info 3. The exchange of info 3 and info 4 over the line constitutes as activated line and the IBC's at either end are in the activated state. The indication downstream is AIN (activation indication normal) during normal activation and AIL (activation indication loop 2) during test loop 2 activation. If the TE looses synchronization to info 4 this state is left and the state corresponding to the signal it now recieves is entered; if the TE recognizes info 2 it goes to the synchronized state (as with normal activation); if it recognizes a signal is present but can't identify it it goes to level detect; if it recognizes no signal present (info 0) it goes to "pending deactivation" and prepares to deactivate.

Pending Deactivation

If info 0 (no signal) is detected on the line once the activation process begins, the TE will enter this state and transmit info 0 itself. However it will only deactivate upon receipt of DIU from layer 2 device.

Pending Loop 3

Loop 3, the local TE loop, is initialized after the layer 2 device issues an ARL command. If the IBC is in any other state except those associated with loop 2 (either loop 2 activated or loop 2 synchronized) ARL will cause the pending loop 3 state to be entered. In this state info 1 is not actually transmitted on the line but simply looped from the TE transmitter back to the TE receiver.

Loop 3 Synchronized

To enter the synchronized state in loop 3, the TE must synchronize to info 1 rather than info 2 as in normal operation. But as outlined in section 3.1.1. info 2 and info 1 are structurally the same and hence the synchronization procedures can be considered equivalent. Info 3 is now transmitted and, as before, looped back to the receiver.

Loop 3 Activated

In this case info 3 is detected and activation is achieved. Loop 3 activation refers to a clear passage of info 3 between transmitter and receiver of the TE and is indicated by AIL to the layer 2 device. If however, a signal is detected on the line from the LT the indication changes to RSYD. The loop isn't broken but the change in indication allows higher software layers to decide whether the loop or the line signal is the more important.

3.1.3. Example of Activation/Deactivation

Figure 3.6 illustrates an activation and deactivation procedure between an IBC in LT-mode and an IBC in TE- mode over the U-interface line. It illustrates how the state machines of the respective modes interwork to facilitate activation and deactivation. In this case activation was

initiated by an ARN request at the terminal and deactivation by a DR command at the LT. Activation could also have been initialised at the LT using an ARN request.

Notes for figure 3.6

- T1 : 1.5ms; time for error free level detection
- T2 : < 80ms; time for synchronization and equalizer adaption
- T3 : 1 ms; four subsequent bursts with no CV in F- bit
- T4 : 2ms; time for error free detection of INFO 0

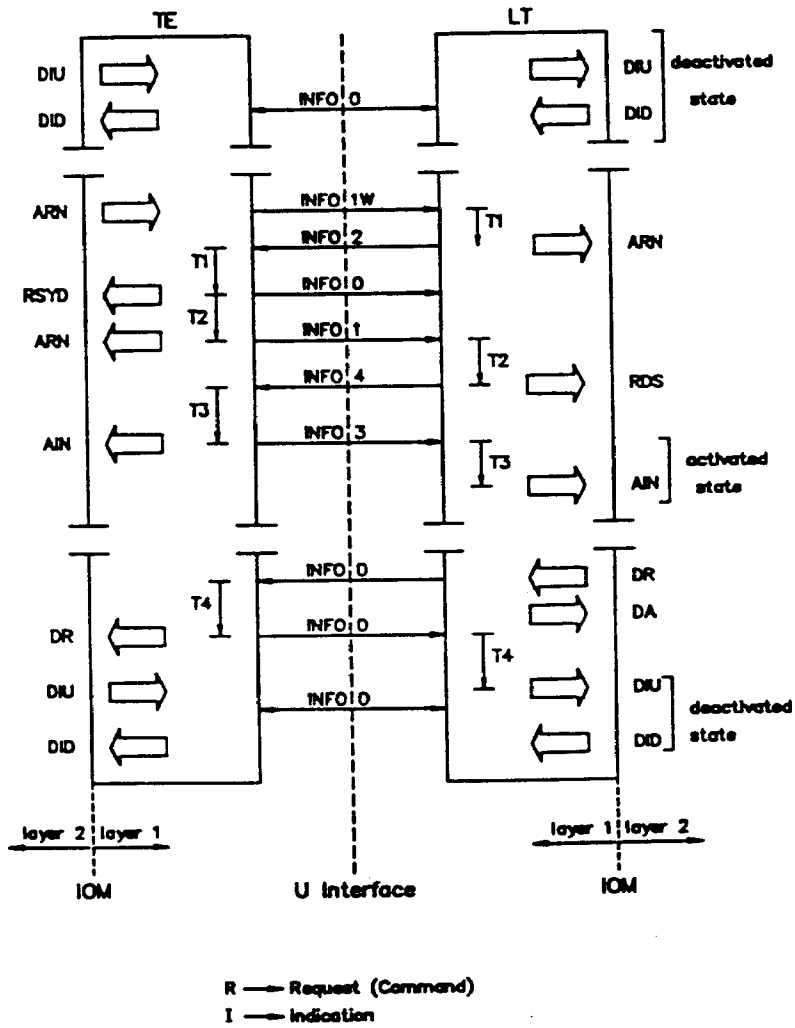


Fig. 3.6: An Example of IBC Activation/Deactivation

40

3.2. Reset

In accordance with the state diagrams the reset state is entered unconditionally after either a software RES command is received or after the $\overline{RST}$ pin is set to 0. After power up a reset should be applied to the IBC to bring it to a well-defined state.

In the LT mode all outputs are high impedance during $\overline{RST}$ = 0. However the IOM clocks must always be enabled.

In the TE/PT modes $\overline{RST}$ acts with $\overline{ENCK}$ to give the following of states.

$\overline{RST}$	$\overline{ENCK}$	
0	1	RESET; Outputs high impedance
0	0	RESET; Outputs low impedance Clocks are running
1	1	NORMAL OPERATION; IOM clocks disabled in deactivated state
1	0	NORMAL OPERATION; IOM clocks not disabled in "deactivated" state

Power consumption is under 13 mW in the deactivated state (also called the "Power-Down" state) when the IOM clocks, and hence the IOM interface itself, are disabled. When disabled the clock lines are low and the data lines are high. When the IOM interface is disabled no C/I commands can be passed to the IBC. To communicate over the C/I channel the clocks must first be enabled.

For the TE/PT case the deactivation procedure is shown in figure 3.7. After detecting the code DIU (Deactivate Indication Upstream) from the downstream unit, the IBC responds by transmitting DID (Deactivate Indication Downstream) during subsequent frames and stops the timing signals synchronously with the end of the last C/I channel bit of the fourth frame.

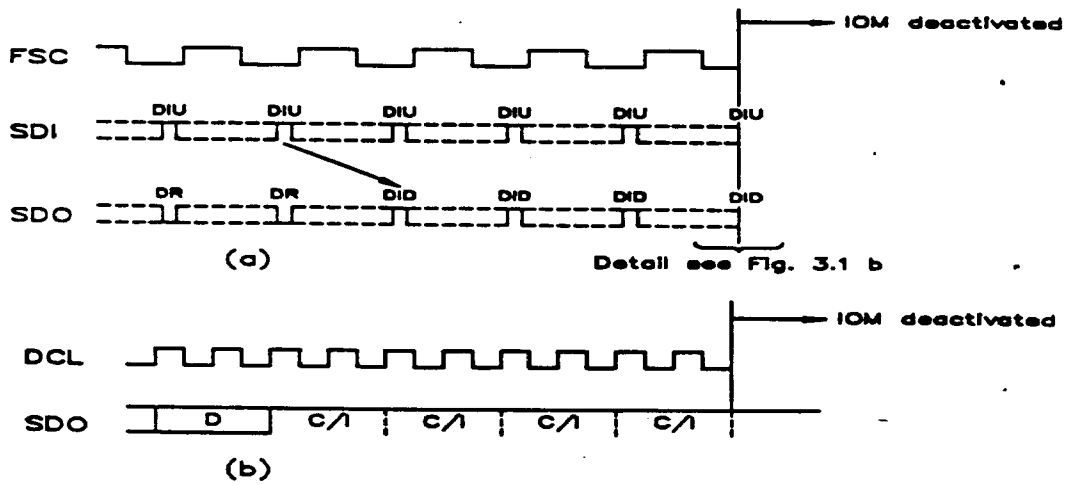


Fig. 3.7: Deactivation of the IOM Interface

The clock pulses will be enabled again when the IBC recognizes a low level on SDI (equivalent to the C/I command TIM = "0000") or when a non-zero level on the U interface is detected.

When the clocks have been enabled the indication PU is sent in the C/I channel. The downstream unit may then insert a valid code in the C/I channel. The continuous supply of timing signals by the IBC is assured as long as there is no DIU command in the C/I channel. If timing signals are no longer required and activation is not yet requested, the downstream unit may indicate this by sending DIU.

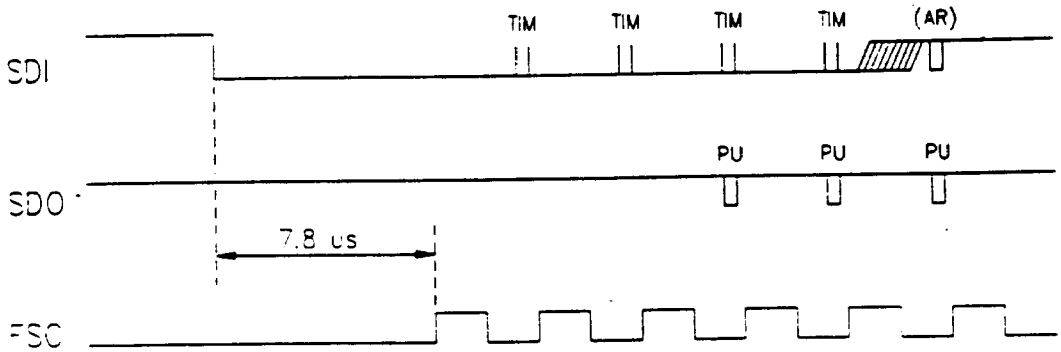


Fig. 3.8: Activation of the IOM Interface

As an alternative to clock activation via SDI, the asynchronous wake-up pin $\overline{\text{ENCK}}$ (X3 in both TE and PT mode) can be grounded. In this case the timing given in figure 3.8 applies. When $\overline{\text{ENCK}}$ is tied to ground the IOM clock pulses are delivered by IBC at all times.

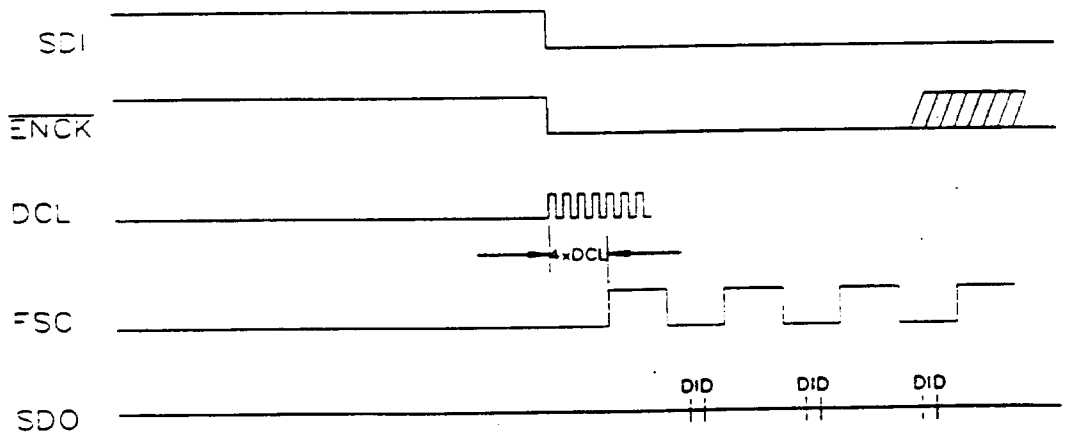


Fig. 3.9: Activation of the IOM Interface via $\overline{\text{ENCK}}$ (pin X3) in TE/PT mode (NB: DCL out of scale).

4. Control Codes

4.1. Command/Indication Control Codes (C/I Codes)

As mentioned in paragraph 2.3.2. the C/I codes transfer information between layer 1 (IBC) and layer 2 (ICC) directly related to the OSI reference model i.e. activation/deactivation, test loop initialisation, reset etc. The exchange of C/I codes is governed by the state machine. A complete list of all codes in each mode is given in table 4.1 and 4.2.

C/I codes are transmitted in the B* channel of the IOM frame and must follow the following procedure: When a new command or indication is to be sent it must be repeated in two successive IOM frames before it is recognized at the receiver (Double-last-look criterian).

Command (downstream)	Abbr.	Code	Remark
Deactivate Request	DR	0000	(x)
Activate Request No loop	ARN	1000	
Activate Request Local loop	ARL	1001	Loop 1 activation requested
Activate Request loop 2	AR2	1010	
Deactivate Indication	DID	1111	
Reset	RES	1101	Software Reset (x)
Disable Supply	DIS	0011	used to control the drain on local power supply (x)
Send Single Pulses	SSP	0101	Ones (AMI pulses) transmitted at 4kHz (TEST MODE 1) (x)
Send Continuous Pulses	SCP	0111	Ones (AMI pulses) transmitted contionously (TEST MODE 2) (x)
Indication (upstream)	**Abbr.**	**Code**	**Remark**
Deactivate Indication	DIU	1111	
Deactivate Acknowledge	DA	0001	
RDS Indication	RDS	0111	Running Digital Sum. Code violation register enabled. Receiver synchronized
Activate Request	ARU	1000	
Activate Indication	AIU	1100	
Resynchronisation	RSYU	0100	Lost Framing: receiver not synchronized to the input signal
High Impedance	HI	0011	After PFOFF the phantom power supply becomes high impedance

(x) unconditional commands

Tab. 4.1: Commands and Indication in the LT Mode

Command (upstream)	Abbr.	Code	Remark
Timing	TIM	0000	Layer 2 device requires clocks to be activated
Activate Request No loop	ARN	1000	
Activate Request Local loop	ARL	1001	* Test loop 3 activation request
Activate Indication	AIN	1100	**
Deactivate Indication	DIU	1111	
Reset	RES	1101	Software Reset (x)
Send Single Pulses	SSP	0101	Ones (AMI pulses) transmitted at 4kHz (TEST MODE 1) (x)
Send Continuous Pulses	SCP	0111	Ones (AMI pulses) transmitted continuously (TEST MODE 2)(X)
Indication (downstream)	**Abbr.**	**Code**	**Remark**
Deactivate Request	DR	0000	
Power Up	PU	0111	
Resynchronsation	RSYU	0100	Lost Framing: receiver not synchronized with input
Activate Request No loop	ARN	1000	
Act. Request Local loop	ARL	1001	*
Activate Request loop 2	AR2	1010	
Act. Indication No loop	AIN	1100	
Act. Indication Local loop	AIL	1101	*Test loop 3 activated
Act. Indication loop 2	AI2	1110	
Testmode Acknowledge	TMA	0101	*
Deactivate Indication	DID	1111	

(x) unconditional commands

* only in TE

** only in PT

Tab. 4.2: Commands and Indications in the PT/TE Mode

4.2. Monitor Commands

Besides the C/I section of the B* channel, inter-device communication on the IOM-interface is also possible via the monitor channel. However the monitor channel protocol is more straightforward; the layer 2 device commands, the layer 1 device responds. Furthermore the monitor codes deal mainly with auxillary tasks not directly related to the maintenance of the link. Finally they are totally under the control of the user and contain 17 NOP codes (00_H and FX_H). Table 4.3 lists all IBC monitor codes.

Upon receipt of a message the IBC will send a response in the monitor channel. Availability of the response is indicated by setting the MX bit of the IOM frame to zero. (IOM-1 or inverted modes) or by looping back the received MX bit into the MX bit transmitted (IOM-2 mode).

The monitor channel is used to read the IBC internal registers (I(7:0) and R(7:0)) and to set or simply read the adaptive amplifier and equalizer settings. Note, however, that once both amplifier and equalizer coefficients have been set, the adaptive logic is turned off and the given settings remain constant regardless of any changes to the input signal.

However the coefficients are zeroed and hence must be reprogrammed after either:

- the device has been through the deactivated (Power-Down) state.

- a local loop has been implemented (i.e. loop 1 in LT mode and loop 3 in TE mode).

The adaptive logic is turned on again only after a hardware or software reset (coefficients again zeroed).

Merely reading the values however does not affect the adaptive nature of the settings.

To protect the chip from reading erroneous data from the monitor channel during the synchronization period, the monitor channel is ignored by the device during the following states:

- Power Up. TE and PT modes.

- Level Detect. TE and PT modes.

- Deactivated LT modes.

Message	Response	Exploration
00000000	-	NOP
1111XXXX	-	NOP
10000000	00111110	Identification
11101110	I(7:0)	Supply Current Equivalent
11101111	R(7:0)	Code Violation Register
00000010	1XX,A(6:2)	Gain Factor (part I)
00000011	1XX,C(2:0),A(1:0)	Equalizer coefficient and gain factor (part II)
001,A(6:2)	101,A(6:2)	External Programming of gain factor (part I)
010,C(2:0),A(1:0)	110,C(2:0),A(1:0)	Programming of gain factor (past II) and equalizer coefficient
011,CONF(4:0)	111,CONF(4:0)	Programming of Conf(4:0)

To implement any of the following integrated functions set the corresponding bit to 0 (Reset Values all high).

CONF4 : TE mode: clock output at pin X4 : 2.56 MHz (CONF4 = 1) or 7.68 MHz (CONF4 = 0)
LT IOM-1 mode: programmable output X0

CONF3 : Equalizer output signal at pin DISS

CONF2 : Descrambler disable

CONF1 : DC balancing bit enable

CONF0 : Amplifier gain modification during data transmission

Note
1. Messages are sent by the layer 2 device to the IBC (in the ICC by writing to the MONR register).
2. Responses are sent by the IBC to the layer 2 device (in the ICC the MODE: HMD1 must be set to enable the ICC to read the incoming monitor byte).

Tab. 4.3: IBC Monitor Commands

4.3. IBC Registers

The IBC contains 2 registers which are user accessible over the monitor channel.

4.3.1. I(7:0) Supply Current Equivalent

This register is only useful in the LT mode when the power supply control functions are active. In this mode X3 functions as the MPF pin (Main Power Feed). Through this pin the 8 bit supply current equivalent from the local power supply can be read into the I(7:0) register. After reset I(7:0) = 00_H.

4.3.2. R(7:0) Code Violation Register

This register counts the number of erroreous code violations in the data channels encountered by the RDS function of the IBC and this information may be used by the software to estimate the bit error rate.

5. Electrical Specification

5.1. Pin Definition and Functions

Pin DIP	PinPLCC	Symbol	Input(I) Output(O)	Function	
17	20	LO1	0	line transmitter; output 1	U-interface
16	19	LO2	0	line transmitter; output 2	
21	26	LI	I	line receiver	
11	13	SDO	0	Serial Data Out	IOM Interface
14	16	SDI	I	Serial Data In	
13	15	DCL	I/O	Serial Data Clock	
12	14	FSC	I/O	Frame Sync.	
24	1	MO	I	Operating Mode setup pins	
8	10	M1	I		
2	3	X0	I/O	Multifunctional pins; mode specific functions (see table 5.4)	
5	7	X1	I/O		
10	12	X2	I		
4	6	X3	I		
3	4	X4	I/O		
6	8	XTAL1	I	External crystal or external oscillator input	
7	9	XTAL2	O	External crysrtal connection (N.C. when external oscillator is used)	
23	28	$\overline{TST}$	I	Device test pin; not for general use; tie high always	
22	27	DISS	O	Disable supply;	
9	11	$\overline{RST}$	I	Hardware reset pin; active low	
18	21,22	VDD	I	Digital Power Supply 5 V ± 5%	
15	17,18	VSS	I	Digital Ground	
1	2	AVDD	I	Analog Power Supply 5 V ± 5%	
20	24	AVSS	I	Analog Ground	
19	23	VDD2	O	2.5 V output; connected to VDD via 10nF capacitor connected to AVSS via 10nF capacitor	
	5,25	N.C		Not Connected internally	

Tab. 5.1: IBC Pin Functions

5.2. DC Characteristics

TA = 0 to 70°C; VDD = 5V ± 5%, VSS = 0V, AVSS = 0V.

	Symbol	Parameter	Limit values min	max	Unit	Test condition
All pins except LO1,2, LI1, XTAL1, XTAL2	VIL	Input low voltage	VSS-.4	0.8	V	
All pins except LO1,2, LI1, XTAL1, XTAL2	VIH	Input high voltage	2.0	VDD+0.4	V	
All pins except LO1,2, LI1, XTAL1, XTAL2	VOL1 VOL2	Output low voltage 1) Output low voltage 2)		0.45 0.45	V V	IOL=2mA IOL=7mA
All pins except LO1,2, LI1, XTAL1, XTAL2	VOH VOH	Output high voltage Output high voltage	2.4 VDD-.5		V V	IOH=-400µA IOH=-200µA
All pins except LO1,2, LI1, XTAL1, XTAL2	ICC	Power supply current operational		20	mA	VDD=5V, Inputs at 0V or VDD, no output loads
All pins except LO1,2, LI1, XTAL1, XTAL2	ICC	Power supply current power down		2.5	mA	VDD=5V, Inputs at 0V or VDD, no output loads
All pins except LO1,2, LI1, XTAL1, XTAL2	ILI ILO	Input leakage current Output leakage current		+10 µA	+10 µA	0V<VIN<VDD to 0V 0V<VOUT<VDD to 0V
L01,2	VX	Absoute value of 3) output pulse 4) amplitude (VL01-VL02) 5)	4.75 -5.25 0	5.25 -4.75 0	V V V	
L01,2	PW	Pulse width	1.22	1.38	µs	
L01,2	RX	Transmitter output impedance	9	21	Ohm	

	Symbol	Parameter	Limit values min	max	Unit	Test condition
XTAL1	VIL VIH	Input low voltage Input high voltage	VDD-.5	0.5	V V	
XTAL2	VOL VOH	Output low voltage Output high voltage	VDD-.5	0.5	V V	Io ≤ 100µA CL ≤ 100pF

Notes:
1) All outputs except SDO
2) Output SDO only
3) Positive Pulse
4) Negative Pulse
5) No pulse

Tab. 5.2: DC Characteristics of the IBC

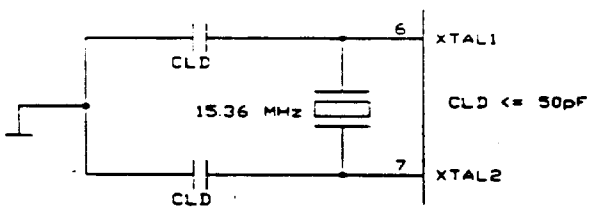
5.3. Capacitances

TA = 0 to 70°C, VDD = 5V ± 5%, VSS = 0V, AVSS = 0V, f_c = 1MHz

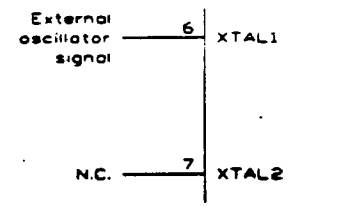
	Symbol	Parameter	Limit values min	max	Unit	Test condition
	CIN CIO	Input capacitane Output capacitance		7 7	pF pF	
L01,2	COUT	Output capacitance against AVSS		10	pF	
XTAL1,2	CLD	Load capacitance		50	pF	

Tab. 5.3: Input/Output Capacitanes of IBC. Unmeasured pins returned to ground.

5.4. Recommended Oscillator Circuits



Crystal oscillator mode



Driving from external source
minimum high time: 30 ns
minimum low time: 28 ns

Fig. 5.1:

5.5. Absolute Maximum Ratings

Ambient temperature under bias	0°	to	70°C
Storage temperature	-65°	to	125°C
Voltage on any pin with respect to ground	-0.4	to	VDD+0.4

Note: Stresses above those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.5.1. Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse (figure 5.2).

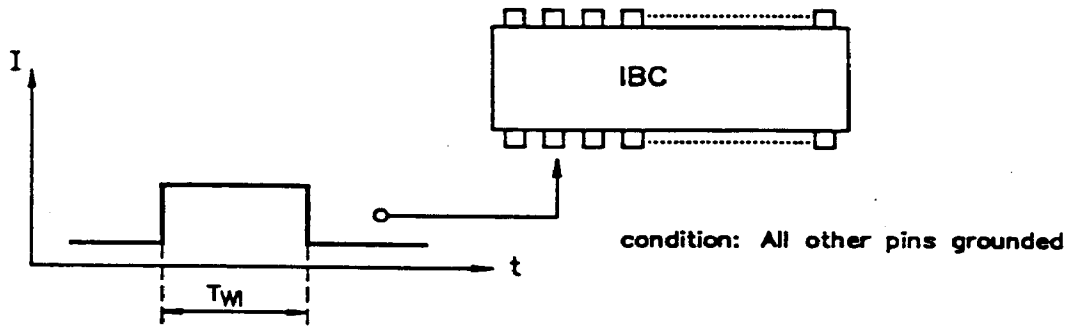


Fig. 5.2: Test Condition for Maximum Input Current

5.5.2. Transmitter Input Current

The destruction limits are given in figure 5.3
Ri ≥ 1 ohm.

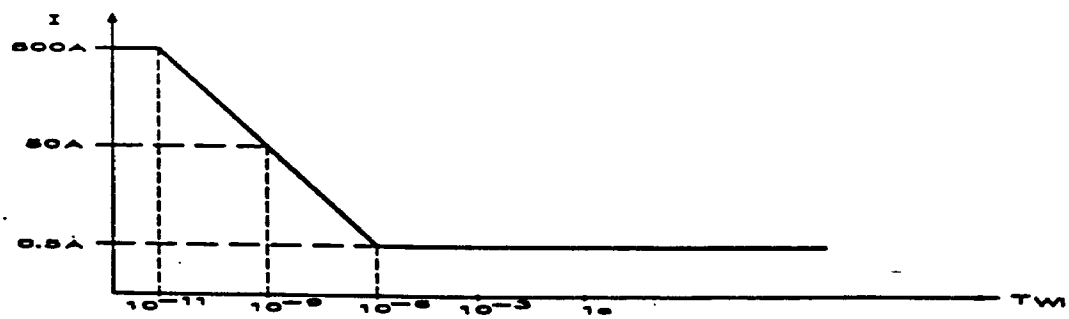


Fig. 5.3:

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5.5.3. Receiver Input Current

The destruction limits are given in figure 5.4.
Ri ≥ 250 ohms.

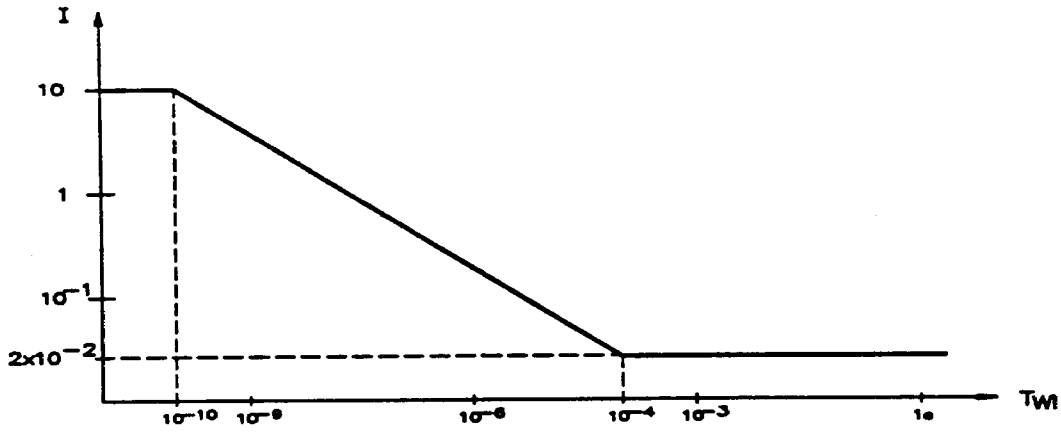

Fig. 5.4:

5.6. AC Characteristics

TA = 0 to 70°C, VDD = 5V ± 5%

Inputs are driven at 2.4 V for a logic "1" and at 0.4 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".

The AC testing input/output waveforms are shown below.

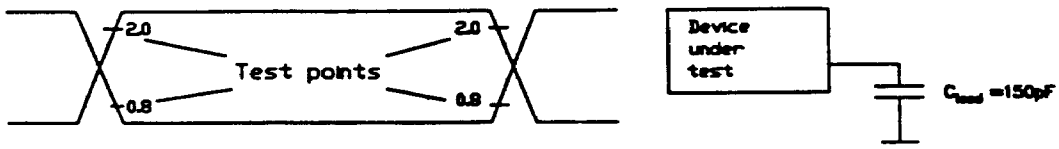

Fig. 5.5: Input/Output Waveform for AC Tests.

5.6.1. Clock Timing

Table 5.4 summarizes the clocks produced in the different operating modes and their respective duty cycles. The table also indicates which clocks are derived directly from the crystal and which are synchronized to the line using the on-board DPLL circuitry.

	application						
	TE	TE	TE	PT	LT	LT	LT
operation of IOM interface	inverted mode	IOM-1 mode	IOM-2 mode	normal mode	IOM-1 mode	inverted mode	IOM-2 mode
M1 M0	0 0	0 0	0 RST	0 1	1 0	1 1	1 1
DCL	o:512kHz* 1:1	o:512kHz*1 :1	o:1.536 MHz* 1:1	o:512kHz* 1:1	i:512kHz	i:4096kHz	i:4096kHz
FSC	o:8kHz* 63:1	o:8kHz* 1:1	o:8kHz* 1:2	o:8kHz* 1:1	i:8kHz	i:8kHz 511:1	i:8kHz
X4	o:2.56MHz 1:2 o:768MHz* 1:1	o:2.56MHz 1:2 o:768MHz* 1:1	o:2.5MHz 1:2	o:7.68MHz* 1:1	i:PFOFF	i:PFOFF	i:PFOFF
X3	i:$\overline{\text{ENCK}}$	i:$\overline{\text{ENCK}}$	i:$\overline{\text{ENCK}}$	i:$\overline{\text{ENCK}}$	i:MPF	i:MPF	i:MPF
X2	i:1	i:0	i:0	i:$\overline{\text{SCP}}$	i:0	i:TS2	i:TS2
X1	o:1.536MHz* 1:1	o:1.536MHz *1:1	o:768kHz* 1:1	i:$\overline{\text{SSP}}$	o:15.36MHz 1:1	i:TS1	i:TS1
X0	o:3.84MHz	o:3.84MHz	o:3.84MHz	i:1	o:CONF4	i:TSO	i:TSO

* : synchronized to U i: = input o: = output

Notes: 1. SDI-(IOM-interface) - the pin is connected to an internal pull-up resistor in TE normal and LT normal modes.

2. SDO -(IOM-interface) - open drain output in LT mux mode inverted.
open drain output with internal pull- up resistor in NT-mode
push-pull otherwise

3. The following clock outputs are derived from the 15.36 MHz crystal/external oscillator:(i.e. un-synchronized)

15.36 MHz
3.84 MHz
2.56 MHz

4. The following clock outputs are synchronized to the line

7.68 MHz
1.536 MHz
768 kHz
512 kHz
8 kHz

Tab. 5.4: IBC Operating Modes and Mode Specific Pin Configurations

Mode	Name	Description	Pin	I/O	Function
LT	PFOFF	Powerfeed off	X4	I	Puts the IBC into a powerfeed off state. This state is indicated by C/I code HI.
LT	MPF	Main Power Feed	X3	I	The 8 bit supply current equivalent is read serially through this pin into I(7:0) from the local power supply. The read is synchronous to the B1 channel in the IOM frame (time slot 0 in LT:mux mode). Used for power supply control by the layer 2 device. Tie low when not in use.
TE/PT	$\overline{\text{ENCK}}$	Enable clocks	X3	I	Enables clocks in 'deactivated' state. Also during RST = 0, outputs are low impedance when $\overline{\text{ENCK}}$ = 0 and high impedance otherwise.
PT	$\overline{\text{SSP}}$ $\overline{\text{SCP}}$	Send Single Pulses Send Contin Pulses	X1 X2	I I	Test Mode 1 Test Mode 2
LT IOM-1	CONF4	Programmable Output Pin	X0	O	Programmed over Monitor Channel. Useful to control other devices.
LT	TS0-2	Time Slot 0 - 2	X0, 1, 2	I	One of eight possible time slots is selected to be read by the device (TS0 = LSB).

Tab. 5.5: Mode Specific Pin Functions

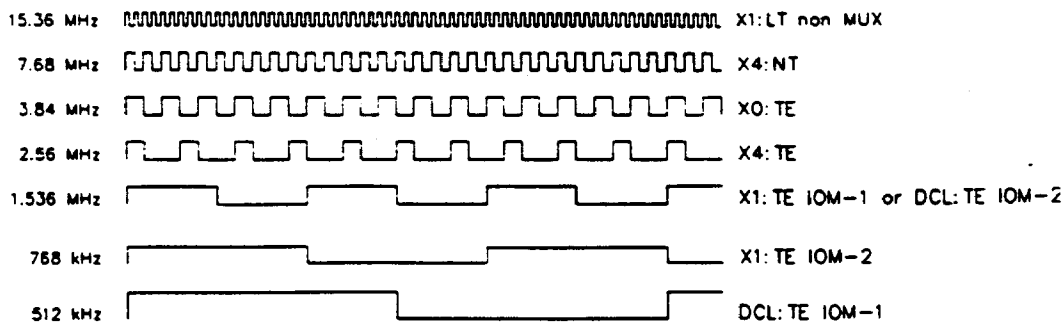

Fig. 5.6: Output Clock Relationships

Figure 5.3 shows the relationship between the various clock outputs from the IBC. The crystal frequency is 15.36 MHz. All clock outputs have a duty cycle of 1:1 except 2.56 MHz (1:2). Note that the following are derived directly from the crystal oscillator; 15.36 MHz, 3.84 MHz and 2.56 MHz. They are not synchronized to the line. Their accuracy will be, to a first order, governed by the crystal accuracy (100 ppm maximum).

The following clocks are derived both from the crystal and, with the help of the DPLL, from the line; 7.68 MHz, 1.536 MHz, DCL and FSC. Synchronization may be regarded as a two stage process. Firstly, a synchronous 7.68 MHz signal is derived using the DPLL. Secondly, all other synchronous clocks are derived, by simple division, from 7.68 MHz synchronous. Because of the internal method of synchronization employed, the 7.68 MHz signal may "step forward or back" by 1 crystal period (see figure 5.4). Hence the period of 7.68 MHz, and all synchronous clocks derived from it, may vary by one crystal period (±65 ns). This, to a first order, gives the accuracy of the various synchronous clocks. Table 5.6 to table 5.10 detail the accuracy of the clock outputs with respect to the symbols defined in figure 5.5.

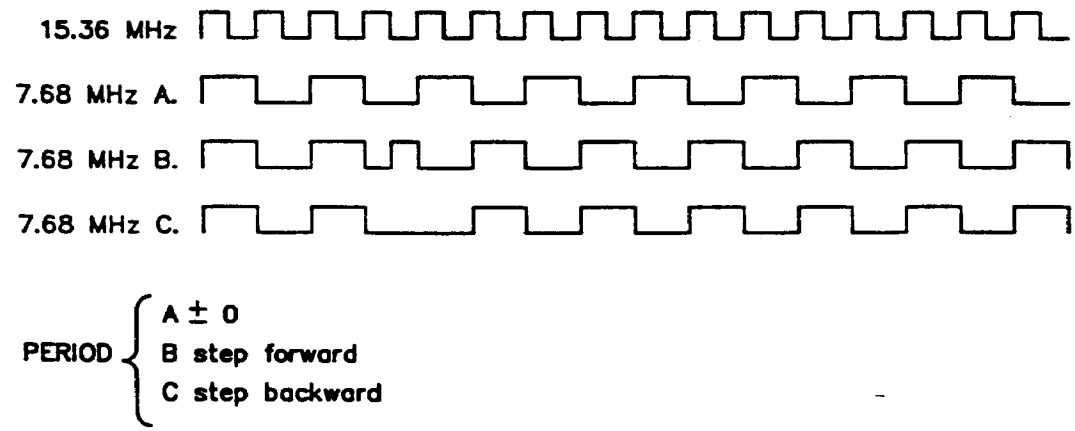

Fig. 5.7: Possible 7.68 MHz Clocks

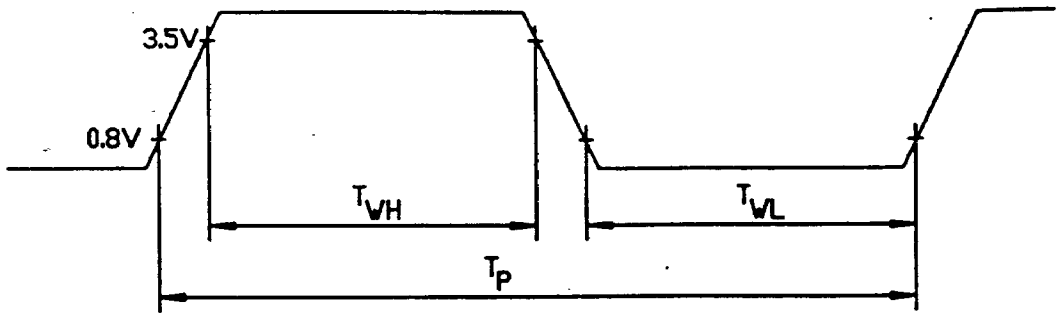

Fig. 5.8: Clock Timing Symbols

	Symbol	Description	min.	typ	max	unit
O	TP	TE/PT 512kHz	1888	1953	2019	ns
U	TWH	TE/PT 512 kHz	944	977	1009	ns
T	TWL	TE/PT 512 kHz	944	977	1009	ns
P	TP	TE: 1.536 MHz	585	651	717	ns
U	TWH	TE: 1.536 MHz	260	326	391	ns
T	TWL	TE: 1.536 MHz	260	326	391	ns
I N P U T	TWH	LT mode	90			ns
	TWL	LT mode	90			ns

Tab. 5.6: DCL Timing

	Symbol	Description	min.	typ	max	unit
O	TP	TE/PT 8kHz 1:1	124.93	125	125.07	µs
U	TWH	TE/PT 8kHz 1:1	62.46	62.5	62.54	µs
T	TWL	TE/PT 8kHz 1:1	62.46	62.5	62.54	µs
P	TP	TE 8kHz 1:2	124.53	125	125.07	µs
U	TWH	TE 8kHz 1:2	41.6	41.67	42.74	µs
T	TWL	TE 8kHz 1:2	83.2	83.3	83.4	µs
OUTPUT	TP	TE(SEL)8kHz63:1	124.93	125	125.07	µs
	TWH	TE(SEL)8kHz63:1	122,08	123.05	124.02	µs
	TWL	TE(SEL)8kHz63:1	1888	1953	2019	ns

Tab. 5.7: FSC Timing

Symbol	Description	min.	typ	max	unit	Conditions
TP	TE 2.56MHz 1:2	-100ppm	390	+100ppm	ns	osc ± 100 ppm
TWH	TE 2.56MHz 1:2	-100ppm	130	+100ppm	ns	osc ± 100 ppm
TWL	TE 2.56MHz 1:2	-100ppm	260	+100ppm	ns	osc ± 100 ppm
TP	PT 7.68MHz 1:1	65	130	196	ns	
TWH	PT 7.68MHz 1:1	65	65	131	ns	
TWL	PT 7.68MHz 1:1	65	65	131	ns	

Tab. 5.8: X4 Clock Timing

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Symbol	Description	min.	typ	max	unit	Conditions
TP	TE: 1.536 MHz	585	651	717	ns	
TWH	TE: 1.536 MHz	260	326	391	ns	
TWL	TE: 1.536 MHz	260	326	391	ns	
TP	TE: 768 kHz	1235	1302	1370	ns	
TWH	TE: 768 kHz	585	651	717	ns	
TWL	TE: 768 kHz	585	651	717	ns	
TP	LT: 15.36 MHz	-100ppm	65.1	+100ppm	ns	osc ± 100 ppm
TWH	LT: 15.36 MHz	-100ppm	65.1	+100ppm	ns	osc ± 100 ppm
TWL	LT: 15.36 MHz	-100ppm	65.1	+100ppm	ns	osc ± 100 ppm

Tab. 5.9: X1 Clock Timing

Symbol	Description	min.	typ	max.	unit	Conditions
TP	TE: 3.84 MHz	-100ppm	260	+100ppm	ns	osc ± 100 ppm
TWH	TE: 3.84 MHz	-100ppm	130	+100ppm	ns	osc ± 100 ppm
TWL	TE: 3.84 MHz	-100ppm	130	+100ppm	ns	osc ± 100 ppm

Tab. 5.10: X0 Clock Timing

Finally table 5.11 defines the rise and fall times of DCL and FSC clocks in the various modes.

Description	Mode	min	typ	max	unit
TRD;DCL rise time	PT/TE			50	ns
	LT IOM-1			60	ns
	else			25	ns
TFD; DCL fall time	PT/TE			50	ns
	LT IOM-1			60	ns
	else			25	ns
TFR; FSC rise time;	PT/TE			50	ns
	LT IOM-1			60	ns
	else			50	ns
TFF; FSC fall time	PT/TE			50	ns
	LT IOM-1			60	ns
	else			50	ns

Tab. 5.11: DCL/FSC Rise and Fall Timing

5.6.2. IOM-Interface

Given the clock accurancies defined in the previous section the following paragraphs define the timing relationships between the data and the DCL and FSC clocks.

5.6.2.1. Master mode

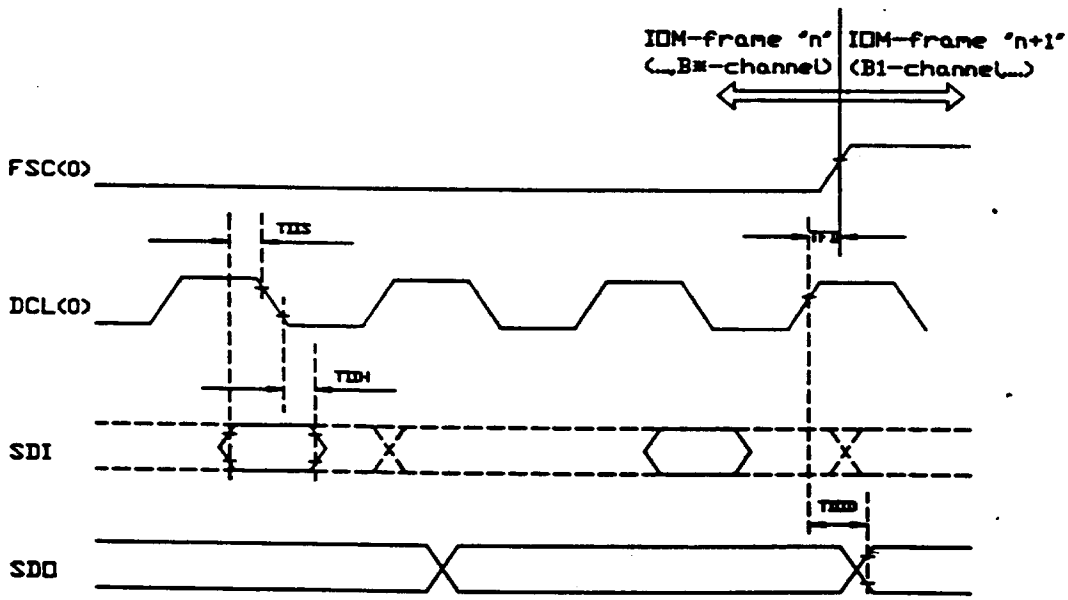

Fig. 5.9: TE/PT IOM-1 and IOM-2 Mode Timing Diagram

Symbol	Parameter	min	max	unit	conditions
TFD	frame sync. delay	-20	20	ns	CL = 100 pF
TIOD	IOM output data delay		200	ns	CL = 100 pF
TIIS	IOM input data setup	20		ns	
TIIH	IOM input data hold	20		ns	

Tab. 5.12: TE/PT Mode Timing (IOM-1 and IOM-2 Mode)

TE Inverted Mode

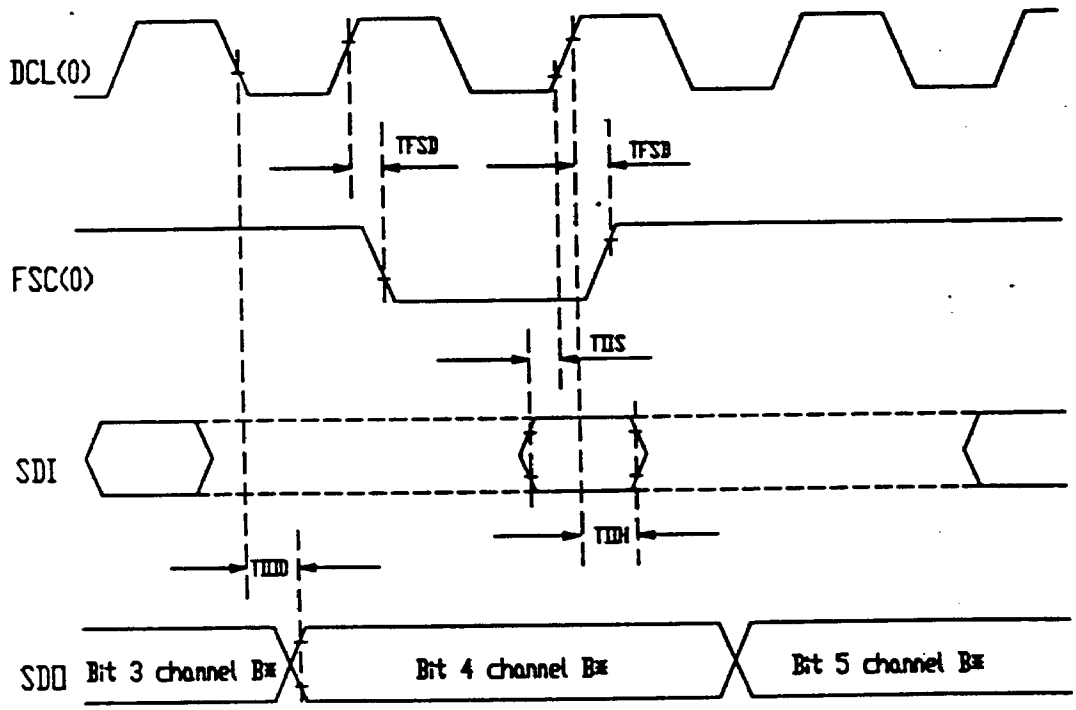

Fig. 5.10: TE Inverted Mode Timing Diagram

Symbol	Parameter	min	max	unit	conditions
TFSD	frame sync delay	- 20	20	ns	CL = 100 pF
TIOD	IOM output data delay		200	ns	CL = 100 pF
TIIS	IOM input data setup	20		ns	
TIIH	IOM input data hold	50		ns	

Tab. 5.13: TE Inverted Mode Timing

5.6.2.2. Slave Mode

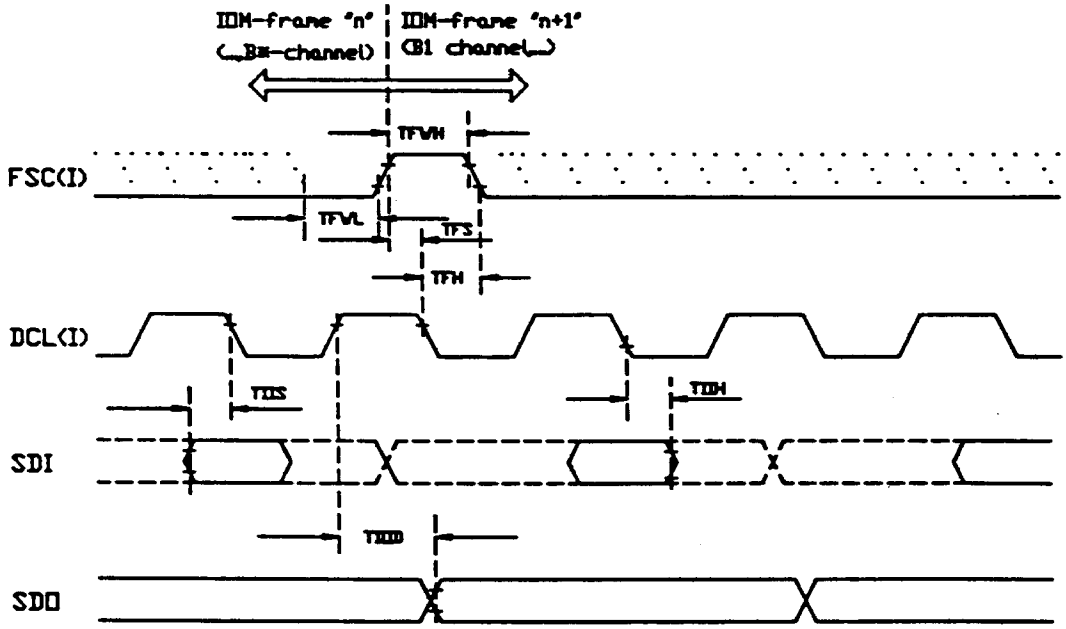

Fig. 5.11: LT IOM-1 and IOM-2 Mode Timing Diagram

Symbol	Parameter	min	max	unit
TFH	frame sync hold	50		ns
TFS	frame sync setup	30		ns
TFWH	frame sync high	80		ns
TFWL	frame sync low	2150		ns
TIOD	IOM output data delay		200	ns
TIIS	IOM input data setup	20		ns
TIIH	IOM data hold	50		ns

Tab. 5.14: LT IOM-1 and IOM-2 Mode Timing

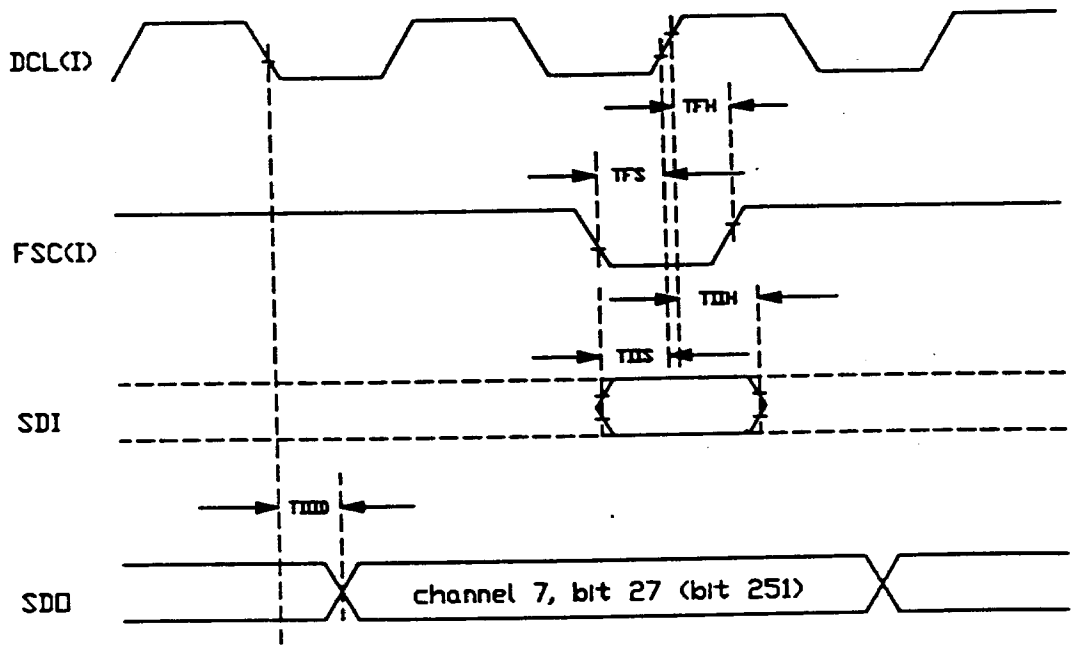

Fig. 5.12: LT Inverted Mode Timing Diagram

Symbol	Parameter	min	max	unit	Conditions
TFH	Frame sync hold	50		ns	
TFS	Frame sync setup	20		ns	
TFH	Frame sync high	124.8		µs	
TFL	Frame sync low	70	200	ns	
TIOD	IOM output data delay		200	ns	
TIIS	IOM input data setup	20		ns	
TIIH	IOM input data hold	50		ns	

Tab. 5.15: LT Inverted Mode Timing

5.7. Receiver Stage Properties

Input stage / measured property		dB
Line Amplifier	- Dynamic Range - Resolution (128 setting)	0 - 30 0.236
Anti Aliasing Filter and Low Pass Filters >1.1 MHz >1.1 MHz	 - minimum attenuation - typical attenuation	 30 35
Equalizer	- Dynamic Range - Resolution (8 settings)	0-15.36dB 2.194

Tab. 5.16: Receiver Stage Properties

5.8. Package Outline

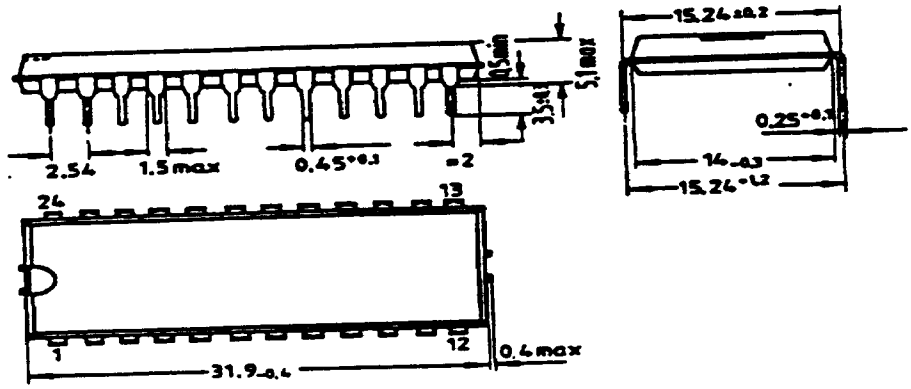

Fig. 5.13: Pin DIP 24

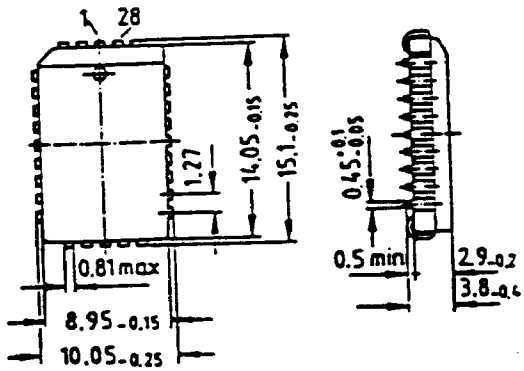

Fig. 5.14: PLCC 28

5.9. Ordering Information

TYPE	ORDERING CODE	PACKAGE
PEB 2095-P PEB 2095-N	Q67100 - H8397 Q67100 - H8396	DIP 24 PLCC 28

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	FAX	(1) 49-75-10-13
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ELECTRA TECHNICAL SALES (206) 821-7442
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