SAPTHAGIRI NPS UNIVERSITY
UNMATCHED EXCELLENCE, UNLIMITED POTENTIAL

School of Engineering and Technology

First Year Department (CSE/CSE-AIML/CSE-AIDS/CSE-DS/ECE/EEE)

BTech - Semester-I

Question bank

Course Title: Computer Organization and Architecture

Course Code: 24BTPHY105

Module -5: Reduced Instruction Set Computer: CISC Characteristics, RISC characteristics. Pipeline and vector processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processors. Multiprocessors: Characteristics of multiprocessors, Interconnection structures, InterProcessor Arbitration, Inter processor Communication and Synchronization, Cache Coherence.

SL NO	QUESTIONS	MARKS	CO	BL
1	Differentiate between the RISC and CISC.	05	CO4	L4
2	Explain the parallel processing with multiple functions units with diagram.	05	CO4	L2
3	Classify organization of computers using Flynn's criteria? Explain.	05	CO4	L2
4	Write about pipelining and its importance in high-speed applications.	02	CO4	L3
5	Demonstrate the pipeline organization for following example $A_i * B_i + C_i$ for i=1,2,3…..	05	CO4	L3
6	With example, explain four segment CPU pipeline and timing of instruction pipeline.	06	CO4	L2
7	Implement a simple pipeline unit for floating point addition and subtraction with example.	07	CO4	L3
8	Explain the instruction pipeline with example.	10	CO4	L2
9	Explain the different major Hazards in pipelined execution.	06	CO4	L2
10	Define vector processing? List the application of vector processing.	02	CO4	L1
11	Explain the 3*3 matrix multiplication using vector processors.	05	CO4	L2
12	Explain the memory interleaving?	04	CO4	L2
13	Define array processors? Explain SIMD array processor.	06	CO4	L2
14	Define a multiprocessor system. What are its main advantages?	05	CO4	L2
15	Differentiate tightly coupled and loosely coupled multiprocessors.	04	CO4	L4
16	Write short note on time shared common bus and multiport memory.	10	CO4	L3
17	Explain in detail about crossbar switching, multistage switching network and hypercube system.	10	CO4	L2
18	Explain the Daisy-chain arbitration with a neat diagram.	07	CO4	L2
19	Explain the parallel arbitration logic with a neat diagram.	07	CO4	L2
20	Explain the inter-processor communication and synchronization in a shared multiprocessor environment.	10	CO4	L2
21	Explain the 8*8 omega switching network with a neat diagram.	06	CO4	L2
22	Explain the mutual exclusion with a semaphore mechanism	05	CO4	L2
23	Explain the cache coherence problem with the solution.	08	CO4	L2
24	Explain write through and write back methods of cache updation.	07	CO4	L2

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