# Quality Control Procedures for High-Speed Backplane System (25 Gbps)

This document outlines the quality control (QC) procedures for validating data transfer links for the backplane system. These procedures ensure signal integrity and reliable data transmission for both on-board and inter-board links operating at up to 25 Gbps. Testing is performed using Xilinx IBERT (Integrated Bit-Error-Rate Testing).

The setup is shown I the figure below, composed by:

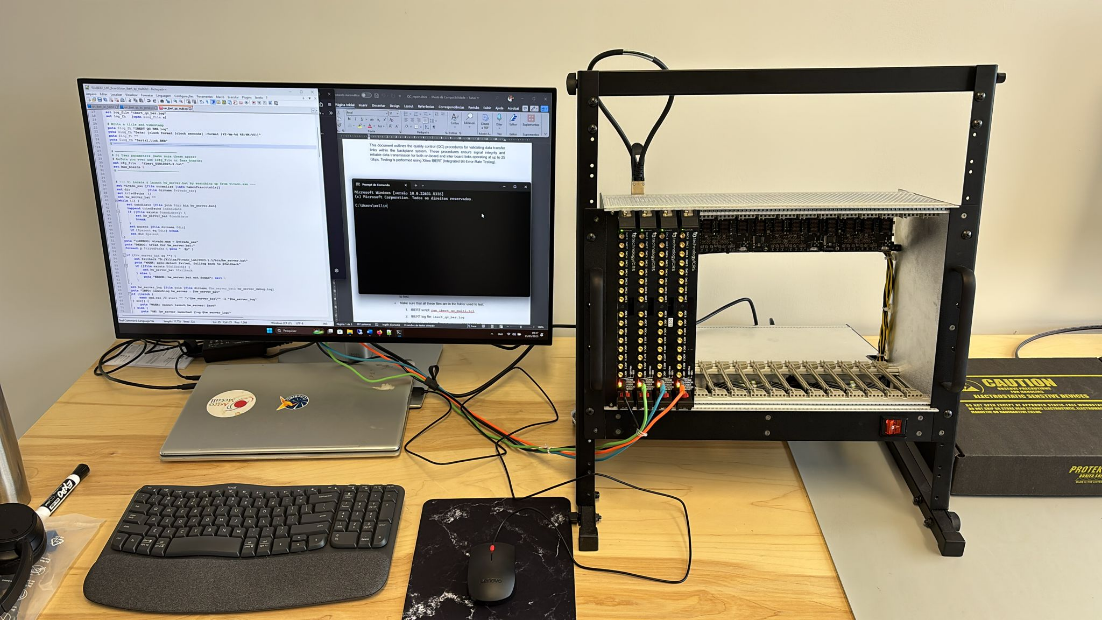


Figure - Testing setup for QC procedures for high-speed backplane links.

* Computer with 4 USB ports available.
* VIVADO Lab Installed.
* Crate with backplane boards installed.
* 4 CRS board, configured to JTAG programming
* 4 micro-USB cable

## 1. Overview of Bit Error Rate Testing

Bit-Error-Rate Testing is a method for assessing the integrity of high-speed digital links. The test transmits a known 31-bit data pattern (31-bit PRBS) across the physical link and compares the received data to identify any bit mismatches.

**Key Parameters:**

* **Test pattern:** PRBS31 (recommended for stress testing)
* **Target BER:** ≤ 10⁻¹²
* **Test duration:** ≥ 60 seconds or based on required confidence level

## 2. On-Board Link Quality Control

### 2.1 Metric Used

* **Bit Error Rate (BER):** Number of erroneous bits / total bits transmitted
* **Eye Diagram analysis (optional):** For visual assessment of signal quality

### 2.2 Test Procedure for 4-slot onboard Links

#### Preparation:

* + Make sure there is VIVADO Lab tools installed in a host computer used to test.
  + Make sure that all these files are in the folder used to test:
    1. IBERT script: run\_ibert\_qc\_multi.tcl (run\_ibert\_qc\_multi\_linux.tcl for Linux SO)
    2. IBERT log file: ibert\_qc\_ber.log
    3. and “links to be tested” file: e.g. ibert\_05012025-2.txt
    4. FPGA bitfile: example\_ibert\_ultrascale\_gty\_0.bit
  + Connect test equipment: 4 CRS boards(set to JTAG programming) connected on 1-slot BP board rev 1 (as shown in the figure).
  + Each CRS board is connected to the host computer (in case reduced available number of ports, consider use a 4-port USB expander ).
  + Power up the crate.

#### Test Execution:

* + Open Windows POWERSHELL
  + Go to directory: …/IBERT\_CRS\_Boards
  + On the prompt, run the following commands:

For Windows:

& “D:\Xilinx\Vivado\_Lab\2023.1.1\bin\vivado\_lab.bat" -mode batch -nojournal -nolog `

-source run\_ibert\_qc\_multi.tcl -log multi\_run.log

For Linux:

/home/lab/Xilinx/Vivado\_lab/2024.2/bin/vivado\_lab -mode batch -source run\_ibert\_qc\_multi\_linux.tcl -log -nojournal -nolog `

* + The test takes around 3 min, and then the results are located on ibert\_qc\_ber\_log, listed per date.

obs: If you are using complete version of VIVADO, replace “vivado\_lab.bat” to “vivado.bat”

#### Pass/Fail Criteria:

* + BER ≤ 10⁻¹²
  + No continuous bit errors observed
  + Optional: Eye opening ≥ recommended threshold (based on receiver margin)

## 3. Reporting Results

* **Template:**

**IBERT QC BER Log**

**Date: 2025-05-01 18:04:45**

|  |  |  |
| --- | --- | --- |
| IBERT QC BER Log | | |
| Date: 2025-05-01 18:04:45 | |  |
|  |  |  |
| Serial | Link | BER |
| 000043A | Quad\_131/MGT\_X0Y18/TX->Quad\_131/MGT\_X0Y18/RX | 2,90E-10 |
| 000043A | Quad\_131/MGT\_X0Y16/TX->Quad\_131/MGT\_X0Y16/RX | 1,02E-09 |
| 000043A | Quad\_130/MGT\_X0Y14/TX->Quad\_130/MGT\_X0Y14/RX | 1,99E-09 |
| 000025A | Quad\_131/MGT\_X0Y18/TX->Quad\_131/MGT\_X0Y18/RX | 5,02E-08 |
| 000025A | Quad\_131/MGT\_X0Y16/TX->Quad\_131/MGT\_X0Y16/RX | 2,17E-07 |
| 000025A | Quad\_130/MGT\_X0Y14/TX->Quad\_130/MGT\_X0Y14/RX | 5,44E-07 |
| 00021A | Quad\_131/MGT\_X0Y18/TX->Quad\_131/MGT\_X0Y18/RX | 7,34E-10 |
| 00021A | Quad\_131/MGT\_X0Y16/TX->Quad\_131/MGT\_X0Y16/RX | 6,42E-12 |
| 00021A | Quad\_130/MGT\_X0Y14/TX->Quad\_130/MGT\_X0Y14/RX | 4,76E-12 |
| 000047A | Quad\_131/MGT\_X0Y18/TX->Quad\_131/MGT\_X0Y18/RX | 2,28E-06 |
| 000047A | Quad\_131/MGT\_X0Y16/TX->Quad\_131/MGT\_X0Y16/RX | 6,62E-10 |
| 000047A | Quad\_130/MGT\_X0Y14/TX->Quad\_130/MGT\_X0Y14/RX | 2,82E-07 |