University of California Irvine

EECS 31L: Introduction to Digital Logic Laboratory (Spring 2024)

Lab 5: Single Cycle Risc V Processor

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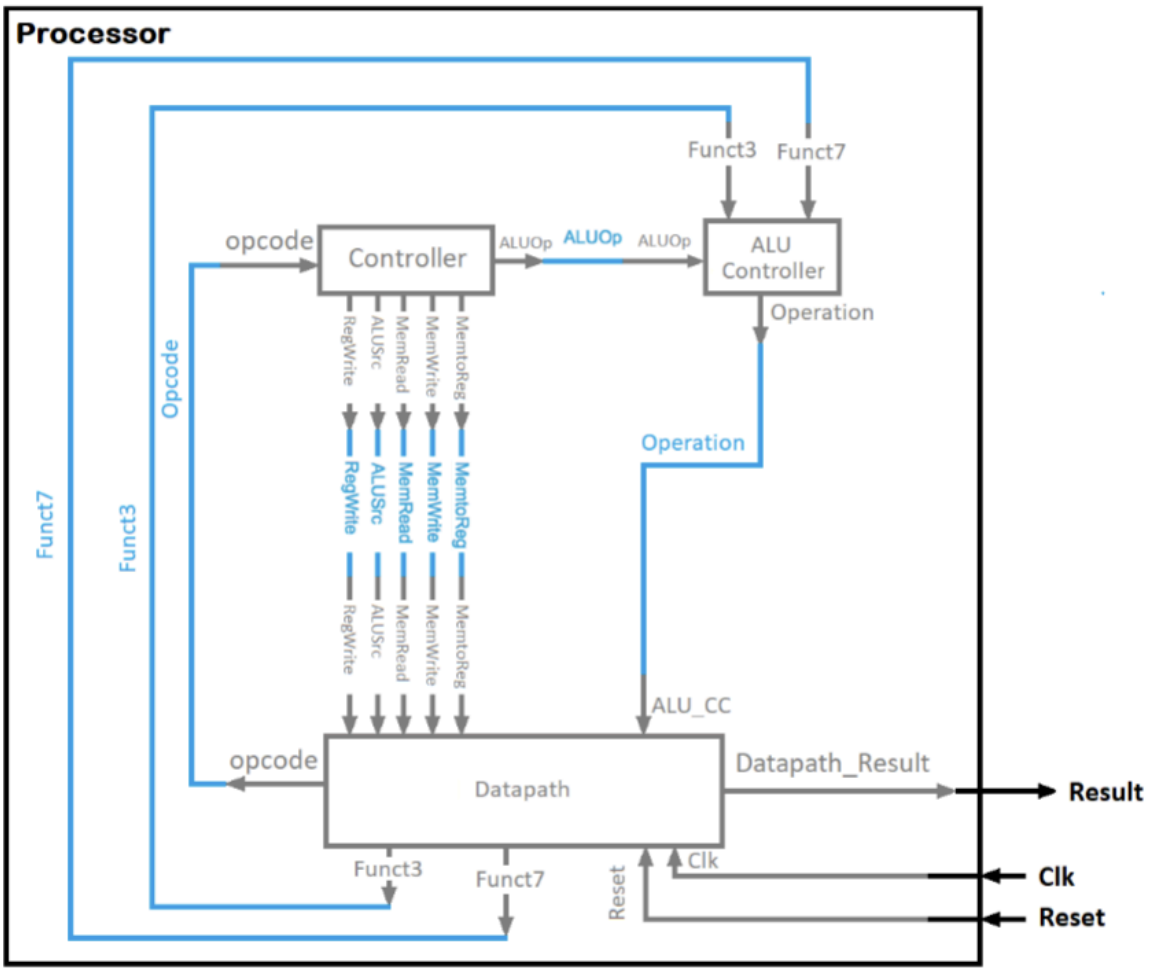
1. Overview

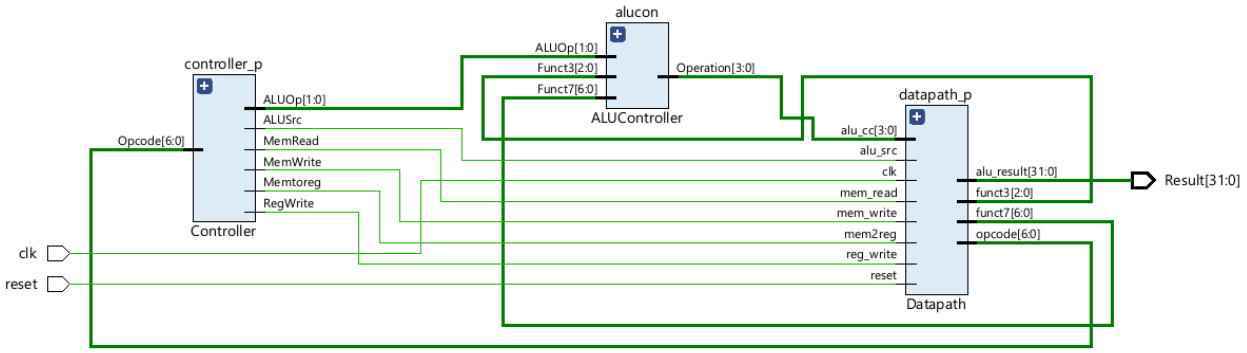
Give a summary or a high-level overview of the design. Use a block diagram for your design to explain inputs, outputs and the relation between them. If your design has more than one module, explain how they are related.



The module takes clock and reset inputs which are fed into datapath, and outputs a 32 bit result. Within are modules to control what operation is performed based on stored instruction memory.

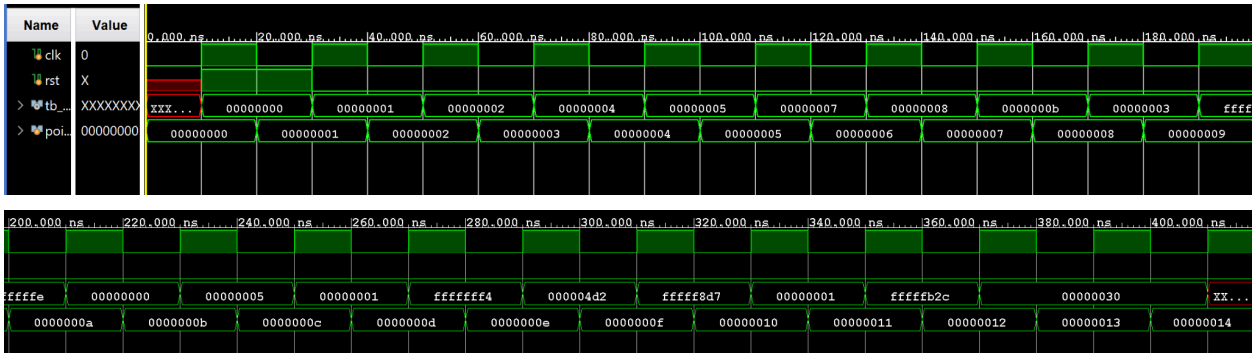
2. Hardware Design

In this section describe how you design your hardware modules. If necessary, you may show some Verilog code samples. A truth table helps to find the Boolean equation (if you want to use logical operators), or in general the relation between inputs and outputs. For more complex designs you can also draw the schematic of your design. The schematic of design includes the components of the design and their connectivity. You can use any software like PowerPoint to draw your figures.

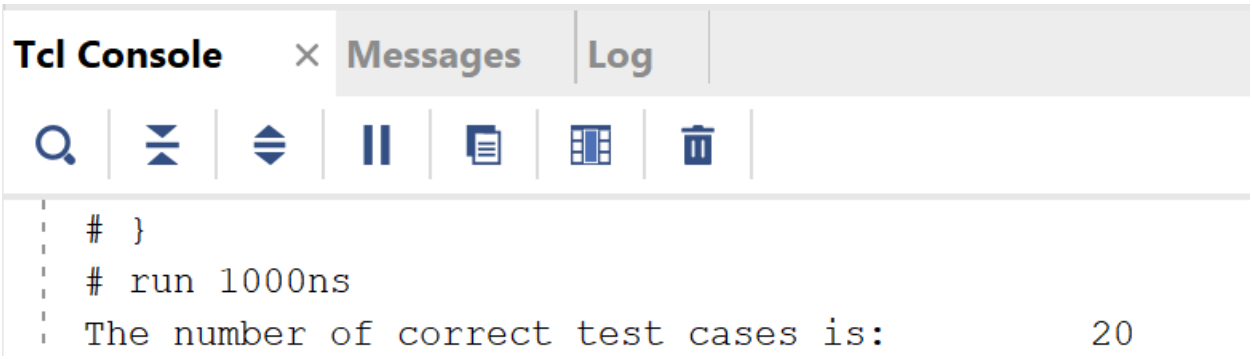


3. Simulation Results

Show your simulation results here. Explain your test cases and how you design them to cover all combinations of inputs. Put screenshots of your simulation here. You may need to put more than one image if necessary. Also, define the signals in the screenshots and explain how and when the input changes cause changes in the output. If there is something different from what you expect, explain why.



console display says I got all the correct test cases


Tcl Console
Messages
Log
}
run 1000ns
The number of correct test cases is: 20