🎎 atv05 - Symphony EDA Sonata 3.1 - [C:/Users/welly/Documents/GitHub/LT38A/pratica05/simili/enable.vhdl] File Edit Project Compile Simulate Window Help | D 🚅 🔲 🗿 | 从 🗈 🖺 | 🚉 🥨 | 🥰 🕮 🕮 🔯 | № 🎉 🔼 | 💆 🚟 🕮 | 針 🚉 🕨 🕨 | 100 us PPRH BEOGOGOXX Workspace: Work = atv05 1 entity enable is Toplevel = testarquitetura 2 port ( 🗎 🌃 Workspace 'atv05' Files 3 temp: in bit\_vector(7 downto 0); Library ieee => \$SYMPHONYEDA/li 4 en: in bit; Library atv05 => C:/Users/w

stateconverter.vhdl
inib.vhdl 5 S: out bit\_vector(7 downto 0) 6 ); 7 end entity; enable.vhdl 8 sevenSegDecoder.vhdl display.vhdl 9 architecture behavior of enable is 10 ⊕ arquitetura.vhdl **+**---testArquitetura.vhdl 11 begin testEnable.vhdl **+**---12 testInib.vhdl S <= temp when en = '1' else "00000000"; 13 testStateConverter.vhdl 14 15 end architecture; 16

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