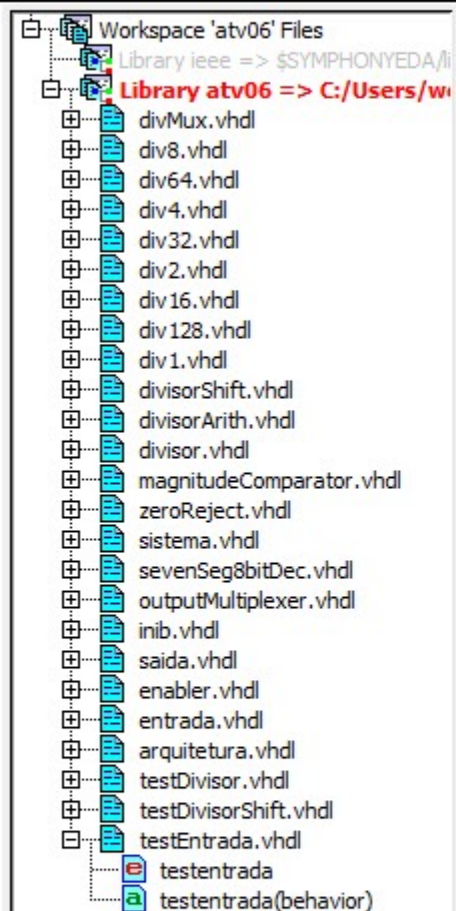




Workspace: Work = atv06
Toplevel = testentrada



```

1  library ieee;
2  use ieee.numeric_std.all;
3  use ieee.std_logic_1164.all;
4
5  entity testEntrada is
6
7  end entity;
8
9  architecture behavior of testEntrada is
10
11      component entrada is
12      port(
13          A,B: in unsigned(7 downto 0);
14          En: in bit;
15          Ae,Be: out unsigned(7 downto 0)
16      );
17  end component;
18
19      signal A,B: unsigned(7 downto 0);
20      signal En: bit;
21      signal Ae,Be: unsigned(7 downto 0);
22  begin
23
24      ent: entrada port map(A,B,En,Ae,Be);
25
26      process
27      begin
28
29          A <= x"00"; B <= x"00"; En <= '1'; wait for 50 ns;
30          A <= x"aa"; B <= x"66"; En <= '1'; wait for 50 ns;
31          A <= x"ff"; B <= x"66"; En <= '0'; wait for 50 ns;
32          A <= x"aa"; B <= x"66"; En <= '1'; wait for 50 ns;
33
34      end process;
35
36  end architecture;
37

```