```
👺 atv05 - Symphony EDA Sonata 3.1 - [C:/Users/welly/Documents/GitHub/LT38A/pratica05/simili/testEnable.vhdl]
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                                                                        Workspace: Work = atv05
                                 1
                                     entity testEnable is
Toplevel = testarquitetura
                                 2
                                     end entity;
🗀 : 🚯 Workspace 'atv05' Files
                                 3
   Library ieee => $SYMPHONYEDA/li
                                 4
                                      architecture behavior of testEnable is
  ☐ FE Library atv05 => C:/Users/w
                                 5
   ⊞ stateconverter.vhdl
                                 6
                                               component enable is
   inib.vhdl
                                 7
                                                        port (
   enable.vhdl
                                 8
                                                                 temp: in bit vector (7 downto 0);
   ⊕ sevenSegDecoder.vhdl
                                 9
                                                                 en: in bit;
   display.vhdl
                               10
                                                                 S: out bit vector (7 downto 0)
   ⊕.... arquitetura.vhdl
   testArquitetura.vhdl
                               11
                                                        );
   testEnable.vhdl
                               12
                                               end component;
   testInib.vhdl
                                13
   testStateConverter.vhdl
                                14
                                               signal temp: bit vector (7 downto 0);
                                               signal en: bit;
                               15
                                               signal S: bit vector (7 downto 0);
                               16
                               17
                               18
                                     begin
                               19
                               20
                                               ena: enable port map(temp,en,S);
                               21
                               22
                                               process
                                23
                                               begin
                               24
                                                        temp <= x"00"; en <= '1'; wait for 50 ns;
                                25
                                                        temp <= x"00"; en <= '0'; wait for 50 ns;
                               26
                               27
                                                        temp <= x"66"; en <= '1'; wait for 50 ns;
                                                        temp <= x"66"; en <= '0'; wait for 50 ns;
                               28
                               29
                               30
                                               end process;
                               31
                               32
                                     end architecture;
                               33
```