```
| □ 🚅 🖫 🗿 | % 🛍 🛍 | 🚅 🕮 🕮 🕮 🗭 | 100 us
                                                                      Workspace: Work = atv05
Toplevel = testarquitetura
                                    entity stateConverter is
                                2
                                             port (
⊕ Workspace 'atv05' Files
                                3
                                                      temp: in bit_vector(7 downto 0);
                                4
                                                       state: out bit_vector(2 downto 0);
  Library atv05 => C:/Users/w
                                                      transition: out bit_vector(2 downto 0)
                                5
   stateconverter.vhdl
                                6
                                             );
                                7
                                    end entity;
   enable.vhul
sevenSegDecoder.vhdl
display.vhdl
arquitetura.vhdl
                                8
                                     architecture behavior of stateConverter is
                                9
                               10
   testArquitetura.vhdl
testEnable.vhdl
testInib.vhdl
testStateConverter.vhdl
                               11
                               12
                               13
                                             state <= "000" when temp >= "00000000" and temp < "00001010" else
                                                       "001" when temp > "00001010" and temp < "00010100" else
                               14
                                                        "010" when temp > "00010100" and temp < "00011110" else
                               15
                                                        "011" when temp > "00011110" and temp < "00111100" else
                               16
                                                        "100" when temp > "00111100";
                               17
                               18
                                                              "001" when temp = "00001010" else
                               19
                                             transition <=
                               20
                                                               "010" when temp = "00010100" else
                                                               "011" when temp = "00011110" else
                               21
                               22
                                                               "100" when temp = "00111100" else
                                                               "000";
                               23
                               24
                               25
                                     end architecture;
                               26
                              27
```