💥 atv05 - Symphony EDA Sonata 3.1 - [C:/Users/welly/Documents/GitHub/LT38A/pratica05/simili/testInib.vhdl] <u>File Edit Project Compile Simulate Window Help</u> || 🗅 🚅 🔚 🚮 | 从 🗈 🛍 | 🚅 🤐 | 🥶 🏭 | 🎛 | № 🎉 | № 🎉 | 🛂 🛗 | 🖭 | 🔡 | ▶ ▶ | 100 us K 🛨 💢 📶 P P P R H | B B O O O O O O 🕶 entity testInib is Workspace: Work = atv05 1 Toplevel = testarquitetura 2 end entity; Workspace 'atv05' Files
Library ieee => \$SYMPHONYEDA/li 3 architecture behavior of testInib is 4 Library atv05 => C:/Users/w 5 stateconverter.vhdl 6 component inib is 7 port (enable.vhdl 8 ss: in bit vector(6 downto 0); sevenSegDecoder.vhdl ₽---9 inib: in bit; Ė.... display.vhdl 10 S: out bit_vector(6 downto 0) arquitetura.vhdl testArquitetura.vhdl 11); **+**---testEnable.vhdl 12 end component; testInib.vhdl 13 testStateConverter.vhdl signal ss: bit vector(6 downto 0); 14 15 signal iniba: bit; 16 signal S: bit vector (6 downto 0); 17 18 begin 19 20 ini: inib port map(ss,iniba,S); 21 22 process 23 begin 24 ss <= "00000000"; iniba<= '0'; wait for 50 ns; 25 ss <= "1010101"; iniba<= '0'; wait for 50 ns; 26 ss <= "11111111"; iniba<= '0'; wait for 50 ns; 27 ss <= "00000000"; iniba<= '1'; wait for 50 ns; 28 ss <= "1010101"; iniba<= '1'; wait for 50 ns; 29 ss <= "11111111"; iniba<= '1'; wait for 50 ns; 30 31

end process;

end architecture;

32

33

35