🕻 atv05 - Symphony EDA Sonata 3.1 - [C:/Users/welly/Documents/GitHub/LT38A/pratica05/simili/inib.vhdl] File Edit Project Compile Simulate Window Help 🗅 🚅 🔚 🗿 | % 🛍 🛍 | 🚉 🕮 | 🕮 🕮 🕮 🕮 | 🖎 🎥 | 🖺 🖺 🕨 🕨 🕨 100 us /orkspace: Work = atv05 oplevel = testarquitetura entity inib is 2 Workspace 'atv05' Files
Library ieee => \$SYMPHONYEDA/li 3 ssState, ssTransition: in bit_vector(6 downto 0); 4 ssTemp0, ssTemp1, ssTemp2: in bit_vector(6 downto 0); Library atv05 => C:/Users/w 5 inib: in bit; stateconverter.vhdl
inib.vhdl
enable.vhdl
sevenSegDecoder.vhdl
display.vhdl
arquitetura.vhdl 6 outssState, outssTransition: out bit vector(6 downto 0); 7 outssTemp0, outssTemp1, outssTemp2: out bit_vector(6 downto 0) 8); 9 end entity; 10 testEnable.vhdl
testInib.vhdl
testStateConverter.vhdl Ė.... architecture behavior of inib is 11 **+**----12 13 begin 14 outssState <= ssState when inib = '0' else "1111111"; 15 outssTransition <= ssTransition when inib = '0' else "1111111"; 16 outssTemp0 <= ssTemp0 when inib = '0' else "1111111"; outssTemp1 <= ssTemp1 when inib = '0' else "11111111";</pre> 17 18 outssTemp2 <= ssTemp2 when inib = '0' else "1111111"; 19 20 21 end architecture; 22 23 24