atv05 - Symphony EDA Sonata 3.1 - [C:/Users/welly/Documents/GitHub/LT38A/pratica05/simili/testInib.vhdl]

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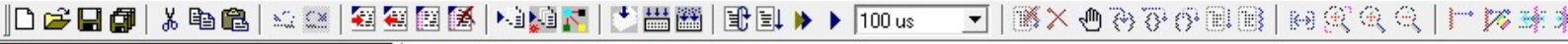
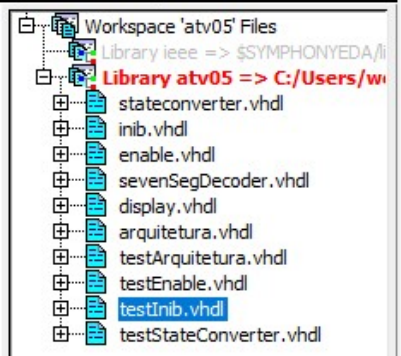


Workspace: Work = atv05
Toplevel = testarquitetura




```
1  entity testInib is
2  end entity;
3
4  architecture behavior of testInib is
5
6          component inib is
7                  port(
8                          ss: in bit_vector(6 downto 0);
9                          inib: in bit;
10                         S: out bit_vector(6 downto 0)
11                 );
12         end component;
13
14         signal ss: bit_vector(6 downto 0);
15         signal iniba: bit;
16         signal S: bit_vector(6 downto 0);
17
18 begin
19
20         ini: inib port map(ss,iniba,S);
21
22         process
23         begin
24
25                 ss <= "0000000"; iniba<= '0'; wait for 50 ns;
26                 ss <= "1010101"; iniba<= '0'; wait for 50 ns;
27                 ss <= "1111111"; iniba<= '0'; wait for 50 ns;
28                 ss <= "0000000"; iniba<= '1'; wait for 50 ns;
29                 ss <= "1010101"; iniba<= '1'; wait for 50 ns;
30                 ss <= "1111111"; iniba<= '1'; wait for 50 ns;
31
32         end process;
33
34 end architecture;
35
```