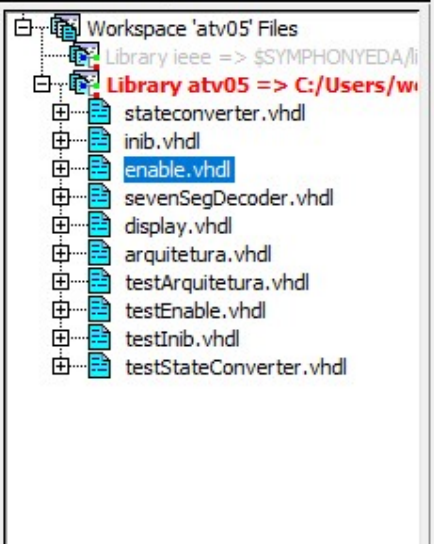
atv05 - Symphony EDA Sonata 3.1 - [C:/Users/welly/Documents/GitHub/LT38A/pratica05/simili/enable.vhdl]

File Edit Project Compile Simulate Window Help

Workspace: Work = atv05
Toplevel = testarquitetura




```
1   entity enable is
2           port(
3                   temp: in bit_vector(7 downto 0);
4                   en: in bit;
5                   S: out bit_vector(7 downto 0)
6           );
7   end entity;
8
9   architecture behavior of enable is
10
11  begin
12
13          S <= temp when en = '1' else "00000000";
14
15  end architecture;
16
17
```