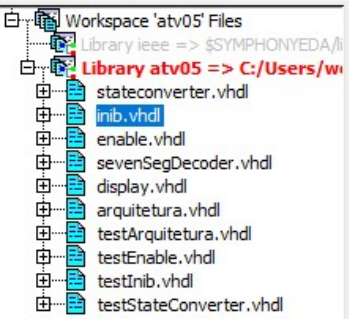
atv05 - Symphony EDA Sonata 3.1 - [C:/Users/welly/Documents/GitHub/LT38A/pratica05/simili/inib.vhdl]

File Edit Project Compile Simulate Window Help

Workspace: Work = atv05
oplevel = testarquitetura




```vhdl
entity inib is
        port(
                ssState, ssTransition: in bit_vector(6 downto 0);
                ssTemp0,ssTemp1,ssTemp2: in bit_vector(6 downto 0);
                inib: in bit;
                outssState, outssTransition: out bit_vector(6 downto 0);
                outssTemp0,outssTemp1,outssTemp2: out bit_vector(6 downto 0)
        );
end entity;

architecture behavior of inib is

begin

        outssState <= ssState when inib = '0' else "1111111";
        outssTransition <= ssTransition when inib = '0' else "1111111";
        outssTemp0 <= ssTemp0 when inib = '0' else "1111111";
        outssTemp1 <= ssTemp1 when inib = '0' else "1111111";
        outssTemp2 <= ssTemp2 when inib = '0' else "1111111";

end architecture;
```