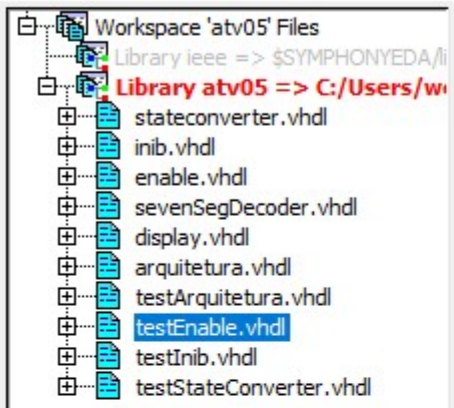
atv05 - Symphony EDA Sonata 3.1 - [C:/Users/welly/Documents/GitHub/LT38A/pratica05/simili/testEnable.vhdl]

File Edit Project Compile Simulate Window Help


Workspace: Work = atv05
Toplevel = testarquitetura




```
1  entity testEnable is
2  end entity;
3
4  architecture behavior of testEnable is
5
6          component enable is
7                  port(
8                          temp: in bit_vector(7 downto 0);
9                          en: in bit;
10                         S: out bit_vector(7 downto 0)
11                 );
12         end component;
13
14         signal temp: bit_vector(7 downto 0);
15         signal en: bit;
16         signal S: bit_vector(7 downto 0);
17
18 begin
19
20         ena: enable port map(temp,en,S);
21
22         process
23         begin
24
25                 temp <= x"00"; en <= '1'; wait for 50 ns;
26                 temp <= x"00"; en <= '0'; wait for 50 ns;
27                 temp <= x"66"; en <= '1'; wait for 50 ns;
28                 temp <= x"66"; en <= '0'; wait for 50 ns;
29
30         end process;
31
32 end architecture;
33
```