Html generated by Symphony EDA Sonata for 'C:/Users/welly/Documents/GitHub/LT38A/pratica06/simili/saida.vhdl'
Source file last modified on Tue Nov 07 22:14:56 Hora oficial do Brasil 2023
Note: Use IE 5+ or Netscape 6+ or Mozilla Firefox for best results

```
 1  library ieee;
 2  use ieee.numeric_std.all;
 3  use ieee.std_logic_1164.all;
 4
 5  entity saida is
 6      port(
 7          dividendo,divisor: in unsigned(7 downto 0);
 8          quociente,resto: in std_logic_vector(7 downto 0);
 9          sel: in bit_vector(1 downto 0);
10          inibi: in bit;
11
12          inibedsevenSeg0,inibedsevenSeg1,inibedsevenSeg2: out std_logic_vector(6 downto 0)
13      );
14  end entity;
15
16  architecture behavior of saida is
17
18      component sevenSeg8bitDec is
19          port(
20              A: in std_logic_vector(7 downto 0);
21              ssA0,ssA1,ssA2: out std_logic_vector(6 downto 0)
22          );
23      end component;
24
25      component outputMultiplexer is
26          port(
27              A,B,C,D: in std_logic_vector(6 downto 0);
28              sel: in bit_vector(1 downto 0);
29              S: out std_logic_vector(6 downto 0)
30          );
31      end component;
32
33      component inib is
34          port(
35              sevenSeg0,sevenSeg1,sevenSeg2: in std_logic_vector(6 downto 0);
36              inib: in bit;
37              inibedsevenSeg0,inibedsevenSeg1,inibedsevenSeg2: out std_logic_vector(6 downto 0)
38          );
39      end component;
40
41      signal ssA0,ssA1,ssA2: std_logic_vector(6 downto 0);
42      signal ssB0,ssB1,ssB2: std_logic_vector(6 downto 0);
43      signal ssC0,ssC1,ssC2: std_logic_vector(6 downto 0);
44      signal ssD0,ssD1,ssD2: std_logic_vector(6 downto 0);
45
46      signal sevenSeg0,sevenSeg1,sevenSeg2: std_logic_vector(6 downto 0);
47
48  begin
49
50      dividendoDecoder: sevenSeg8bitDec port map(std_logic_vector(dividendo),ssA0,ssA1,ssA2);
51      divisorDecoder: sevenSeg8bitDec port map(std_logic_vector(divisor),ssB0,ssB1,ssB2);
52      quocienteDecoder: sevenSeg8bitDec port map(quociente,ssC0,ssC1,ssC2);
53      restoDecoder: sevenSeg8bitDec port map(resto,ssD0,ssD1,ssD2);
54
55      mux0: outputMultiplexer port map(ssA0,ssB0,ssC0,ssD0,sel,sevenSeg0);
56      mux1: outputMultiplexer port map(ssA1,ssB1,ssC1,ssD1,sel,sevenSeg1);
57      mux2: outputMultiplexer port map(ssA2,ssB2,ssC2,ssD2,sel,sevenSeg2);
58
59      inibidor: inib port map(sevenSeg0,sevenSeg1,sevenSeg2,inibi,inibedsevenSeg0,inibedsevenSeg1,inibedsevenSeg2);
60
61
62
63  end architecture;
64
65
```

Note: Modifying your display preferences for the text editor in Sonata will correspondingly modify the look and feel of the generated HTML file. Also, to properly print background colors, you may have to enable a setting in your browser (especially IE users).