```
Html generated by <u>Symphony EDA</u> Sonata for 'C:/Users/welly/Documents/GitHub/LT38A/pratica05/simili/arquitetura.vhdl' Source file last modified on Thu Oct 19 23:53:20 Hora oficial do Brasil 2023
Note: Use IE 5+ or Netscape 6+ or Mozilla Firefox for best results
     entity arquitetura is
         port (
               temp: in bit_vector(7 downto 0);
                        en: in bit;
              inibicao: in bit;
               outssState, outssTransition: out bit_vector(6 downto 0);
 9
               outssTemp0, outssTemp1, outssTemp2: out bit_vector(6 downto 0)
10
11
          );
     end entity;
12
13
14
     architecture behavior of arquitetura is
15
          component enable is
              port(
17
18
                   temp: in bit_vector(7 downto 0);
19
                    en: in bit;
20
                   S: out bit vector(7 downto 0)
21
               );
          end component;
23
24
          signal S: bit vector(7 downto 0);
2.5
26
          component stateConverter is
27
              port (
                    temp: in bit vector(7 downto 0);
29
                    state: out bit_vector(2 downto 0);
30
                    transition: out bit vector(2 downto 0)
31
              ) :
          end component;
32
33
          signal state: bit_vector(2 downto 0);
signal transition: bit_vector(2 downto 0);
34
37
          component display is
              port(
38
                   etemp: in bit vector(7 downto 0);
39
                   state, transition: in bit_vector(2 downto 0);
40
41
                    ssState, ssTransition: out bit vector(6 downto 0);
43
                    ssTemp0, ssTemp1, ssTemp2: out bit_vector(6 downto 0)
44
              );
45
          end component;
46
          signal ssState, ssTransition: bit vector(6 downto 0);
48
          signal ssTemp0,ssTemp1,ssTemp2: bit vector(6 downto 0);
50
          component inib is
              port(
51
                   ssState, ssTransition: in bit_vector(6 downto 0);
ssTemp0,ssTemp1,ssTemp2: in bit_vector(6 downto 0);
52
53
                    inib: in bit;
                   outssState, outssTransition: out bit_vector(6 downto 0);
                        outssTemp0,outssTemp1,outssTemp2: out bit_vector(6 downto 0)
57
58
          end component;
59
60
62
          enable0: enable port map(temp,en,S);
          stateConverter0: stateConverter port map(S, state, transition);
64
          display0: display port map(S, state, transition, ssState, ssTransition, ssTemp0, ssTemp1, ssTemp2);
6.5
          inib0: inib port map(ssState,ssTransition,ssTemp0,ssTemp1,ssTemp2,inibicao,outssState,outssTransition,outssTemp0,
66
67
     end architecture;
```

Note: Modifying your display preferences for the text editor in Sonata will correspondingly modify the look and feel of the generated HTML file. Also, to properly print background colors, you may have to enable a setting in your browser (especially IE users).

