atv06 - Symphony EDA Sonata 3.1 - [C:/Users/welly/Documents/GitHub/LT38A/pratica06/simili/sistema.vhdl]

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Workspace: Work = atv06
Toplevel = testsistema

- Workspace 'atv06' Files
  - Library ieee => $SYMPHONYEDA/li
  - **Library atv06 => C:/Users/w**
    - divMux.vhdl
    - div8.vhdl
    - div64.vhdl
    - div4.vhdl
    - div32.vhdl
    - div2.vhdl
    - div16.vhdl
    - div128.vhdl
    - div1.vhdl
    - divisorShift.vhdl
    - divisorArith.vhdl
    - divisor.vhdl
    - magnitudeComparator.vhdl
    - zeroReject.vhdl
    - sistema.vhdl
    - sevenSeg8bitDec.vhdl
    - outputMultiplexer.vhdl
    - inib.vhdl
    - saida.vhdl
    - enabler.vhdl
    - entrada.vhdl
    - arquitetura.vhdl
    - testDivisor.vhdl
    - testDivisorShift.vhdl
    - testEntrada.vhdl
      - testentrada
      - testentrada(behavior)
    - testSistema.vhdl
      - testsistema
      - testsistema(behavior)

```
1  library ieee;
2  use ieee.numeric_std.all;
3  use ieee.std_logic_1164.all;
4
5  entity sistema is
6      port(
7          A,B: in unsigned(7 downto 0);
8          Q,R: out std_logic_vector(7 downto 0)
9      );
10 end entity;
11
12 architecture behavior of sistema is
13
14     component zeroReject is
15         port(
16             A,B: in unsigned(7 downto 0);
17             Q,R: out std_logic_vector(7 downto 0)
18         );
19     end component;
20
21 begin
22
23     zr: zeroReject port map(A,B,Q,R);
24
25 end architecture;
```