

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.numeric_std.ALL;
4
5  entity ClockDivider is
6      port ( clk: in std_logic;
7            clock_out: out std_logic);
8  end entity;
9
10 architecture behavior of ClockDivider is
11
12     signal count: integer:=1;
13     signal tmp : std_logic := '0';
14
15     signal oscillator: integer := 50000000;
16     signal newfrequency: integer := 1;
17
18 begin
19     process(clk)
20
21         variable halfPeriod: integer := (oscillator)/(newfrequency*2);
22
23     begin
24
25         if(clk'event and clk='1') then
26             count <= count+1;
27             if (count > halfPeriod) then -- usar 2500000 na FPGA
28                 tmp <= NOT tmp;
29                 count <= 1;
30             end if;
31         end if;
32         clock_out <= tmp;
33     end process;
34
35 end architecture;
```