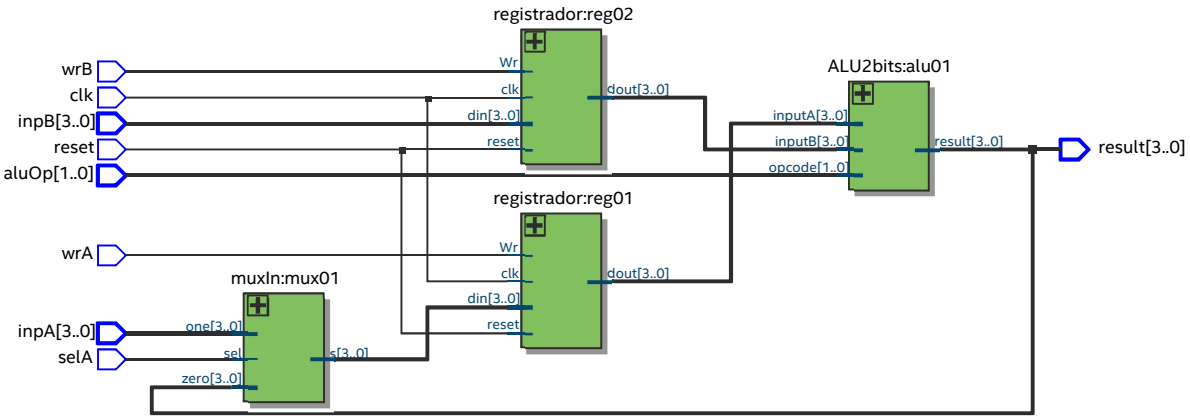
```
1   module operacional (
2       input wire[3:0] inpA,inpB,
3       input wire clk, reset,
4
5       input wire selA,wrA,wrB,
6       input wire[1:0] aluOp,
7
8       output wire[3:0] result
9   );
10
11      wire[3:0] outMux;
12      muxIn mux01 (.zero(result), .one(inpA), .sel(selA), .s(outMux));
13
14      wire[3:0] outReg01, outReg02;
15      registrador reg01 (clk,reset,wrA,outMux,outReg01);
16      registrador reg02 (clk,reset,wrB,inpB,outReg02);
17
18      ALU2bits alu01 (outReg01,outReg02,aluOp,result);
19
20  endmodule
```

```
1   module muxIn (
2       input wire[3:0] zero, one,
3       input wire sel,
4       output reg[3:0] s
5   );
6       always @(sel) begin
7           if(sel) begin
8               s = one;
9           end else begin
10              s = zero;
11          end
12      end
13  endmodule
```

```
1   module registrador (
2       input wire clk,
3       input wire reset,
4       input wire Wr,
5       input wire [3:0] din,
6       output reg [3:0] dout
7   );
8
9       always @(posedge clk or posedge reset) begin
10          if (reset) begin
11              dout <= 4'b0000;
12          end else begin
13              if (Wr) begin
14                  dout <= din;
15              end
16          end
17      end
18
19  endmodule
```

```
1   module ALU2bits (
2       input wire [3:0] inputA, // 4-bit input A
3       input wire [3:0] inputB, // 4-bit input B
4       input wire [1:0] opcode, // 2-bit opcode
5       output reg [3:0] result   // 4-bit output result
6   );
7
8       wire[3:0]Q,R;
9       Divisor Divisor01(Q,R,inputA,inputB);
10      always @(*) begin
11          case (opcode)
12              2'b00: begin
13                   result = inputA;
14              end
15              2'b01: begin
16                  result = inputB;
17              end
18
19              2'b10: begin
20                  result = Q;
21              end
22
23              2'b11: begin
24                  result = R;
25              end
26
27              default: begin
28                  result = 4'b0000;
29              end
30          endcase
31      end
32
33  endmodule
```


registrador:reg02
wrB
clk
inpB[3..0]
reset
aluOp[1..0]
Wr
clk
din[3..0]
reset
dout[3..0]
ALU2bits:alu01
inputA[3..0]
inputB[3..0]
opcode[1..0]
result[3..0]
result[3..0]
registrador:reg01
wrA
Wr
clk
din[3..0]
reset
dout[3..0]
muxIn:mux01
inpA[3..0]
selA
one[3..0]
sel
zero[3..0]
s[3..0]

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Master Time Bar: 0 ps Pointer: 425.18 ns Interval: 425.18 ns Start: End:

Name	Value at 0 ps
clk	B 0
inpA	B 1101
inpB	B 0110
aluOp	B 00
reset	B 1
selA	B 0
wrA	B 0
wrB	B 0
result	B 0000