



```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  USE ieee.numeric_std.all;
4
5  entity ULA is
6      port
7      (
8          A,B: in unsigned(3 downto 0);
9          ALUop: in std_logic_vector(1 downto 0);
10
11          ALUout: out unsigned(4 downto 0)
12      );
13  end entity;
14
15  architecture behavior of ULA is
16
17  component Somador is
18      port
19      (
20          A,B: in unsigned(3 downto 0);
21
22          Sum: out unsigned(4 downto 0)
23      );
24  end component;
25
26  signal Sum: unsigned(4 downto 0);
27
28  begin
29
30      sum01: Somador port map(A,B,Sum);
31
32      with ALUop select ALUout <=
33          "00000" when "00",
34          ("0" & A)      when "01",
35          ("0" & B)      when "10",
36          Sum            when "11";
37
38  end architecture;
```