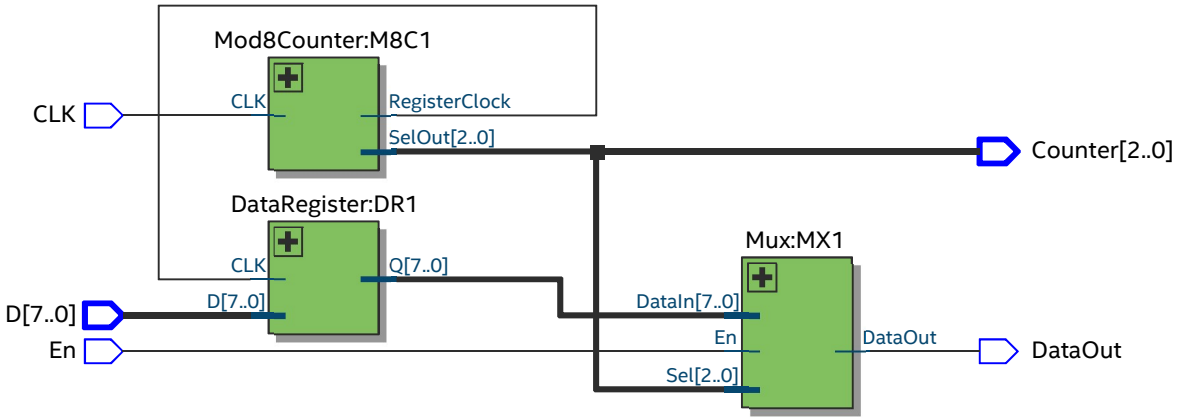
```vhdl
library ieee;
use ieee.numeric_std.all;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity sistema is
    port
    (
        CLK: in std_logic;
        D: in std_logic_vector(7 downto 0);
        En: in std_logic;

        DataOut: out std_logic;
        Counter: out std_logic_vector(2 downto 0)
    );
end entity;

architecture behavior of sistema is

    component DataRegister is
        Port(
            CLK: in std_logic;
            D: in std_logic_vector(7 downto 0);
            Q: out std_logic_vector(7 downto 0)
        );
    end component;
    signal Q: std_logic_vector(7 downto 0);

    component Mux is
        port(
            DataIn: in std_logic_vector(7 downto 0);
            Sel: in std_logic_vector(2 downto 0);
            En: in std_logic;
            DataOut: out std_logic
        );
    end component;

    component Mod8Counter is
        port
        (
            CLK: in std_logic;
            RegisterClock: out std_logic;
            SelOut: out std_logic_vector(2 downto 0)
        );
    end component;
    signal RegisterClock: std_logic;
    signal SelOut: std_logic_vector(2 downto 0);

begin

    DR1: DataRegister port map(RegisterClock,D,Q);
    MX1: Mux port map(Q,SelOut,En,DataOut);
    M8C1: Mod8Counter port map(CLK,RegisterClock,SelOut);

    Counter <= SelOut;

end architecture;

```


Mod8Counter:M8C1
CLK
CLK
RegisterClock
SelOut[2..0]
Counter[2..0]
DataRegister:DR1
CLK
Q[7..0]
D[7..0]
D[7..0]
Mux:MX1
DataIn[7..0]
En
DataOut
DataOut
En
Sel[2..0]

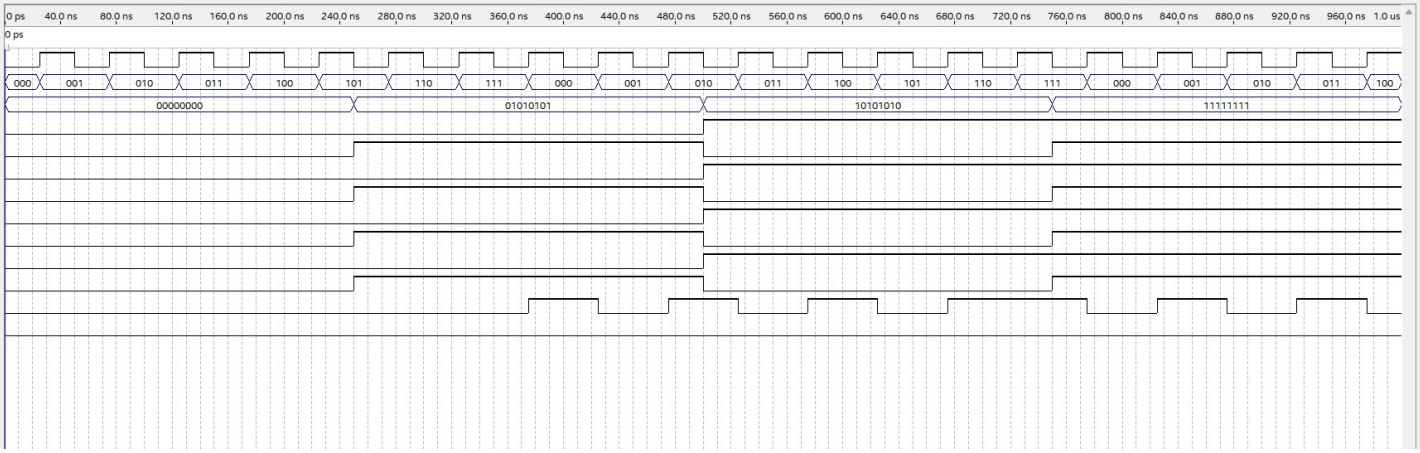
Simulation Waveform Editor - C:/Users/welly/Documents/GitHub/LT39A/pratica00/Quartus/atv00 - atv00 - [atv00_20240411210944.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: 229.49 ns Interval: 229.49 ns Start: End:

Name	Value at 0 ps
CLK	B 0
Counter	B 000
D	B 00000000
D[7]	B 0
D[6]	B 0
D[5]	B 0
D[4]	B 0
D[3]	B 0
D[2]	B 0
D[1]	B 0
D[0]	B 0
DataOut	B 0
En	B 0



Simulation Waveform Editor - C:/Users/welly/Documents/GitHub/LT39A/pratica00/Quartus/atv00 - atv00 - [atv00_20240411211012.sim.vwf (Read-Only)]

File Edit View Simulation Help

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Master Time Bar: 0 ps Pointer: 453.65 ns Interval: 453.65 ns Start: End:

Name	Value at 0 ps
CLK	B 0
Counter	B 000
D	B 00000000
D[7]	B 0
D[6]	B 0
D[5]	B 0
D[4]	B 0
D[3]	B 0
D[2]	B 0
D[1]	B 0
D[0]	B 0
DataOut	B 0
En	B 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

Counter: 000 001 010 011 100 101 110 111 000 001 010 011 100 101 110 111 000 001 010 011 100

D: 00000000 01010101 10101010 11111111