```
1   module RomPadrao (
2       input wire clock,
3       input wire[4:0] addr,
4
5       output reg[7:0] dataOut
6   );
7
8       reg[7:0] phrase [0:31];
9       initial begin
10          phrase[0]  = "A";
11          phrase[1]  = "i";
12          phrase[2]  = "n";
13          phrase[3]  = ":";
14          phrase[4]  = "X";      // Dezena Address
15          phrase[5]  = "X";      // Unidade Address
16          phrase[6]  = " ";
17          phrase[7]  = " ";
18          phrase[8]  = "S";
19          phrase[9]  = "t";
20          phrase[10] = "a";
21          phrase[11] = "t";
22          phrase[12] = "e";
23          phrase[13] = ":";
24          phrase[14] = "Y";      // R ou W
25          phrase[15] = " ";
26
27
28
29          phrase[16] = "D";
30          phrase[17] = "i";
31          phrase[18] = "n";
32          phrase[19] = ":";
33          phrase[20] = "X";      // Dezena DataTeclado
34          phrase[21] = "X";      // Unidade DataTeclado
35          phrase[22] = " ";
36          phrase[23] = " ";
37          phrase[24] = "D";
38          phrase[25] = "o";
39          phrase[26] = "u";
40          phrase[27] = "t";
41          phrase[28] = ":";
42          phrase[29] = "Y";      // Dezena DataMemoria
43          phrase[30] = "Y";      // Unidade DataMemoria
44          phrase[31] = " ";
45      end
46
47
48      always @(posedge clock ) begin
49          dataOut <= phrase[addr];
50      end
51
52  endmodule
```