



```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  USE ieee.numeric_std.all;
4
5  entity Sistema is
6      port
7      (
8          clock,reset: in std_logic;
9          InpA,InpB: in unsigned(3 downto 0);
10
11          ALUout: buffer unsigned(4 downto 0);
12          RegPrState,RegNxState: out std_logic_vector(1 downto 0)
13      );
14  end entity;
15
16  architecture behavior of Sistema is
17
18      component StateMachine_ControlUnit is
19          port
20          (
21              clock,reset: in std_logic;
22              dv: in std_logic;
23
24              RegSelA, RegWrA, RegWrB: out std_logic;
25              RegALUop: out std_logic_vector(1 downto 0);
26              RegPrState,RegNxState: out std_logic_vector(1 downto 0)
27          );
28      end component;
29
30      signal RegSelA, RegWrA, RegWrB: std_logic;
31      signal RegALUop: std_logic_vector(1 downto 0);
32
33      component blocoOperacional is
34          port
35          (
36              InpA,InpB: in unsigned(3 downto 0);
37              selA: in std_logic;
38              wrA,wrB: in std_logic;
39              ALUop: in std_logic_vector(1 downto 0);
40              reset: in std_logic;
41
42              ALUout: buffer unsigned(4 downto 0)
43          );
44      end component;
45
46      component Mod8Counter is
47          port
48          (
49              CLK,reset: in std_logic;
50              dv: out std_logic
51          );
52      end component;
53      signal dv: std_logic;
54
55  begin
56
57      FSM01: StateMachine_ControlUnit port map(clock, reset, dv, RegSelA, RegWrA, RegWrB,
58      RegALUop, RegPrState, RegNxState);
59      blocoOp: blocoOperacional port map(InpA, InpB, RegSelA, RegWrA, RegWrB, RegALUop,
60      reset, ALUout);
61      m8c: Mod8Counter port map(clock, reset, dv);
62  end architecture;
```