```
module keypadEncoder (
              input wire clk, reset,
input wire[2:0] Col,
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              output wire[3:0] Row,
output reg[3:0] d,
              output reg dav
        );
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              wire Freeze;
              wire[1:0] RowOut, ColOut;
wire[3:0] dataConverted;
              RingCounter inst01 (clk, reset, Freeze, Row);
RowEncoder inst02 (Row, RowOut);
ColEncoder inst03 (Col, ColOut);
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              RowColEncoder inst04 (RowOut, ColOut, dataConverted);
              assign Freeze = \sim(Col[0] & Col[1] & Col[2]);
              always @(posedge clk or posedge reset) begin
                    if(reset) begin
d = 4'b0000;
                           dav = 1'b0;
                    end
                    else begin
                           d = dataConverted;
                           dav = Freeze;
                    end
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32
              end
        endmodule
```

Date: August 23, 2024 Project: pratica05

