```
1   module RamMemory (
2       input clk,
3       input write_enable,
4       input [9:0]address,
5       input [3:0]data_in,
6       output reg [3:0]data_out
7   );
8
9
10  reg [3:0] RamBlock [0:15];
11
12  always @(posedge clk) begin
13      if(write_enable)
14          RamBlock[address] <= data_in;
15      else
16          data_out <= RamBlock[address];
17  end
18
19  endmodule
```