```
1   module ControleVGA (
2       input wire clk50,
3       input wire[8:0] CircleRow,
4       input wire[9:0] CircleCol,
5
6       output wire clk25, Hsync, Vsync,
7       output wire syncVGA,blankVGA,
8       output wire[7:0] R,G,B
9   );
10
11  assign syncVGA = 1'b0;
12  assign blankVGA = 1'b1;
13
14  wire Hactive, Vactive, enable;
15  GeradorControle gC(clk50, clk25, Hsync, Hactive, Vsync, Vactive, enable);
16  GeradorImagem gI(clk25, Hsync, Hactive, Vsync, Vactive, enable, CircleRow, CircleCol, R,
    G, B);
17
18  endmodule
```