```
1   module ContadorLinha (
2       input wire Hsync, Vsync, Vactive,
3       output reg[8:0] row
4   );
5
6       always @(posedge Hsync ) begin
7           if (Vsync == 1'b0) row <= 9'd0;
8           else if (Vactive == 1'b1) row <= row + 9'd1;
9       end
10
11  endmodule
```