

```
1  module clockDivider #(
2      parameter INPUT_FREQ = 50000000,
3      parameter OUTPUT_FREQ = 1
4  )(
5      input wire clk_in,
6      input wire reset,
7      output reg clk_out
8  );
9
10     localparam integer halfPeriod = INPUT_FREQ / (2 * OUTPUT_FREQ);
11
12     integer counter;
13
14     always @(posedge clk_in or posedge reset) begin
15         if (reset) begin
16             counter <= 0;
17             clk_out <= 0;
18         end else begin
19             counter <= counter + 1;
20             if (counter >= halfPeriod) begin
21                 clk_out <= ~clk_out;
22                 counter <= 0;
23             end
24         end
25     end
26 endmodule
27
```