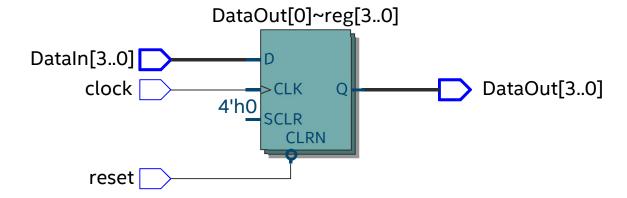
Date: June 13, 2024 Project: atv02



```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;
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        entity registrador is
              port (
                    DataIn: in unsigned(3 downto 0);
clock, reset: in std_logic;
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                    DataOut: out unsigned(3 downto 0)
        );
end entity;
        architecture behavior of registrador is
        begin
              process(clock, reset)
              begin
                    if(reset = '0') then
    DataOut <= "0000";</pre>
                    elsif rising_Edge(clock) then
                           DataOut <= DataIn;</pre>
                    end if;
              end process;
        end architecture;
```

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