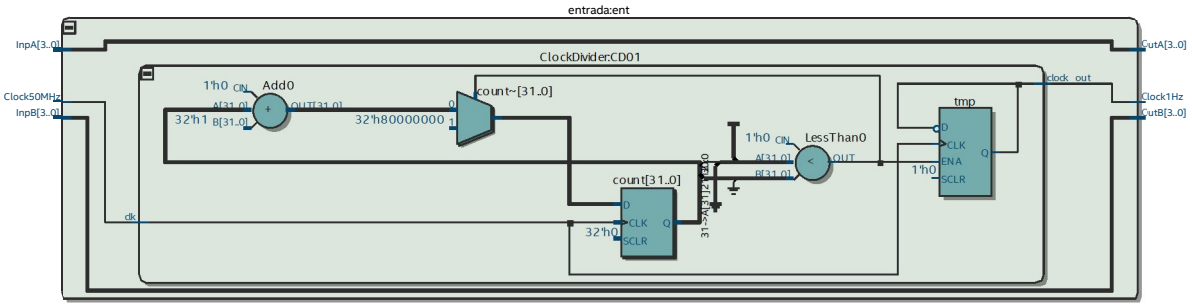
entrada:ent
InpA[3..0]
ClockDivider:CD01
OutA[3..0]
Clock50MHz
InpB[3..0]
clock_out
Clock1Hz
OutB[3..0]
1'h0 CIN
Add0
A[31..0]
32'h1 B[31..0]
OUTT[31..0]
count~[31..0]
0
32'h80000000 1
1'h0 CIN
LessThan0
A[31..0]
B[31..0]
OUT
tmp
D
CLK
ENA
SCLR
Q
1'h0
count[31..0]
D
CLK
SCLR
Q
32'h0
31~32
clk

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.numeric_std.ALL;

entity ClockDivider is
   port ( clk: in std_logic;
      clock_out: out std_logic);
end entity;

architecture behavior of ClockDivider is

   signal count: integer:=1;
   signal tmp : std_logic := '0';

    signal oscillator: integer := 50000000;
    signal newfrequency: integer := 1;


begin

   process(clk)

      variable halfPeriod: integer := (oscillator)/(newfrequency*2);

   begin


      if(clk'event and clk='1') then
         count <=count+1;
         if (count > halfPeriod) then -- usar 2500000 na FPGA
            tmp <= NOT tmp;
            count <= 1;
         end if;
      end if;
      clock_out <= tmp;
   end process;

end architecture;
```