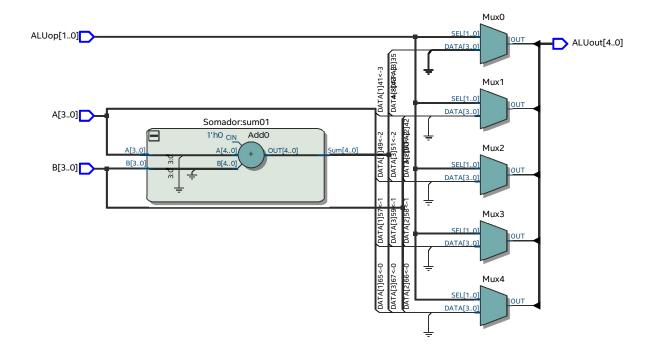
Date: June 13, 2024 Project: atv02



```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;
 1
 2
5
6
7
8
9
      entity ULA is
           port (
                A,B: in unsigned(3 downto 0);
ALUop: in std_logic_vector(1 downto 0);
ALUout: out unsigned (4 downto 0)
      );
end entity;
      architecture behavior of ULA is
      component Somador is
           port (
                A,B: in unsigned(3 downto 0);
                Sum: out unsigned (4 downto 0)
      end component;
      signal Sum: unsigned(4 downto 0);
      begin
           sum01: Somador port map(A,B,Sum);
           when "00",
A) when "01",
B) when "10",
when "11";
                Sum
37
38
      end architecture;
```