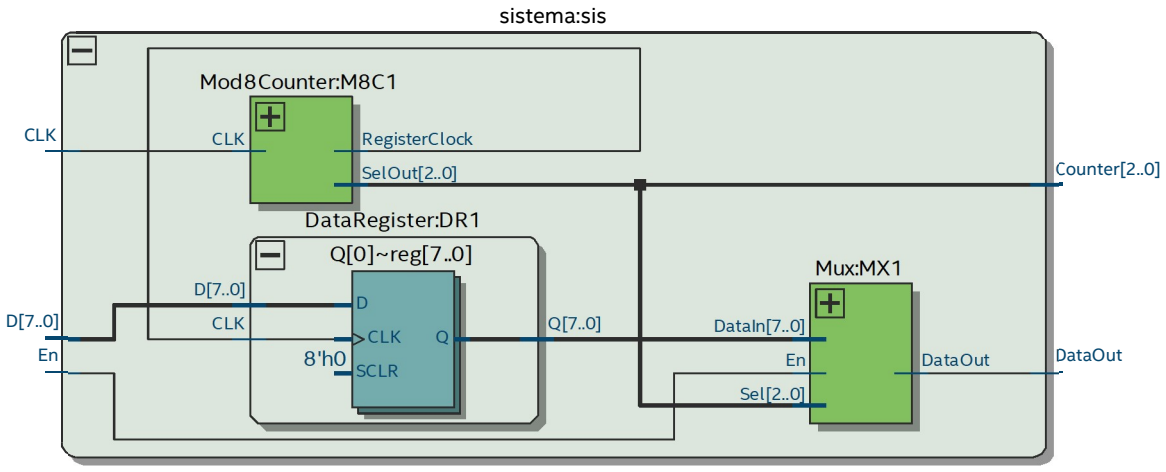
sistema:sis
Mod8Counter:M8C1
CLK
CLK
RegisterClock
SelOut[2..0]
Counter[2..0]
DataRegister:DR1
Q[0]~reg[7..0]
D[7..0]
D[7..0]
CLK
D
CLK
Q
Q[7..0]
En
8'h0
SCLR
Mux:MX1
DataIn[7..0]
En
DataOut
DataOut
Sel[2..0]

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity DataRegister is
    Port(
        CLK: in std_logic;
        D: in std_logic_vector(7 downto 0);
        Q: out std_logic_vector(7 downto 0)
    );
end entity;

architecture behavior of DataRegister is

begin

    Process(CLK)
    begin
        if(CLK'event and CLK='1') then
            Q <= D;
        end if;

    end Process;

end architecture;

```

Simulation Waveform Editor - C:/Users/welly/Documents/GitHub/LT39A/pratica00/Quartus/atv00 - atv00 - [atv00_20240411205125.sim.vwf (Read-Only)]

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Master Time Bar: 0 ps Pointer: 990.31 ns Interval: 990.31 ns Start: End:

Name	Value at 0 ps
CLK	B 0
D	B 00000000
Q	B 00000000

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

D: 00000000 | 00000001 | 00000010 | 00000011 | 00000100 | 00000101 | 00000110 | 00000111 | 00001000 | 00001001

Q: 00000000 | 00000001 | 00000100 | 00000111