```
1   module Divisor (output[3:0]Q,R, input[3:0]A,B);
2
3      wire [3:0]SubOut1;
4      wire BOut1;
5      wire [2:0]Mout1;
6
7      Subtractor s1(SubOut1,BOut1,{3'b000,A[3]},B,1'b0);
8      assign Q[3] = ~BOut1;
9      Multiplexer m1(Mout1,SubOut1[2:0],{2'b00,A[3]},BOut1);
10
11     wire [3:0]SubOut2;
12     wire BOut2;
13     wire [2:0]Mout2;
14
15     Subtractor s2(SubOut2,BOut2,{Mout1,A[2]},B,1'b0);
16     assign Q[2] = ~BOut2;
17     Multiplexer m2(Mout2,SubOut2[2:0],{Mout1[1:0],A[2]},BOut2);
18
19     wire [3:0]SubOut3;
20     wire BOut3;
21     wire [2:0]Mout3;
22
23     Subtractor s3(SubOut3,BOut3,{Mout2,A[1]},B,1'b0);
24     assign Q[1] = ~BOut3;
25     Multiplexer m3(Mout3,SubOut3[2:0],{Mout2[1:0],A[1]},BOut3);
26
27     wire [3:0]SubOut4;
28     wire BOut4;
29
30     Subtractor s4(SubOut4,BOut4,{Mout3,A[0]},B,1'b0);
31     assign Q[0] = ~BOut4;
32     Multiplexer4x m4(R,SubOut4,{Mout3,A[0]},BOut4);
33
34
35  endmodule
```