

```
1  module muxIn (  
2      input wire [3:0] zero, one,  
3      input wire sel,  
4      output reg [3:0] s  
5  );  
6      always @(sel) begin  
7          if(sel) begin  
8              s = one;  
9          end else begin  
10             s = zero;  
11         end  
12     end  
13 endmodule
```