```
1   module arquitetura (
2       input wire clock, reset,
3       input wire[3:0] AddressIn,
4
5       input wire[2:0] col,
6       output wire[3:0] row,
7
8       output wire RS,RW,
9       output wire E,
10      output wire[7:0] DB,
11      output wire LCD_Blon, LCD_On
12  );
13
14      wire clock50MHz, clock500Hz, clock1Hz, dav;
15      wire[3:0] AddressOut, KeypadData;
16      Entrada inst00 (clock, reset, clock50MHz, clock500Hz, clock1Hz, AddressIn, AddressOut
    , col, row, KeypadData, dav);
17
18      wire[3:0] DataOut;
19      wire[1:0] PresentStateFlag;
20      Sistema inst01(clock50MHz, clock1Hz, reset, dav, KeypadData, AddressOut, DataOut,
    PresentStateFlag);
21
22      Saida inst03(clock50MHz, clock500Hz, reset, AddressOut, DataOut, KeypadData,
    PresentStateFlag, RS, RW, E, DB, LCD_Blon, LCD_On);
23  endmodule
```