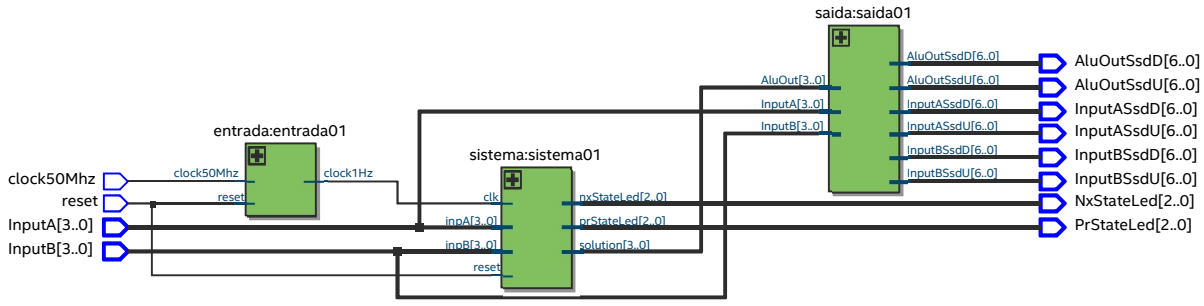
```
1   module Arquitetura (
2       input wire[3:0]InputA, InputB,
3       input wire clock50Mhz, reset,
4
5       output wire[2:0] PrStateLed,NxStateLed,
6       output wire[6:0] InputASsdU,InputASsdD,
7       output wire[6:0] InputBSsdU,InputBSsdD,
8       output wire[6:0] AluOutSsdU,AluOutSsdD
9   );
10
11  wire clock1Hz;
12  entrada entrada01(clock50Mhz, reset, clock1Hz);
13
14  wire[3:0] AluOut;
15  sistema sistema01(clock1Hz, reset, InputA, InputB, AluOut, PrStateLed, NxStateLed);
16
17  saida saida01(InputA, InputB, AluOut, InputASsdU, InputASsdD, InputBSsdU, InputBSsdD,
    AluOutSsdU, AluOutSsdD);
18
19  endmodule
```


saida:saida01
AluOutSsdD[6..0]
AluOutSsdU[6..0]
InputASsdD[6..0]
InputASsdU[6..0]
InputBSsdD[6..0]
InputBSsdU[6..0]
NxStateLed[2..0]
PrStateLed[2..0]
AluOut[3..0]
InputA[3..0]
InputB[3..0]
entrada:entrada01
clock50Mhz
reset
clock1Hz
sistema:sistema01
clk
inpA[3..0]
inpB[3..0]
reset
nxStateLed[2..0]
prStateLed[2..0]
solution[3..0]
clock50Mhz
reset
InputA[3..0]
InputB[3..0]

Entity:Instance	Logic Cells	:d Logic F	I/O Registers	Memory Bits	M9Ks	DSP Elements	DSP 9x9	DSP 18x18	Pins	Virtual Pins	LUT-Only LCs	Register-Only LCs	LUT/Register LCs	Full Hierarchy Name
Cyclone IV E: EP4CE115F29C7														
Arquitetura	160 (0)	50 (0)	0 (0)	0	0	0	0	0	58	0	110 (0)	6 (0)	44 (0)	|Arquitetura
entrada:entrada01	47 (0)	33 (0)	0 (0)	0	0	0	0	0	0	0	14 (0)	5 (0)	28 (0)	|Arquitetura|entrada...
saida:saida01	54 (0)	0 (0)	0 (0)	0	0	0	0	0	0	0	51 (0)	0 (0)	3 (0)	|Arquitetura|saida:s...
sistema:sistema01	62 (0)	17 (0)	0 (0)	0	0	0	0	0	0	0	45 (0)	1 (0)	16 (0)	|Arquitetura|sistem...