



```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  USE ieee.numeric_std.all;
4
5  entity registrador is
6      port
7      (
8          DataIn: in unsigned(3 downto 0);
9          clock, reset: in std_logic;
10
11          DataOut: out unsigned(3 downto 0)
12      );
13  end entity;
14
15  architecture behavior of registrador is
16
17  begin
18
19      process(clock, reset)
20      begin
21          if(reset = '0') then
22              DataOut <= "0000";
23          elsif rising_edge(clock) then
24              DataOut <= DataIn;
25          end if;
26      end process;
27
28
29  end architecture;
```