```verilog
1    module GeradorHorizontal (
2        input wire clk25,
3        output reg Hsync, Hactive
4    );
5
6        localparam  Hp = 96, Hbp = 48,
7                    Hact = 640, Hfp = 16;
8
9        reg[9:0] count;
10
11       always @(posedge clk25) begin
12           count <= count + 10'd1;
13           if (count == Hp) Hsync <= 1'b1;
14           else if(count == Hp+Hbp) Hactive <= 1'b1;
15           else if(count == Hp+Hbp+Hact) Hactive <= 1'b0;
16           else if(count == Hp+Hbp+Hact+Hfp) begin
17               Hsync <= 1'b0;
18               count <= 10'd0;
19           end
20       end
21
22   endmodule
```