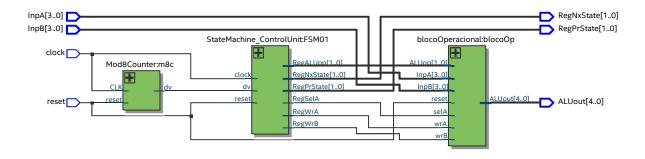
Date: June 13, 2024 Project: atv02



```
LIBRARY ieee;
USE ieee.std_logic_1164_all;
 1
     USE ieee.numeric_std.all;
     entity Sistema is
 6
          port
 7
8
              clock,reset: in std_logic;
              InpA,InpB: in unsigned(3 downto 0);
10
11
              ALUout: buffer unsigned (4 downto 0);
12
13
              RegPrState,RegNxState: out std_logic_vector(1 downto 0)
14
     end entity;
15
16
17
     architecture behavior of Sistema is
18
          component StateMachine_ControlUnit is
port
              (
                   clock,reset: in std_logic;
                   dv: in std_logic;
                  RegSelA, RegWrA, RegWrB: out std_logic;
RegALUop: out std_logic_vector(1 downto 0);
                   RegPrState RegNxState: out std_logic_vector(1 downto 0)
          end component;
          signal RegSelA, RegWrA, RegWrB: std_logic;
         signal RegALUop: std_logic_vector(1 downto 0);
          component blocoOperacional is
              port
                   InpA,InpB: in unsigned(3 downto 0);
                  selA: in std_logic;
                  wrA,wrB: in std_logic;
                  ALUop: in std_logic_vector(1 downto 0); reset: in std_logic;
                  ALUout: buffer unsigned (4 downto 0)
          end component;
          component Mod8Counter is
              port
                   CLK,reset: in std_logic;
                   dv: out std_logic
          end component;
          signal dv: std_logic;
     begin
          FSM01: StateMachine_ControlUnit port map(clock, reset, dv, RegSelA, RegWrA, RegWrB,
     RegALUop, RegPrState, RegNxState);
58
          blocoOp: blocoOperacional port map(InpA, InpB, RegSelA, RegWrA, RegWrB, RegALUop,
     reset, ALUout);
59
         m8c: Mod8Counter port map(clock, reset, dv);
60
61
     end architecture;
```

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