```
1   module Arquitetura(  input [3:0]A,B,
2                        input Enable,Strobe,
3                        output [6:0]ssdQD,ssdQU,ssdRD,ssdRU,ssdAD,ssdAU,ssdBD,ssdBU,
4                        output [3:0]Asig,Bsig,Qsig,Rsig);
5
6      wire [3:0]Ao,Bo;
7      wire [3:0]Q,R;
8
9      Entrada ent1(A,B,Enable,Ao,Bo);
10     Divisor div1(Q,R,Ao,Bo);
11     Saida   sai1(Q,R,Ao,Bo,Strobe,ssdQD,ssdQU,ssdRD,ssdRU,ssdAD,ssdAU,ssdBD,ssdBU);
12
13     assign Asig = Ao;
14     assign Bsig = Bo;
15     assign Qsig = Q;
16     assign Rsig = R;
17
18  endmodule
```