```
1   module registrador (
2       input wire clk,
3       input wire reset,
4       input wire Wr,
5       input wire [3:0] din,
6       output reg [3:0] dout
7   );
8
9       always @(posedge clk or posedge reset) begin
10          if (reset) begin
11              dout <= 4'b0000;
12          end else begin
13              if (Wr) begin
14                  dout <= din;
15              end
16          end
17      end
18
19  endmodule
```