```
1   module GeradorVertical (
2       input wire Hsync,
3       output reg Vsync, Vactive
4   );
5
6       localparam  Vp = 2, Vbp = 31,
7                   Vact = 480, Vfp = 11;
8
9       reg[9:0] count;
10
11      always @(posedge Hsync) begin
12          count <= count + 10'd1;
13          if (count == Vp) Vsync <= 1'b1;
14          else if(count == Vp+Vbp) Vactive <= 1'b1;
15          else if(count == Vp+Vbp+Vact) Vactive <= 1'b0;
16          else if(count == Vp+Vbp+Vact+Vfp) begin
17              Vsync <= 1'b0;
18              count <= 10'd0;
19          end
20      end
21
22  endmodule
```