

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  USE ieee.numeric_std.all;
4
5  entity arquitetura is
6      port
7      (
8          Clock50MHz, reset: in std_logic;
9          InpA, InpB: in unsigned(3 downto 0);
10
11          InpA_ssU, InpA_ssD: out std_logic_vector(6 downto 0);
12          InpB_ssU, InpB_ssD: out std_logic_vector(6 downto 0);
13          ALUOut_ssU, ALUOut_ssD: out std_logic_vector(6 downto 0);
14
15          RegPrState, RegNxState: out std_logic_vector(1 downto 0)
16      );
17 end entity;
18
19 architecture behavior of arquitetura is
20
21     component entrada is
22     port
23     (
24         Clock50MHz: in std_logic;
25         InpA, InpB: in unsigned(3 downto 0);
26
27         OutA, OutB: out unsigned(3 downto 0);
28         Clock1Hz: out std_logic
29     );
30 end component;
31
32     signal OutA, OutB: unsigned(3 downto 0);
33     signal Clock1Hz: std_logic;
34
35     component Sistema is
36     port
37     (
38         clock, reset: in std_logic;
39         InpA, InpB: in unsigned(3 downto 0);
40
41         ALUout: buffer unsigned(4 downto 0);
42         RegPrState, RegNxState: out std_logic_vector(1 downto 0)
43     );
44 end component;
45
46     signal ALUout: unsigned(4 downto 0);
47
48     component saida is
49     port
50     (
51         InpA, InpB: in unsigned(3 downto 0);
52         ALUOut: in unsigned(4 downto 0);
53
54         InpA_ssU, InpA_ssD: out std_logic_vector(6 downto 0);
55         InpB_ssU, InpB_ssD: out std_logic_vector(6 downto 0);
56         ALUOut_ssU, ALUOut_ssD: out std_logic_vector(6 downto 0)
57     );
58 end component;
59
60 begin
61
62     ent: entrada port map(Clock50MHz, InpA, InpB, OutA, OutB, Clock1Hz);
63     sis: Sistema port map(Clock1Hz, reset, OutA, OutB, ALUout, RegPrState, RegNxState);
64     sai: saida port map(InpA, InpB, ALUout, InpA_ssU, InpA_ssD, InpB_ssU, InpB_ssD, ALUOut_ssU
65 , ALUOut_ssD);
66
67 end architecture;
```