

```
1  library ieee;
2  use ieee.numeric_std.all;
3  use IEEE.STD_LOGIC_1164.ALL;
4  use IEEE.STD_LOGIC_ARITH.ALL;
5  use IEEE.STD_LOGIC_UNSIGNED.ALL;
6
7  entity sistema is
8  port
9  (
10     CLK: in std_logic;
11     D: in std_logic_vector(7 downto 0);
12     En: in std_logic;
13
14     DataOut: out std_logic;
15     Counter: out std_logic_vector(2 downto 0)
16 );
17 end entity;
18
19 architecture behavior of sistema is
20
21     component DataRegister is
22     port(
23         CLK: in std_logic;
24         D: in std_logic_vector(7 downto 0);
25         Q: out std_logic_vector(7 downto 0)
26     );
27 end component;
28 signal Q: std_logic_vector(7 downto 0);
29
30 component Mux is
31 port(
32     DataIn: in std_logic_vector(7 downto 0);
33     Sel: in std_logic_vector(2 downto 0);
34     En: in std_logic;
35     DataOut: out std_logic
36 );
37 end component;
38
39 component Mod8Counter is
40 port
41 (
42     CLK: in std_logic;
43     RegisterClock: out std_logic;
44     SelOut: out std_logic_vector(2 downto 0)
45 );
46 end component;
47 signal RegisterClock: std_logic;
48 signal SelOut: std_logic_vector(2 downto 0);
49
50 begin
51
52     DR1: DataRegister port map(RegisterClock,D,Q);
53     MX1: Mux port map(Q,SelOut,En,DataOut);
54     M8C1: Mod8Counter port map(CLK,RegisterClock,SelOut);
55
56     Counter <= SelOut;
57
58 end architecture;
59
```