```
1   module ContadorColuna (
2       input wire Hsync, clk25, Hactive,
3       output reg[9:0] col
4   );
5
6       always @(posedge clk25 ) begin
7           if (Hsync == 1'b0) col <= 10'd0;
8           else if (Hactive == 1'b1) col <= col + 10'd1;
9       end
10
11  endmodule
```