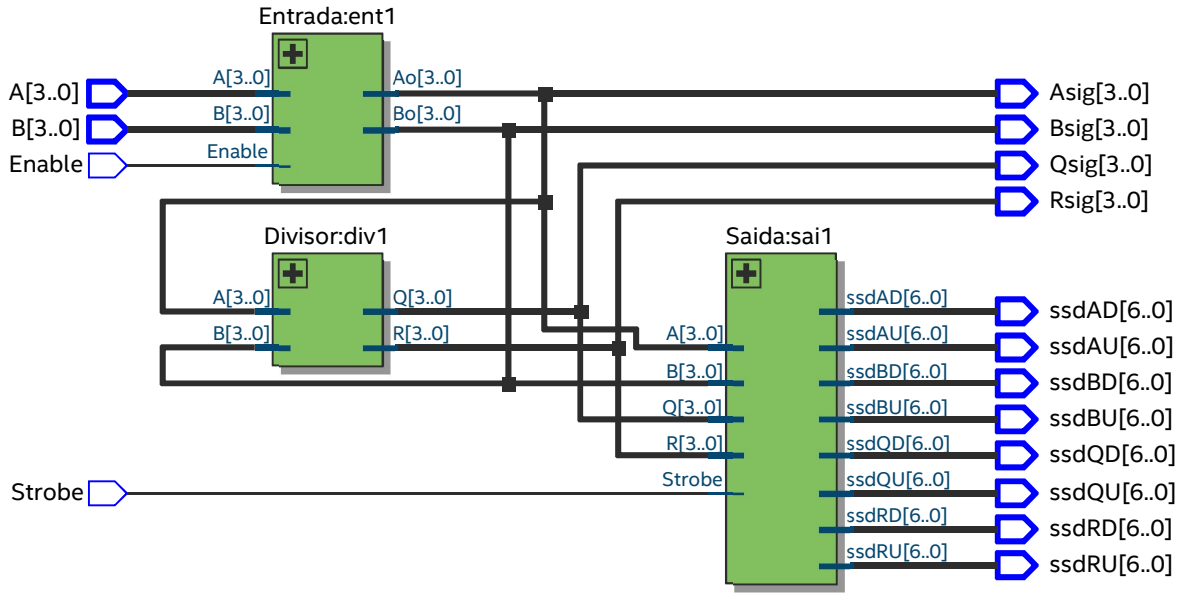

Entrada:ent1
A[3..0]
B[3..0]
Enable
Ao[3..0]
Bo[3..0]
Divisor:div1
Q[3..0]
R[3..0]
Saida:sai1
Strobe
ssdAD[6..0]
ssdAU[6..0]
ssdBD[6..0]
ssdBU[6..0]
ssdQD[6..0]
ssdQU[6..0]
ssdRD[6..0]
ssdRU[6..0]
Asig[3..0]
Bsig[3..0]
Qsig[3..0]
Rsig[3..0]

Project Navigator

Hierarchy

Entity:Instance	Logic Cells	ed Logic R	I/O Registers	Memory Bits	M9Ks	DSP Elements	DSP 9x9	DSP 18x18	Pins	Virtual Pins	LUT-Only LCs	Register-Only LCs	LUT/Register LCs	Full Hierarchy Name
Cyclone IV E: EP4CE115F29C7														
Arquitetura	115 (0)	0 (0)	0 (0)	0	0	0	0	0	82	0	115 (0)	0 (0)	0 (0)	|Arquitetura
Divisor:div1	33 (0)	0 (0)	0 (0)	0	0	0	0	0	0	0	33 (0)	0 (0)	0 (0)	|Arquitetura|Divisor:div1
Entrada:ent1	8 (8)	0 (0)	0 (0)	0	0	0	0	0	0	0	8 (8)	0 (0)	0 (0)	|Arquitetura|Entrada:ent1
Saida:sai1	74 (0)	0 (0)	0 (0)	0	0	0	0	0	0	0	74 (0)	0 (0)	0 (0)	|Arquitetura|Saida:sai1

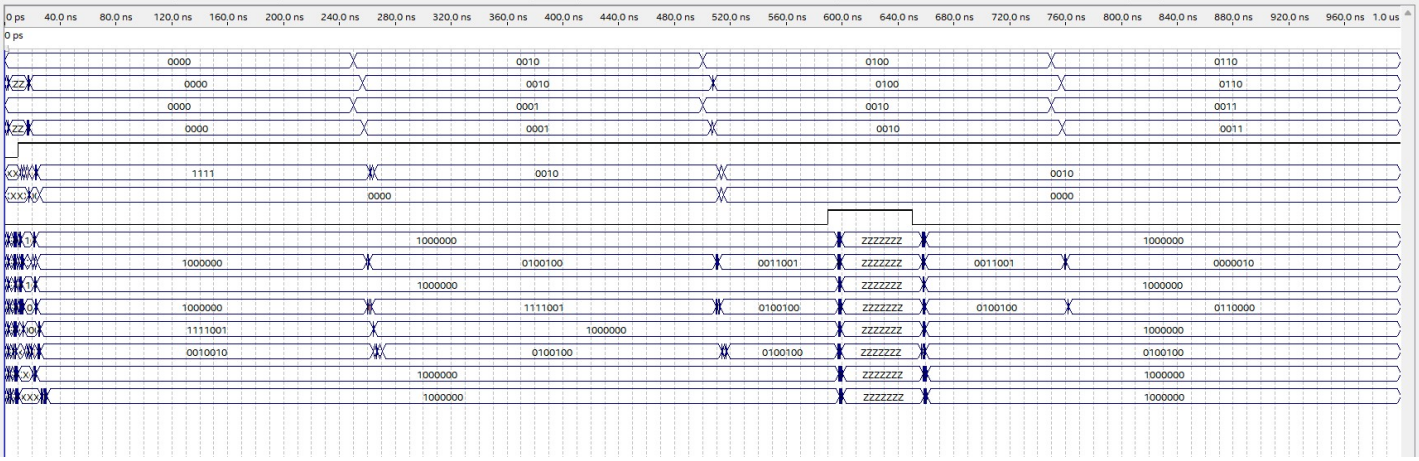
Simulation Waveform Editor - C:/Users/welly/Documents/GitHub/LT39A/pratica03/atv03 - atv03 - [atv03_20240613175840.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: 327.93 ns Interval: 327.93 ns Start: End:

Name	Value at 0 ps
A	B 0000
Asig	B XXXX
B	B 0000
Bsig	B XXXX
Enable	B 0
Qsig	B XXXX
Rsig	B XXXX
Strobe	B 0
ssdAD	B XXXXZZX
ssdAU	B XXXXXXX
ssdBD	B XXXXZZX
ssdBU	B XXXXXXX
ssdQD	B XXXXZZX
ssdQU	B XXXXXXX
ssdRD	B XXXXZZX
ssdRU	B XXXXXXX



```
1   module Arquitetura(  input [3:0]A,B,
2                        input Enable,Strobe,
3                        output [6:0]ssdQD,ssdQU,ssdRD,ssdRU,ssdAD,ssdAU,ssdBD,ssdBU,
4                        output [3:0]Asig,Bsig,Qsig,Rsig);
5
6      wire [3:0]Ao,Bo;
7      wire [3:0]Q,R;
8
9      Entrada ent1(A,B,Enable,Ao,Bo);
10     Divisor div1(Q,R,Ao,Bo);
11     Saida   sai1(Q,R,Ao,Bo,Strobe,ssdQD,ssdQU,ssdRD,ssdRU,ssdAD,ssdAU,ssdBD,ssdBU);
12
13     assign Asig = Ao;
14     assign Bsig = Bo;
15     assign Qsig = Q;
16     assign Rsig = R;
17
18  endmodule
```