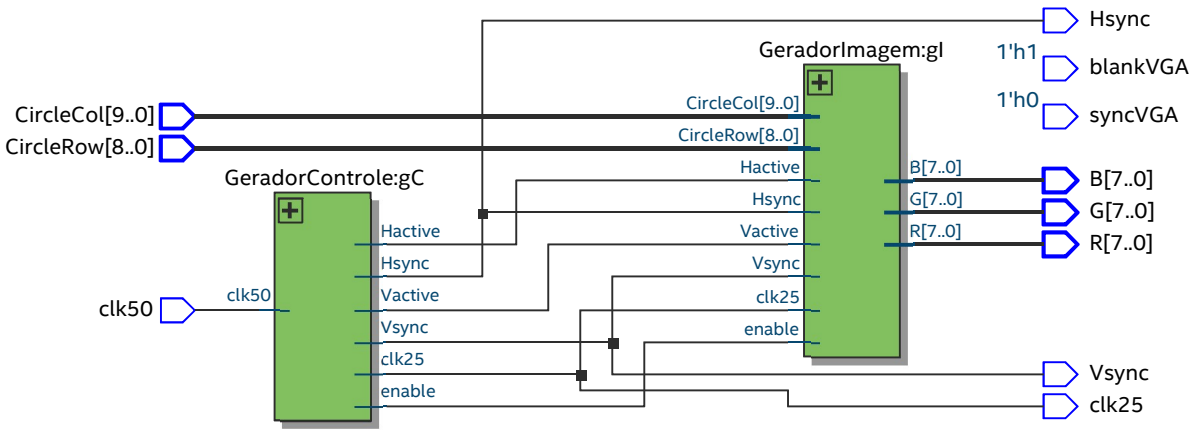
```
1   module ControleVGA (
2       input wire clk50,
3       input wire[8:0] CircleRow,
4       input wire[9:0] CircleCol,
5
6       output wire clk25, Hsync, Vsync,
7       output wire syncVGA,blankVGA,
8       output wire[7:0] R,G,B
9   );
10
11  assign syncVGA = 1'b0;
12  assign blankVGA = 1'b1;
13
14  wire Hactive, Vactive, enable;
15  GeradorControle gC(clk50, clk25, Hsync, Hactive, Vsync, Vactive, enable);
16  GeradorImagem gI(clk25, Hsync, Hactive, Vsync, Vactive, enable, CircleRow, CircleCol, R,
    G, B);
17
18  endmodule
```


Hsync
1'h1
blankVGA
1'h0
syncVGA
GeradorImagem:gl
CircleCol[9..0]
CircleRow[8..0]
Hactive
Hsync
Vactive
Vsync
clk25
enable
B[7..0]
G[7..0]
R[7..0]
CircleCol[9..0]
CircleRow[8..0]
GeradorControle:gC
clk50
Hactive
Hsync
Vactive
Vsync
clk25
enable
clk50
B[7..0]
G[7..0]
R[7..0]
Vsync
clk25

Simulation Waveform Editor - C:/Users/welly/Documents/GitHub/LT39A/pratica07/atv07 - atv07 - [atv07_20240907164916.sim.vwf (Read-Only)]

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Master Time Bar: 0 ps Pointer: 356.99 ns Interval: 356.99 ns Start: End:

Name	Value at 0 ps
B	U 0
CircleCol	U 125
CircleRow	U 175
G	U 0
Hsync	U 0
R	U 0
Vsync	U 0
blankVGA	U 1
clk25	U 0
clk50	U 0
syncVGA	U 0