```
1   module Arquitetura (
2       input wire[3:0]InputA, InputB,
3       input wire clock50Mhz, reset,
4
5       output wire[2:0] PrStateLed,NxStateLed,
6       output wire[6:0] InputASsdU,InputASsdD,
7       output wire[6:0] InputBSsdU,InputBSsdD,
8       output wire[6:0] AluOutSsdU,AluOutSsdD
9   );
10
11  wire clock1Hz;
12  entrada entrada01(clock50Mhz, reset, clock1Hz);
13
14  wire[3:0] AluOut;
15  sistema sistema01(clock1Hz, reset, InputA, InputB, AluOut, PrStateLed, NxStateLed);
16
17  saida saida01(InputA, InputB, AluOut, InputASsdU, InputASsdD, InputBSsdU, InputBSsdD,
    AluOutSsdU, AluOutSsdD);
18
19  endmodule
```