Quartus Prime Lite Edition - C:/Users/welly/Documents/GitHub/LT39A/pratica02/atv02 - atv02

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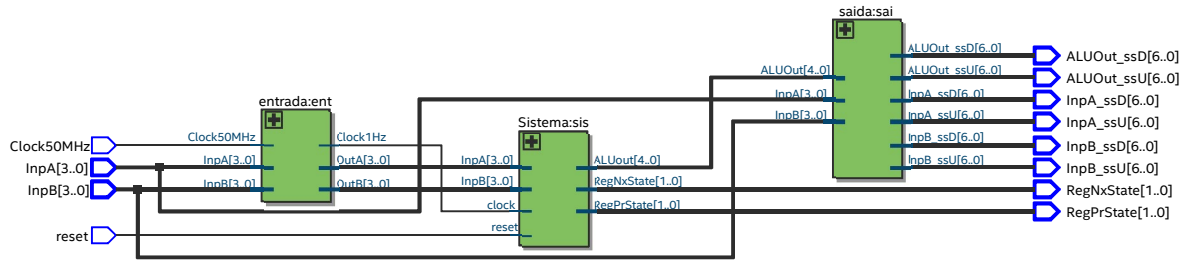
atv02

Project Navigator

Hierarchy

Entity:Instance	Logic Cells	ed Logic R	I/O Registers	Memory Bits	M9Ks	DSP Elements	DSP 9x9	DSP 18x18	Pins	Virtual Pins	LUT-Only LCs	Register-Only LCs	LUT/Register LCs	Full Hierarchy Name
Cyclone IV E: EP4CE115F29C7														
arquitetura	189 (0)	54 (0)	0 (0)	0	0	0	0	0	56	0	135 (0)	8 (0)	46 (0)	|arquitetura
entrada:ent	76 (0)	33 (0)	0 (0)	0	0	0	0	0	0	0	43 (0)	0 (0)	33 (0)	|arquitetura|entrada...
ClockDivider:CD01	76 (76)	33 (33)	0 (0)	0	0	0	0	0	0	0	43 (43)	0 (0)	33 (33)	|arquitetura|entrada...
saida:sai	86 (0)	0 (0)	0 (0)	0	0	0	0	0	0	0	85 (0)	0 (0)	1 (0)	|arquitetura|saida:sai
SevenSegmentsDecoder_4bitsToDec:outA	20 (15)	0 (0)	0 (0)	0	0	0	0	0	0	0	20 (15)	0 (0)	0 (0)	|arquitetura|saida:s...
SevenSegmentsDecoder_5bitsToDec:outALU	46 (29)	0 (0)	0 (0)	0	0	0	0	0	0	0	45 (28)	0 (0)	1 (1)	|arquitetura|saida:s...
SevenSegmentsDecoder_4bitsToDec:outB	20 (15)	0 (0)	0 (0)	0	0	0	0	0	0	0	20 (15)	0 (0)	0 (0)	|arquitetura|saida:s...
Sistema:sis	28 (0)	21 (0)	0 (0)	0	0	0	0	0	0	0	7 (0)	8 (0)	13 (0)	|arquitetura|Sistem...
blocoOperacional:blocoOp	14 (0)	8 (0)	0 (0)	0	0	0	0	0	0	0	6 (0)	4 (0)	4 (0)	|arquitetura|Sistem...
StateMachine_ControlUnit:FSM01	11 (11)	10 (10)	0 (0)	0	0	0	0	0	0	0	1 (1)	4 (4)	6 (6)	|arquitetura|Sistem...
Mod8Counter:m8c	3 (3)	3 (3)	0 (0)	0	0	0	0	0	0	0	0 (0)	0 (0)	3 (3)	|arquitetura|Sistem...


saida:sai
entrada:ent
Sistema:sis
Clock50MHz
InpA[3..0]
InpB[3..0]
reset
Clock50MHz
InpA[3..0]
InpB[3..0]
Clock1Hz
OutA[3..0]
OutB[3..0]
InpA[3..0]
InpB[3..0]
clock
reset
ALUout[4..0]
RegNxState[1..0]
RegPrState[1..0]
ALUOut[4..0]
InpA[3..0]
InpB[3..0]
ALUOut_ssD[6..0]
ALUOut_ssU[6..0]
InpA_ssD[6..0]
InpA_ssU[6..0]
InpB_ssD[6..0]
InpB_ssU[6..0]
ALUOut_ssD[6..0]
ALUOut_ssU[6..0]
InpA_ssD[6..0]
InpA_ssU[6..0]
InpB_ssD[6..0]
InpB_ssU[6..0]
RegNxState[1..0]
RegPrState[1..0]

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;

entity arquitetura is
    port
    (
        Clock50MHz, reset: in std_logic;
        InpA,InpB: in unsigned(3 downto 0);

        InpA_ssU,InpA_ssD: out std_logic_vector(6 downto 0);
        InpB_ssU,InpB_ssD: out std_logic_vector(6 downto 0);
        ALUOut_ssU,ALUOut_ssD: out std_logic_vector(6 downto 0);

        RegPrState,RegNxState: out std_logic_vector(1 downto 0)

    );
end entity;

architecture behavior of arquitetura is

    component entrada is
        port
        (
            Clock50MHz: in std_logic;
            InpA,InpB: in unsigned(3 downto 0);

            OutA,OutB: out unsigned(3 downto 0);
            Clock1Hz: out std_logic
        );
    end component;

    signal OutA,OutB: unsigned(3 downto 0);
    signal Clock1Hz: std_logic;

    component Sistema is
        port
        (
            clock,reset: in std_logic;
            InpA,InpB: in unsigned(3 downto 0);

            ALUout: buffer unsigned(4 downto 0);
            RegPrState,RegNxState: out std_logic_vector(1 downto 0)

        );
    end component;
    signal ALUout: unsigned(4 downto 0);


    component saida is
        port
        (
            InpA,InpB: in unsigned(3 downto 0);
            ALUOut: in unsigned(4 downto 0);

            InpA_ssU,InpA_ssD: out std_logic_vector(6 downto 0);
            InpB_ssU,InpB_ssD: out std_logic_vector(6 downto 0);
            ALUOut_ssU,ALUOut_ssD: out std_logic_vector(6 downto 0)
        );
    end component;

begin

    ent: entrada port map(Clock50MHz,InpA,InpB,OutA,OutB,Clock1Hz);
    sis: Sistema port map(Clock1Hz,reset,OutA,OutB,ALUOut,RegPrState,RegNxState);
    sai: saida   port map(InpA,InpB,ALUOut,InpA_ssU,InpA_ssD,InpB_ssU,InpB_ssD,ALUOut_ssU
,ALUOut_ssD);

end architecture;
```