```
1   module Sistema (
2       input wire clock50MHz, clock1Hz, reset,
3
4       input wire dav,
5       input wire[3:0] KeypadData,
6
7       input wire[3:0] AddressIn,
8
9       output reg[3:0] DataOut,
10
11      output wire[1:0] PresentStateFlag
12
13  );
14
15      wire WriteEnable, MemoryEnable, TimerTrigger;
16      wire[7:0] TimerRef;
17      ControlUnit inst00(clock1Hz, reset, dav, WriteEnable, MemoryEnable, TimerTrigger,
    TimerRef, PresentStateFlag);
18
19      Timer inst01(TimerRef, clock1Hz, reset, TimerTrigger);
20
21      wire MemoryClock;
22      assign MemoryClock = (MemoryEnable == 1'b1) ? clock50MHz : 1'bz;
23      wire[3:0] RamData;
24      RamMemory inst02(MemoryClock, WriteEnable, AddressIn, KeypadData, RamData);
25
26      always @(*) begin
27          case (PresentStateFlag)
28              2'd0: DataOut = DataOut;
29              2'd1: DataOut = DataOut;
30              2'd2: DataOut = RamData;
31              default: begin
32
33              end
34          endcase
35
36      end
37
38  endmodule
```