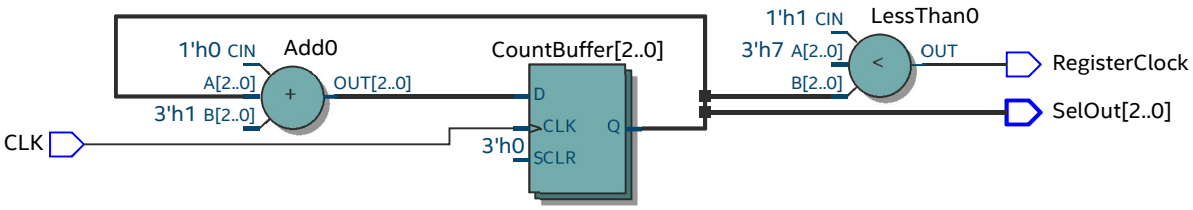
```vhdl
library ieee;
use ieee.numeric_std.all;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity Mod8Counter is
    port
    (
        CLK: in std_logic;
        RegisterClock: out std_logic;
        SelOut: out std_logic_vector(2 downto 0)
    );
end entity;

architecture behavior of Mod8Counter is

begin

    process(CLK)

    variable CountBuffer: std_logic_vector(2 downto 0);

    begin

        if(CLK'event and CLK='1') then
            CountBuffer := CountBuffer + 1;
        end if;

        if(CountBuffer >= 7) then
            RegisterClock <= '1';
        else
            RegisterClock <= '0';
        end if;

    SelOut <= CountBuffer;

    end process;

end architecture;
```


1'h0 CIN
Add0
A[2..0]
3'h1 B[2..0]
OUT[2..0]
CLK
CountBuffer[2..0]
D
CLK
Q
3'h0
SCLR
1'h1 CIN
LessThan0
3'h7 A[2..0]
B[2..0]
OUT
RegisterClock
SelOut[2..0]

Simulation Waveform Editor - C:/Users/welly/Documents/GitHub/LT39A/pratica00/Quartus/atv00 - atv00 - [atv00_20240411210437.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: 311.92 ns Interval: 311.92 ns Start: End:

Name	Value at 0 ps
CLK	B 0
Register...	B 0
SelOut	B 000

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us