Entrada:ent1

Enable

A[3..0]

OE   Ao[3..0]

DATAIN   OUT0   Ao[3..0]

OE   Bo[3..0]

B[3..0]

DATAIN   OUT0   Bo[3..0]

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Master Time Bar: 0 ps   Pointer: 199.84 ns   Interval: 199.84 ns   Start: End:

Name	Value at 0 ps
A	B 0000
Ao	B ZZZZ
B	B 0000
Bo	B ZZZZ
Enable	B 0

0 ps   40.0 ns   80.0 ns   120.0 ns   160.0 ns   200.0 ns   240.0 ns   280.0 ns   320.0 ns   360.0 ns   400.0 ns   440.0 ns   480.0 ns   520.0 ns   560.0 ns   600.0 ns   640.0 ns   680.0 ns   720.0 ns   760.0 ns   800.0 ns   840.0 ns   880.0 ns   920.0 ns   960.0 ns   1.0 us

A: 0000   0001   0010   0011   0100   0101   0110   0111
Ao: ZZZZ   0100   0101   0110   0111
B: 0000   0001   0010   0011   0100   0101   0110   0111
Bo: ZZZZ   0100   0101   0110   0111

```verilog
module Entrada (input [3:0]A,B, input Enable, output [3:0]Ao,Bo);

    assign Ao = (Enable == 1'b1) ? A : 3'bzzz;
    assign Bo = (Enable == 1'b1) ? B : 3'bzzz;

endmodule
```