```
1   module operacional (
2       input wire[3:0] inpA,inpB,
3       input wire clk, reset,
4
5       input wire selA,wrA,wrB,
6       input wire[1:0] aluOp,
7
8       output wire[3:0] result
9   );
10
11      wire[3:0] outMux;
12      muxIn mux01 (.zero(result), .one(inpA), .sel(selA), .s(outMux));
13
14      wire[3:0] outReg01, outReg02;
15      registrador reg01 (clk,reset,wrA,outMux,outReg01);
16      registrador reg02 (clk,reset,wrB,inpB,outReg02);
17
18      ALU2bits alu01 (outReg01,outReg02,aluOp,result);
19
20  endmodule
```