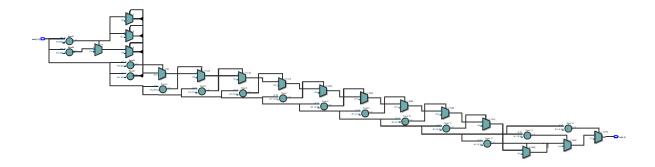
```
library ieee;
  1
           use ieee.numeric_std.all;
           use ieee.std_logic_1164.all;
  4
           entity sevenSegDecoder is
   port(
  5
 6
7
                        data: in std_logic_vector(3 downto 0);
ss: out std_logic_vector(6 downto 0)
  8
 9
10
           end entity;
11
12
13
           architecture behavior of sevenSegDecoder is
14
15
           begin
                              "1000000" when data = x"0" else "1111001" when data = x"1" else "0100100" when data = x"2" else
16
17
                 SS <=
                              "1111001"
18
                              "0110000" when data = x"3" else
"0011001" when data = x"4" else
"0010010" when data = x"4" else
19
20
21
22
23
24
25
26
27
28
29
30
31
32
                               "0000010"
                                                    when data = x''6'' else
                               "1111000" when data = x o else

"0000000" when data = x"7" else

"0011000" when data = x"8" else

"0011000" when data = x"9" else
                              "0011000" when data = x"9" else
"0001000" when data = x"a" else --invertidos
"1100000" when data = x"b" else
"0110001" when data = x"c" else
"1000010" when data = x"d" else
"0110000" when data = x"d" else
"0111000";
           end architecture;
35
```

Date: April 11, 2024 Project: atv00



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