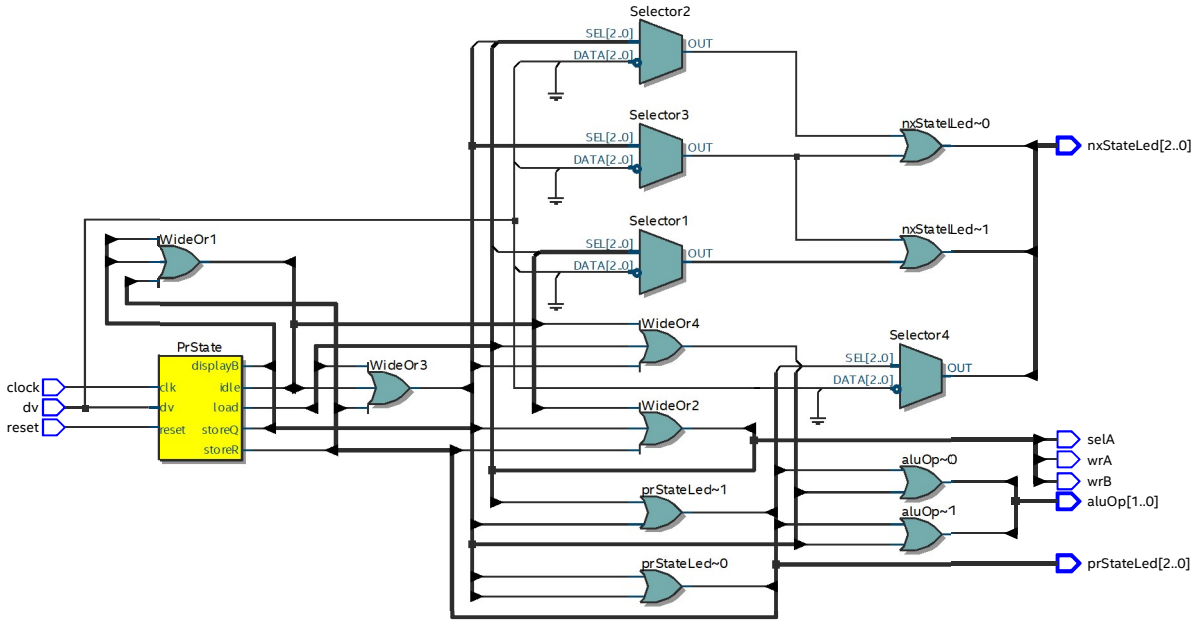
```
module controle(
    input reset,clock,dv,
    output reg selA,wrA,wrB,
    output reg [1:0]aluOp,
    output reg[2:0] prStateLed,nxStateLed
);
    //estados
    parameter    idle = 3'h0,
            load = 3'h1,
                displayB = 3'h2,
                storeQ = 3'h3,
                storeR = 3'h4;

    reg[2:0] PrState,NxState;

    //reg selA, wrA, wrB;
    //reg aluOp;

    //bloco sequencial
    always @(posedge reset or posedge clock) begin
        if(reset) begin
            PrState <= idle;
        end
        else begin
            PrState <= NxState;
        end
    end

    //bloco combinacional
    always @(*) begin
        case (PrState)
            idle: begin
                selA = 1'b0;
                wrA = 1'b0;
                wrB = 1'b0;
                aluOp = 2'b00;

                if (dv == 1) begin
                    NxState = load;
                end else begin
                    NxState = idle;
                end
            end
            load: begin
                selA = 1'b1;
                wrA = 1'b1;
                wrB = 1'b1;
                aluOp = 2'b00;

                if (dv == 1) begin
                    NxState = displayB;
                end else begin
                    NxState = load;
                end
            end
            displayB: begin
                selA = 1'b0;
                wrA = 1'b0;
                wrB = 1'b0;
                aluOp = 2'b01;

                if (dv == 1) begin
                    NxState = storeQ;
                end else begin
                    NxState = displayB;
                end
            end
            storeQ: begin
                selA = 1'b0;
                wrA = 1'b0;
                wrB = 1'b0;
                aluOp = 2'b10;

                if (dv == 1) begin
                    NxState = storeR;
                end else begin
                    NxState = storeQ;
                end
            end
            storeR: begin
                selA = 1'b0;
```

```
82                      wrA = 1'b0;
83                      wrB = 1'b0;
84                      aluOp = 2'b11;
85
86                      if (dv == 1) begin
87                          NxState = idle;
88                      end else begin
89                          NxState = storeR;
90                      end
91                  end
92                  default: begin
93                      NxState = idle;
94                      selA = 1'b0;
95                      wrA = 1'b0;
96                      wrB = 1'b0;
97                      aluOp = 2'b00;
98                  end
99              endcase
100
101             prStateLed = PrState;
102             nxStateLed = NxState;
103         end
104     endmodule
```


Selector2
SEL[2..0]
DATA[2..0]
OUT
Selector3
SEL[2..0]
DATA[2..0]
OUT
Selector1
SEL[2..0]
DATA[2..0]
OUT
Selector4
SEL[2..0]
DATA[2..0]
OUT
nxStateLed~0
nxStateLed~1
nxStateLed[2..0]
WideOr1
WideOr2
WideOr3
WideOr4
PrState
displayB
clk
idle
dv
load
reset
storeQ
storeR
clock
dv
reset
aluOp~0
aluOp~1
prStateLed~1
prStateLed~0
selA
wrA
wrB
aluOp[1..0]
prStateLed[2..0]

Simulation Waveform Editor - C:/Users/welly/Documents/GitHub/LT39A/pratica04/atv04 - atv04 - [atv04_20240816202130.sim.vwf (Read-Only)]

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Master Time Bar: 0 ps Pointer: 339.2 ns Interval: 339.2 ns Start: End:

Name	Value at 0 ps
clock	B 0
reset	B 1
dv	B 0
aluOp	B 00
nxState...	B 000
prStateL...	B 000
selA	B 0
wrA	B 0
wrB	B 0