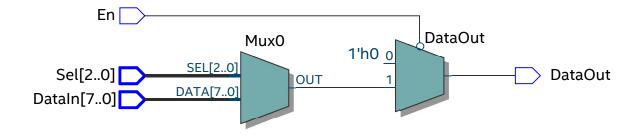
```
1
          library ieee;
          use ieee.numeric_std.all;
use ieee.std_logic_1164.all;
  4
          entity Mux is
    port(
 6
7
8
9
                          DataIn: in std_logic_vector(7 downto 0);
Sel: in std_logic_vector(2 downto 0);
En: in std_logic;
DataOut: out std_logic
10
11
12
13
14
15
16
17
          end entity;
          architecture behavior of Mux is
          signal DataBuffer: std_logic;
18
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32
          begin
                  with Sel select
                                                   DataIn(0) when "000",
DataIn(1) when "001",
DataIn(2) when "010",
DataIn(3) when "011",
DataIn(4) when "100",
DataIn(5) when "101",
                  DataBuffer <=
                                                   DataIn(6) when "110", DataIn(7) when "111", '0' when OTHERS;
                  DataOut <= DataBuffer when En = '0' else '0';
33
34
          end architecture;
```

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