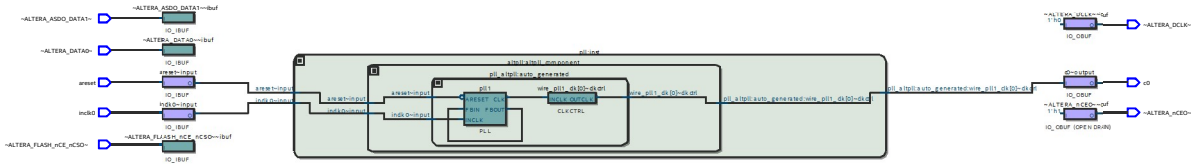
~ALTERA_ASDO_DATA1~
~ALTERA_ASDO_DATA1~~ibuf
IO_IBUF
~ALTERA_DATA0~
~ALTERA_DATA0~~ibuf
IO_IBUF
areset
areset~input
IO_IBUF
inclk0
inclk0~input
IO_IBUF
~ALTERA_FLASH_nCE_nCSO~
~ALTERA_FLASH_nCE_nCSO~~ibuf
IO_IBUF
areset~input
inclk0~input
pll~inst
altpll:altpll_component
pll_altpll:auto_generated
areset~input
inclk0~input
pll1
RESET
CLK
FBIN
FBOUT
VCLK
PLL
wire_pll1_clk[0]~clkctrl
VCLK OUTCLK
CLK CTRL
wire_pll1_clk[0]~clkctrl
pll_altpll:auto_generated|wire_pll1_clk[0]~clkctrl
pll_altpll:auto_generated|wire_pll1_clk[0]~clkctrl
IO~output
IO_OBUF
~ALTERA_nCEO~~ibuf
IO_OBUF (OPEN DRAIN)
~ALTERA_DCLK~~ibuf
IO_OBUF
~ALTERA_DCLK~
o0
~ALTERA_nCEO~