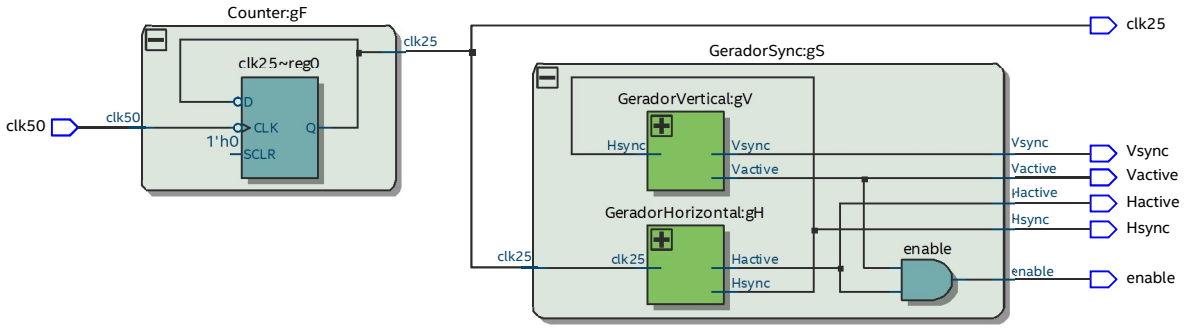
```
1   module GeradorControle (
2       input wire clk50,
3       output wire clk25,
4       output wire Hsync, Hactive,
5       output wire Vsync, Vactive,
6       output wire enable
7   );
8
9       Counter gF(clk50,clk25);
10      GeradorSync gS(clk25, Hsync, Hactive, Vsync, Vactive, enable);
11  endmodule
```

```
1   module Counter (
2       input wire clk50,
3       output reg clk25
4   );
5
6       always @(negedge clk50) begin
7           clk25 <= ~clk25;
8       end
9
10  endmodule
```

```
1   module GeradorSync (
2       input wire clk25,
3       output wire Hsync, Hactive,
4       output wire Vsync, Vactive,
5       output wire enable
6   );
7
8       GeradorHorizontal gH(clk25,Hsync, Hactive);
9       GeradorVertical gV(Hsync,Vsync, Vactive);
10      assign enable = Hactive & Vactive;
11
12  endmodule
```

```
1   module GeradorHorizontal (
2       input wire clk25,
3       output reg Hsync, Hactive
4   );
5
6       localparam  Hp = 96, Hbp = 48,
7                   Hact = 640, Hfp = 16;
8
9       reg[9:0] count;
10
11      always @(posedge clk25) begin
12          count <= count + 10'd1;
13          if (count == Hp) Hsync <= 1'b1;
14          else if(count == Hp+Hbp) Hactive <= 1'b1;
15          else if(count == Hp+Hbp+Hact) Hactive <= 1'b0;
16          else if(count == Hp+Hbp+Hact+Hfp) begin
17              Hsync <= 1'b0;
18              count <= 10'd0;
19          end
20      end
21
22  endmodule
```

```
1   module GeradorVertical (
2       input wire Hsync,
3       output reg Vsync, Vactive
4   );
5
6       localparam  Vp = 2, Vbp = 31,
7                   Vact = 480, Vfp = 11;
8
9       reg[9:0] count;
10
11      always @(posedge Hsync) begin
12          count <= count + 10'd1;
13          if (count == Vp) Vsync <= 1'b1;
14          else if(count == Vp+Vbp) Vactive <= 1'b1;
15          else if(count == Vp+Vbp+Vact) Vactive <= 1'b0;
16          else if(count == Vp+Vbp+Vact+Vfp) begin
17              Vsync <= 1'b0;
18              count <= 10'd0;
19          end
20      end
21
22  endmodule
```


Counter:gF
clk25~reg0
D
CLK
Q
SCLR
1'h0
clk50
clk50
clk25
clk25
GeradorSync:gS
GeradorVertical:gV
Hsync
Vsync
Vactive
GeradorHorizontal:gH
clk25
Hactive
Hsync
enable
Vsync
Vactive
Hactive
Hsync
enable
clk25

Simulation Waveform Editor - C:/Users/welly/Documents/GitHub/LT39A/pratica07/atv07 - atv07 - [atv07_20240907164307.sim.vwf (Read-Only)]

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Master Time Bar: 0 ps Pointer: 456.61 ns Interval: 456.61 ns Start: End:

Name	Value at 0 ps
clk50	B 0
Hactive	B 0
Hsync	B 0
Vactive	B 0
Vsync	B 0
clk25	B 0
enable	B 0