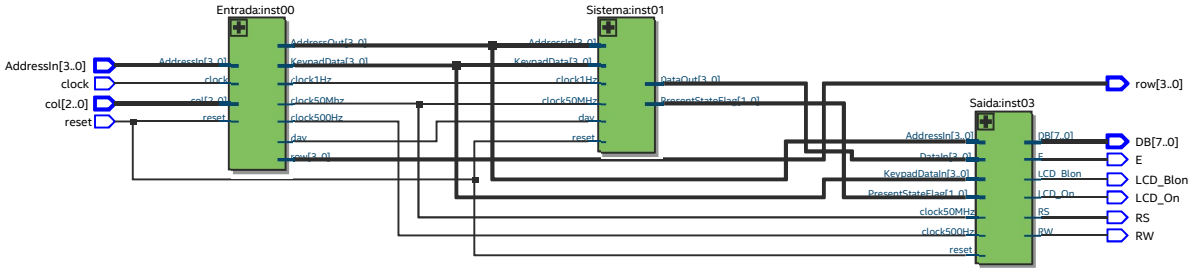
```
1   module arquitetura (
2       input wire clock, reset,
3       input wire[3:0] AddressIn,
4
5       input wire[2:0] col,
6       output wire[3:0] row,
7
8       output wire RS,RW,
9       output wire E,
10      output wire[7:0] DB,
11      output wire LCD_Blon, LCD_On
12  );
13
14      wire clock50MHz, clock500Hz, clock1Hz, dav;
15      wire[3:0] AddressOut, KeypadData;
16      Entrada inst00 (clock, reset, clock50MHz, clock500Hz, clock1Hz, AddressIn, AddressOut
    , col, row, KeypadData, dav);
17
18      wire[3:0] DataOut;
19      wire[1:0] PresentStateFlag;
20      Sistema inst01(clock50MHz, clock1Hz, reset, dav, KeypadData, AddressOut, DataOut,
    PresentStateFlag);
21
22      Saida inst03(clock50MHz, clock500Hz, reset, AddressOut, DataOut, KeypadData,
    PresentStateFlag, RS, RW, E, DB, LCD_Blon, LCD_On);
23  endmodule
```


Entrada:inst00
Sistema:inst01
Saida:inst03
AddressIn[3..0]
clock
col[2..0]
reset
row[3..0]
DB[7..0]
E
LCD_Blon
LCD_On
RS
RW

Entity:Instance	Logic Cells	ed Logic R	I/O Registers	Memory Bits	M9Ks	DSP Elements	DSP 9x9	DSP 18x18	Pins	Virtual Pins	LUT-Only LCs	Register-Only LCs	LUT/Register LCs	Full Hierarchy Name
Cyclone IV E: EP4CE115F29C7														
arquitetura	411 (0)	204 (0)	0 (0)	0	0	0	0	0	26	0	207 (0)	44 (0)	160 (0)	|arquitetura
Entrada:inst00	167 (0)	103 (0)	0 (0)	0	0	0	0	0	0	0	64 (0)	3 (0)	100 (0)	|arquitetura|Entrada...
ClockDivider:inst01	155 (155)	94 (94)	0 (0)	0	0	0	0	0	0	0	61 (61)	3 (3)	91 (91)	|arquitetura|Entrada...
keypadEncoder:inst02	12 (5)	9 (5)	0 (0)	0	0	0	0	0	0	0	3 (0)	0 (0)	9 (2)	|arquitetura|Entrada...
Sistema:inst01	129 (5)	79 (0)	0 (0)	0	0	0	0	0	0	0	50 (5)	40 (0)	39 (0)	|arquitetura|Sistem...
ControlUnit:inst00	5 (5)	3 (3)	0 (0)	0	0	0	0	0	0	0	2 (2)	1 (1)	2 (2)	|arquitetura|Sistem...
Timer:inst01	11 (11)	8 (8)	0 (0)	0	0	0	0	0	0	0	3 (3)	1 (1)	7 (7)	|arquitetura|Sistem...
RamMemory:inst02	108 (108)	68 (68)	0 (0)	0	0	0	0	0	0	0	40 (40)	38 (38)	30 (30)	|arquitetura|Sistem...
Saida:inst03	116 (0)	22 (0)	0 (0)	0	0	0	0	0	0	0	93 (0)	1 (0)	22 (0)	|arquitetura|Saida:in...
PhraseBank:inst01	74 (35)	7 (0)	0 (0)	0	0	0	0	0	0	0	67 (35)	0 (0)	7 (0)	|arquitetura|Saida:in...
DisplayControlUnit:inst02	42 (42)	15 (15)	0 (0)	0	0	0	0	0	0	0	26 (26)	1 (1)	15 (15)	|arquitetura|Saida:in...