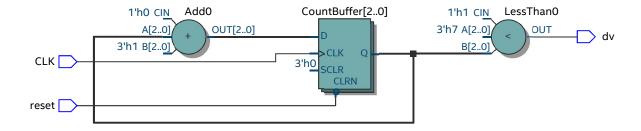
Date: June 13, 2024 Project: atv02





```
1
      library ieee;
     use ieee numeric_std all;
     use IEEE STD_LOGIC_1164 ALL;
     use IEEE.STD_LOGIC_ARITH.ALL;
     use IEEE.STD_LOGIC_UNSIGNED .ALL;
 67
     entity Mod8Counter is
 8
          port (
10
               CLK,reset: in std_logic;
               dv: out std_logic
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     end entity;
      architecture behavior of Mod8Counter is
     begin
process(CLK, reset)
          variable CountBuffer: std_logic_vector(2 downto 0);
               if(reset = '0') then
   CountBuffer := "000";
               elsif rising_edge (CLK) then
CountBuffer := CountBuffer + 1;
               if(CountBuffer >= 7) then
                    dv <= '1';
                    dv <= '0';
               end if;
          end process;
     end architecture;
40
```

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