```
1   module GeradorControle (
2       input wire clk50,
3       output wire clk25,
4       output wire Hsync, Hactive,
5       output wire Vsync, Vactive,
6       output wire enable
7   );
8
9       Counter gF(clk50,clk25);
10      GeradorSync gS(clk25, Hsync, Hactive, Vsync, Vactive, enable);
11  endmodule
```