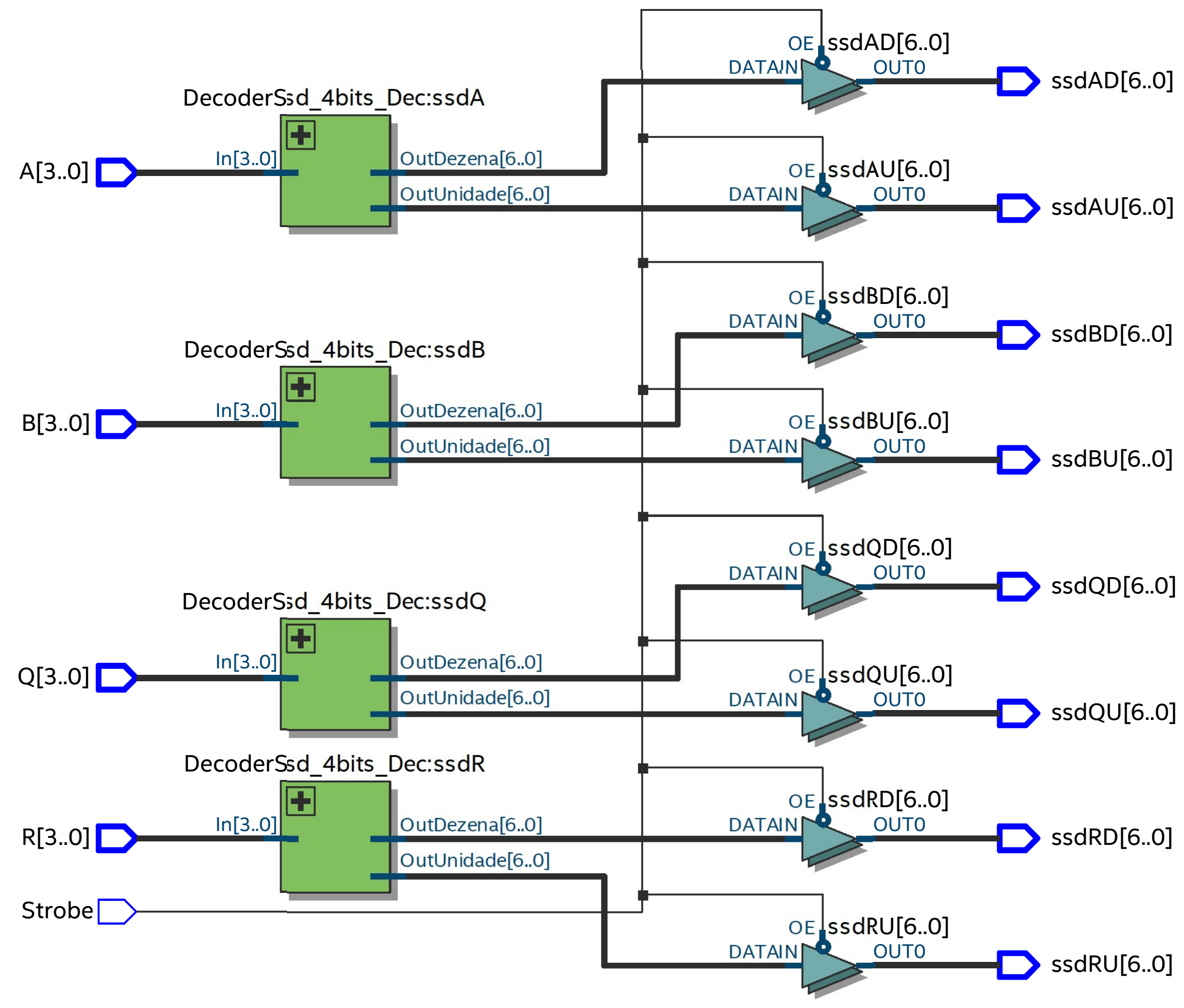
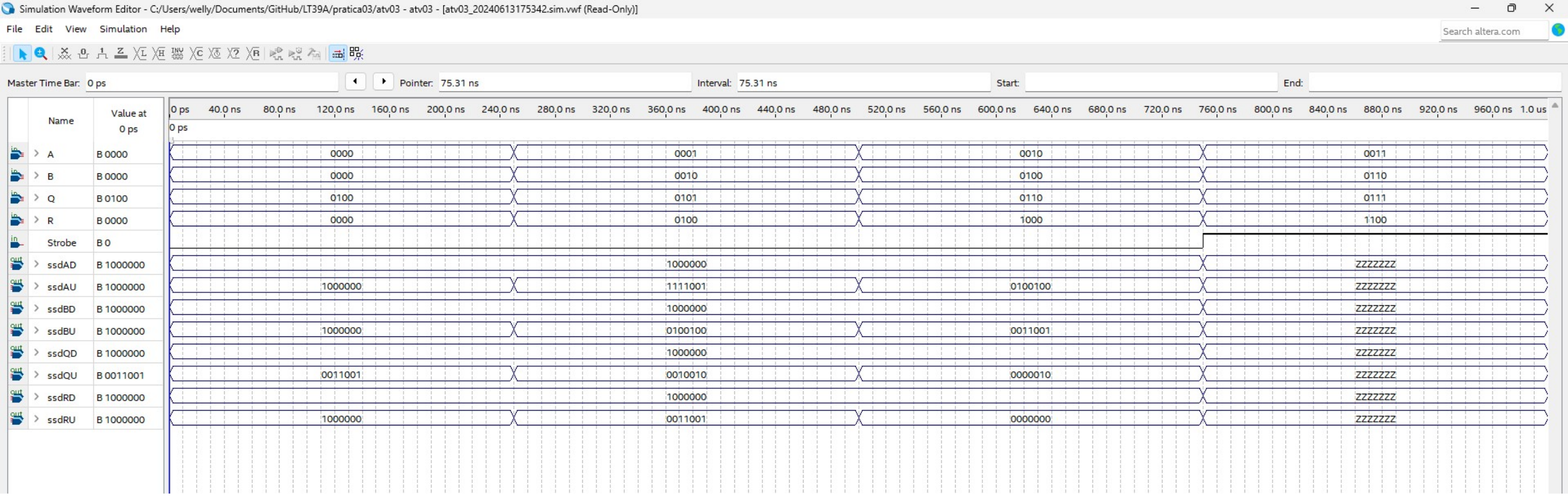


DecoderSsd_4bits_Dec:ssdA
DecoderSsd_4bits_Dec:ssdB
DecoderSsd_4bits_Dec:ssdQ
DecoderSsd_4bits_Dec:ssdR
A[3..0]
B[3..0]
Q[3..0]
R[3..0]
Strobe
In[3..0]
OutDezena[6..0]
OutUnidade[6..0]
OE
DATAIN
OUT0
ssdAD[6..0]
ssdAU[6..0]
ssdBD[6..0]
ssdBU[6..0]
ssdQD[6..0]
ssdQU[6..0]
ssdRD[6..0]
ssdRU[6..0]

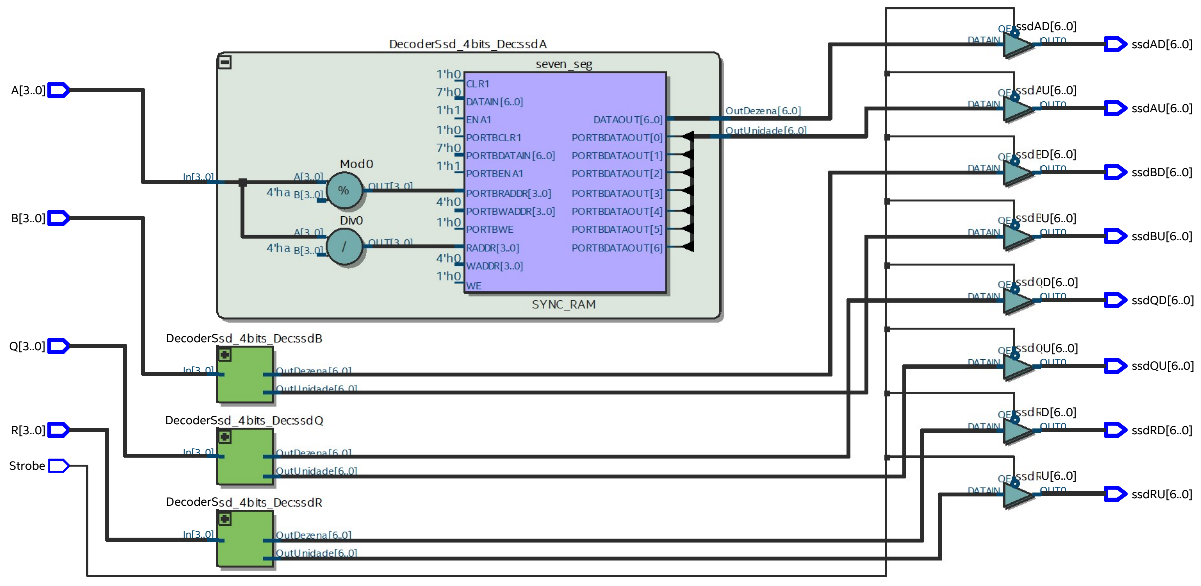

Simulation Waveform Editor - C:/Users/welly/Documents/GitHub/LT39A/pratica03/atv03 - atv03 - [atv03_20240613175342.sim.vwf (Read-Only)]

File Edit View Simulation Help

Master Time Bar: 0 ps   Pointer: 75.31 ns   Interval: 75.31 ns   Start: End:

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

Name	Value at 0 ps				
A	B 0000	0000	0001	0010	0011
B	B 0000	0000	0010	0100	0110
Q	B 0100	0100	0101	0110	0111
R	B 0000	0000	0100	1000	1100
Strobe	B 0				
ssdAD	B 1000000		1000000		ZZZZZZZ
ssdAU	B 1000000	1000000	1111001	0100100	ZZZZZZZ
ssdBD	B 1000000		1000000		ZZZZZZZ
ssdBU	B 1000000	1000000	0100100	0011001	ZZZZZZZ
ssdQD	B 1000000		1000000		ZZZZZZZ
ssdQU	B 0011001	0011001	0010010	0000010	ZZZZZZZ
ssdRD	B 1000000		1000000		ZZZZZZZ
ssdRU	B 1000000	1000000	0011001	0000000	ZZZZZZZ


DecoderSsd_4bits_Dec:ssdA
seven_seg
SYNC_RAM
Mod0
Div0
A[3..0]
B[3..0]
Q[3..0]
R[3..0]
Strobe
DecoderSsd_4bits_Dec:ssdB
DecoderSsd_4bits_Dec:ssdQ
DecoderSsd_4bits_Dec:ssdR
ssdAD[6..0]
ssdAU[6..0]
ssdBD[6..0]
ssdBU[6..0]
ssdQD[6..0]
ssdQU[6..0]
ssdRD[6..0]
ssdRU[6..0]

```verilog
module DecoderSsd_4bits_Dec  (input [3:0]In, output [6:0]OutDezena,OutUnidade);

   reg [6:0] seven_seg [0:9];

   initial begin
      seven_seg[0] = 7'b1000000;
      seven_seg[1] = 7'b1111001;
      seven_seg[2] = 7'b0100100;
      seven_seg[3] = 7'b0110000;
      seven_seg[4] = 7'b0011001;
      seven_seg[5] = 7'b0010010;
      seven_seg[6] = 7'b0000010;
      seven_seg[7] = 7'b1111000;
      seven_seg[8] = 7'b0000000;
      seven_seg[9] = 7'b0011000;
   end

   reg[3:0] Dezena;
   reg[3:0] Unidade;

   always @(In)
   begin

      Dezena = In / 10;
      Unidade = In % 10;

   end

    assign OutDezena = seven_seg[Dezena];
    assign OutUnidade = seven_seg[Unidade];


endmodule
```

```verilog
module Saida(input [3:0]Q,R,A,B, input Strobe, output [6:0]ssdQD,ssdQU,ssdRD,ssdRU,ssdAD,
ssdAU,ssdBD,ssdBU);

   wire [6:0]ssdQDs,ssdQUs,ssdRDs,ssdRUs,ssdADs,ssdAUs,ssdBDs,ssdBUs;

   DecoderSsd_4bits_Dec  ssdA(A,ssdADs,ssdAUs);
   DecoderSsd_4bits_Dec  ssdB(B,ssdBDs,ssdBUs);
   DecoderSsd_4bits_Dec  ssdQ(Q,ssdQDs,ssdQUs);
   DecoderSsd_4bits_Dec  ssdR(R,ssdRDs,ssdRUs);

   assign ssdQD = (Strobe == 1'b0) ? ssdQDs : 7'bZZZZZZZ;
   assign ssdQU = (Strobe == 1'b0) ? ssdQUs : 7'bZZZZZZZ;
   assign ssdRD = (Strobe == 1'b0) ? ssdRDs : 7'bZZZZZZZ;
   assign ssdRU = (Strobe == 1'b0) ? ssdRUs : 7'bZZZZZZZ;
   assign ssdAD = (Strobe == 1'b0) ? ssdADs : 7'bZZZZZZZ;
   assign ssdAU = (Strobe == 1'b0) ? ssdAUs : 7'bZZZZZZZ;
   assign ssdBD = (Strobe == 1'b0) ? ssdBDs : 7'bZZZZZZZ;
   assign ssdBU = (Strobe == 1'b0) ? ssdBUs : 7'bZZZZZZZ;


endmodule
```