```
1   module ALU2bits (
2       input wire [3:0] inputA, // 4-bit input A
3       input wire [3:0] inputB, // 4-bit input B
4       input wire [1:0] opcode, // 2-bit opcode
5       output reg [3:0] result   // 4-bit output result
6   );
7
8       wire[3:0]Q,R;
9       Divisor Divisor01(Q,R,inputA,inputB);
10      always @(*) begin
11          case (opcode)
12              2'b00: begin
13                   result = inputA;
14              end
15              2'b01: begin
16                  result = inputB;
17              end
18
19              2'b10: begin
20                  result = Q;
21              end
22
23              2'b11: begin
24                  result = R;
25              end
26
27              default: begin
28                  result = 4'b0000;
29              end
30          endcase
31      end
32
33  endmodule
```