

```
1  module GeradorImagem (
2      input wire clk25,
3      input wire Hsync, Hactive,
4      input wire Vsync, Vactive,
5      input wire enable,
6
7      input wire[8:0] CircleRow,
8      input wire[9:0] CircleCol,
9
10     output reg[7:0] R,G,B
11 );
12
13 wire[8:0] Row;
14 wire[9:0] Col;
15 ContadorLinha contLinha(Hsync, Vsync, Vactive, Row);
16 ContadorColuna contColuna(Hsync, clk25, Hactive, Col);
17
18 wire [8:0] RowInferior, RowSuperior;
19 wire [9:0] ColInferior, ColSuperior;
20
21 reg[9:0] DistanceToEnd;
22
23
24 assign RowInferior = CircleRow - 9'd20;
25 assign RowSuperior = CircleRow + 9'd20;
26 assign ColInferior = CircleCol - 10'd15;
27 assign ColSuperior = CircleCol + 10'd15;
28
29
30
31
32 //teste
33
34 reg [20:0] CircleEquation;
35 reg [20:0] RadiusSquared;
36 reg [9:0] x_diff;
37 reg [8:0] y_diff;
38
39
40 localparam [9:0] RADIUS = 10'd30;
41
42 always @(enable,CircleRow,CircleCol,Row,Col) begin
43     if( enable == 1'b1) begin
44
45         x_diff = (Col > CircleCol) ? (Col - CircleCol) : (CircleCol - Col);
46         y_diff = (Row > CircleRow) ? (Row - CircleRow) : (CircleRow - Row);
47
48         CircleEquation = (x_diff * x_diff) + (y_diff * y_diff);
49         RadiusSquared = RADIUS * RADIUS;
50
51         if (CircleEquation <= RadiusSquared) begin
52             // If pixel is within the circle
53             R <= 8'h00;
54             G <= 8'h00;
55             B <= 8'hff;
56         end
57
58         else begin
59             R <= 8'hff;
60             G <= 8'hff;
61             B <= 8'hff;
62         end
63     end
64     else begin
65         R <= 8'h00;
66         G <= 8'h00;
67         B <= 8'h00;
68     end
69 end
70 endmodule
```

```
1  module ContadorLinha (  
2      input wire Hsync, Vsync, Vactive,  
3      output reg[8:0] row  
4  );  
5  
6      always @(posedge Hsync ) begin  
7          if (Vsync == 1'b0) row <= 9'd0;  
8          else if (Vactive == 1'b1) row <= row + 9'd1;  
9      end  
10  
11  endmodule
```

```
1  module ContadorColuna (  
2      input wire Hsync, clk25, Hactive,  
3      output reg[9:0] col  
4  );  
5  
6      always @(posedge clk25 ) begin  
7          if (Hsync == 1'b0) col <= 10'd0;  
8          else if (Hactive == 1'b1) col <= col + 10'd1;  
9      end  
10  
11  endmodule
```



