Introduction to Verilog

Instructions: The purpose of this lab is to practice using Verilog by creating and testing a simple circuit.

Please note, all code must be in the 'lab01' directory. This directory is case sensitive!

Part 1:

For part one we will fork the repository, install Icarus Verilog, and install gtkWave.

- 1. Visit http://www.github.com and create an account if you do not already have one.
- 2. Email me your account name (if you haven't already). My email is pwest@csuniv.edu.
- 3. Once I email you back you should be part of the CSU-CS organization and have access to the csci-330-spring-2018 repository.
- 4. Fork the repository.
- 5. Windows: install git-scm and make sure to integrate with the Windows command prompt. All other installation options should be the defaults.
- 6. Linux: Install git with your favorite package manager.
- 7. Mac: Look for the git dev tools and install.
- 8. Windows: Right-click on your desktop and select Run Git Bash Here. Linux/Mac: Start a command prompt and navigate to where you want your repository to exist.
- 9. On you local machine checkout the repository: \$ git clone <url to your repository> (Note: this make take awhile.)
- 10. Open Git Bash in your repository (make sure you are in your repository!)
- 11. After checkout, enter the new directory and add upstream: git remote add upstream https://github.com/csu-cs/csci-330-spring-2018.git This upstream will need for later updates.
- 12. Install iVerilog (Windows: http://bleyer.org/icarus/, Linux/Mac: You package manager or http://iverilog.icarus.com/).
- 13. Finally install gtkwave (http://sourceforge.net/projects/gtkwave/)

Part 2:

Create two modules for each circuit describe in figure 1. Please create two separate files named:

1. circuitlong.v

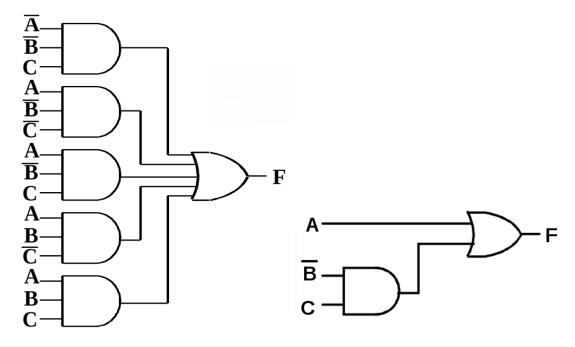


Figure 1: The two circuits for Part 2

2. circuitshort.v

Part 3:

Create another Verilog file that tests the inputs and outputs of your program. Make sure to include a dump to a .vcd file so that I may inspect your output. Name your files:

- 1. circuitlong-test.v
- 2. circuitshort-test.v

How to turn in:

Turn in via GitHub. Ensure the file(s) are in your lab01 directory and push via the command line:

- \$ git add <files>
- \$ git commit
- \$ git push

Due Date: January 24, 2018 2359

Teamwork: No teamwork, your work must be your own.