**Computer Architecture 2025**

**Exercise Session Report**

Group:

Name and student number:

Date:

**Part 1: Fill in the Design Metrics**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***Implementation*** | ***Simulation*** | ***Backend*** | | | | | | |
| *Synthesis* | | | | *Floorplan* | *Signoff* | |
| *# of Cycles for MULT\** | *Design*  *area (μm2)* | *Critical path*  *(ns)* | *Maximum operating frequency (MHz)* | *Minimal time to execute the MULT (ns)* | *Die area (μm2)* | *Area utilization (%)* | *Maximum operating frequency (MHz)* |
| *1. Single Cycle\*\** |  |  |  |  |  | *\*\*\** |  |  |
| *2. Single Cycle with Multiplication* |  |  |  |  |  |  |  |  |
| *3a. Basic Pipelined* |  |  |  |  |  |  |  |  |
| *3b. Basic Pipelined (50MHz, preset 1)* |  |  |  |  |  |  |  |  |
| *3c. Basic Pipelined (50MHz, preset 2)* |  |  |  |  |  |  |  |  |
| *4. Pipelined with hazard logic* |  |  |  |  |  |  |  |  |
| *5. Advanced acceleration* |  |  |  |  |  |  |  |  |

*\* The program*

* *MULT1 is for “1. Single cycle”;*
* *MULT2 is for “2. Single Cycle with Multiplication” and “3a/3b. Basic Pipelined”;*
* *MULT3 is for “4. Pipelined with hazard logic”;*
* *MULT4 (or your modified version of it) is used for “5. Advanced acceleration”.*

*\*\* Implementations 1, 2, 3a, 4 and 5 have a clock frequency of 10MHz and should be synthesized under the default strategy preset “AREA 0”.*

*Presets 1 & 2 must be replaced by your synthesis strategy after performing the Synthesis Exploration step (e.g., DELAY 0-4/AREA 0-3)*

*\*\*\* The grey regions are not required to fill in.*

**Part 2: Answer the Questions based on Your Designs**

***Questions:***

1. *What is the critical path of the single-cycle processor (simple program)? Which operation does this critical path stand for?*

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1. *For the single-cycle processor, what are the top-5 components in terms of area? After adding MULT-support, what are the top-5 components then? What has the changed? What is your explanation for this?*

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1. *What is the critical path after you support the MULT operation in the single-cycle processor? Is there anything changed? What is your explanation for this?*

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1. *Regarding to your findings in Q2 & Q3, do you think adding MULT-operator support is always a good choice for any microprocessor? Please elaborate your answer.*

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1. *What is the critical path of your basic pipelined design? How does the critical path length change compare to the single-cycle version? What about your final advanced version? Try to discuss the benefits and costs of processor pipelining according to your findings (hint: speed/throughput/area/power/etc.).*

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1. *What techniques have you applied to accelerate MULT4? Explain under what conditions/workloads your strategies would have the maximum/minimum performance gain. What is the cost for your strategy?*

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1. *(Backend Flow) Please explain the following terms of the backend flow: PDK, LEF, CTS, STA, GDSII. Which PDK are we using?*

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1. *(Backend Flow) Have you encountered any warnings/errors in the backend session? What are they? How do you fix those critical issues?*

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1. *(Backend Flow) The major steps of this session’s backend flow are Synthesis, Floorplan, Placing and Routing. Have a look at the “runs/results/” folder. What output files does each step generate? Anything similar/different between steps? What are the later steps doing upon the previous?  
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1. *(Backend Flow) Try to compare between the three full-flow scenarios. What is the impact of the target clock frequency? What is the impact of different synthesis strategy presets? Please discuss the tradeoff in terms of speed and area, i.e. if not using AREA-0, which preset will you choose after the synthesis exploration and why?*

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1. *(Optional survey) Have you used LLM services to help with this project (as suggested in Session1-Page8)? If so, which model/service? What the task have you submitted? To which extent do you find it helpful? Or, does it misguide your exploration? What is your general opinion/suggestion on using LLMs in this course?*

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**Part 3: Post your design photos**

*Following the step “****Analysis and Discussion #5****” in Jupyter Lab, take a screenshot of the final die photo. If the signoff is unavailable, post the photo from the furthest stage you can reach with your RTL and mention the stage of it.*

*Photo 1: Signoff - Basic Pipelined (10MHz)*

*Photo 2: Signoff - Basic Pipelined (50MHz)*