1. Optimization to a processor that will improve **both** throughput and latency and another example, that improves **throughput** but may not have any impact latency
2. Describe ways by which you can reduce the power consumption of a processor
3. Describe 2 ways by which you can improve the **yield**  in the manufacturing of a processor



a) If we increase the voltage of the processor by double, from 1V to 2V how much power increase in processor are we expecting to have? Power=CV2F

power new = 2C (2V)2 2f

power old = c V2 f

2.22.2 = 16

b) Which of power or energy optimization is most important in mobile processors? How about server scale architectures?

**c) Consider the two following sequence of the same code compiled with two different method 1 and 2.**

**which one is faster and by how much?**

|  |  |  |  |
| --- | --- | --- | --- |
| Class | A | B | C |
| CPI for class | 2 | 4 | 1 |
| IC in compiled sequence 1 | 1 | 2 | 3 |
| IC in compiled sequence 2 | 4 | 1 | 2 |

IC sequence 1: 1\*2 + 2\*4 + 3\*1 = 13 clock cycles: CPI: 13/6

IC sequence 2: 4\*2 + 1\*4 + 2\*1 = 14 clock cycles. CPI: 14/7

**Question 1** What are the differences between stack and heap? **( 3 points)**

(a) which one is larger?

(b)which one is managed by the compiler?

(c) which one can be accessed faster?

**Question 2** **( 6 points)**

Assume all registers are 32 bits. Assume all numbers are expressed in **hexadecimal** notation. Remember RISC-V uses Little Endian notation.

Initially Memory [00000064] = 456789AB and register x6 contains 00000064.

What are the contents of registers x5, x6, x7, x8, x9 and memory location 00000064 after the execution of the following RISC-V code.

lw x5, 0(x6) x5 = 456789AB

lb x7, 2(x6). x7 = 00000067

lbu x8, 2(x6) x8 = 00000067

lh x9, 1(x6) x9 = 00004567

addi x10, x0, -5. 0000000101

111111111010: 1011

000000000001

x10 = -5 = FFFF FFFB

x5 = x6 = x7 = x8 =

x9 =

**Question 3 (2+2+2 = 6 points)**

Consider the following RISC-V code –

500 add x6, x9, x0 #address of this instruction is decimal 500

504 add x7, x2, x0

508. jal x1, L

512. sub x9, x10, x0

…

1000 L: la x9, Class #address of this instruction is decimal 1000

1004 lw x10, 0(x9)

1008 addi x10, x14, -5

beq x10, x0, L

jalr x0, 0(x1)

1. What is the value of PC and register x1 **after** the execution **jal L** instruction? Explain your answer.

**PC=1000, X1: 512**

1. What is the value of PC and register x0 **after** the execution of **jalr x0, 0(x1)?** Explain your answer

**PC = 512, X0: 0**

**A better compiler optimization:**

**a)**

**1) reduce instruction count**

**2) increase instruction count**

**3)does not change**

**b)**

**1) reduce CPI**

**2)increase CPI**

**3)sometime reduce sometime increase**

**How does compiler optimization sensitive to algorithm and programming language?**