University of California, Davis
Department of Electrical and Computer Engineering

EEC180 DIGITAL SYSTEMS II Winter Quarter 2021

LAB 3: Finite State Machine (FSM) Design and Implementation

Objective: In this lab you will design a Mealy FSM for the given sequence detector task and use Verilog to implement the sequence detector.

Prelab

Read the lab carefully and draw the state diagram of the FSM.

I. Mealy FSM

Design and implement the following FSM in Verilog :

A Mealy finite state machine has one input X and one output Z. The output Z = 1 occurs when the sequence 101 is observed on the input X, provided that the sequences 000 and 111 did not yet appear on X.

Once the sequence 000 is observed on X, the output Z becomes 0 and remains 0 indefinitely. Also, once the sequence 111 is observed on X, the output Z becomes 1 and remains 1 indefinitely.

II. Testing

- Write a Verilog testbench for the following two cases, verify the functionality of your design, and demonstrate it to your TA.

X	0	1	0	1	0	1	0	0	1	0	1	0	0	0	1	0	1	1	1	1
Z	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

X	0	1	0	1	0	1	0	0	1	0	1	1	1	0	1	0	1	0	0	0
Z	0	0	0	1	0	1	0	0	0	0	1	0	1	1	1	1	1	1	1	1

III. Lab report

For your lab report, include the following:

- Mealy machine state diagram.
- Complete Verilog source code.
- Simulation waveforms/screenshot of the transcript window from your functional simulation.
- Statement of contribution of each team member.

IV. Grading Guidelines

- Prelab 10 points
- Functional Simulation Check off 65 points
- Lab Report 25 points