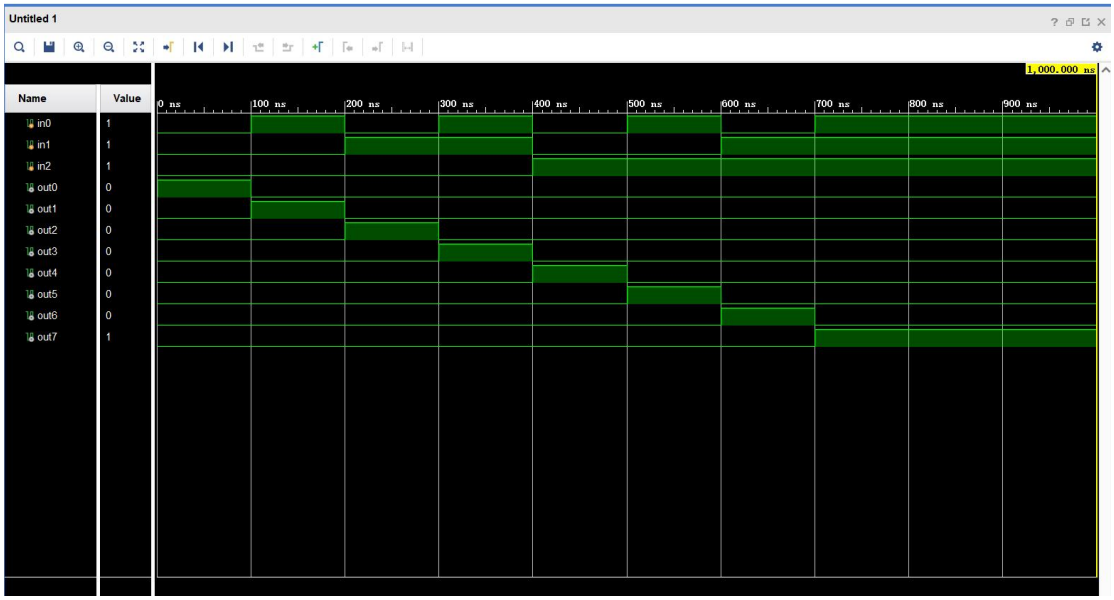


```
21
22
23  module test_01(
24      input wire in0,
25      input wire in1,
26      input wire in2,
27      output wire out0,
28      output wire out1,
29      output wire out2,
30      output wire out3,
31      output wire out4,
32      output wire out5,
33      output wire out6,
34      output wire out7
35      );
36      assign out7 = (in2 & in1) & in0;
37      assign out6 = (in2 & in1) & !in0;
38      assign out5 = (in2 & !in1) & in0;
39      assign out4 = (in2 & !in1) & !in0;
40      assign out3 = (!in2 & in1) & in0;
41      assign out2 = (!in2 & in1) & !in0;
42      assign out1 = (!in2 & !in1) & in0;
43      assign out0 = (!in2 & !in1) & !in0;
44  endmodule
45
```

```
22
23  module tb_test_01(
24
25      );
26      reg in0;
27      reg in1;
28      reg in2;
29      wire out0;
30      wire out1;
31      wire out2;
32      wire out3;
33      wire out4;
34      wire out5;
35      wire out6;
36      wire out7;
37      initial
38      begin
39        in0 <= 0;
40        in1 <= 0;
41        in2 <= 0;
42      #100
43        in0 <= 1;
44        in1 <= 0;
45        in2 <= 0;
46      #100
47        in0 <= 0;
48        in1 <= 1;
49        in2 <= 0;
50      #100
51        in0 <= 1;
52        in1 <= 1;
```

E:/project_5/project_5.srcs/sim_1/new/tb_test_01.v

```
43        in0 <= 1;
44        in1 <= 0;
45        in2 <= 0;
46      #100
47        in0 <= 0;
48        in1 <= 1;
49        in2 <= 0;
50      #100
51        in0 <= 1;
52        in1 <= 1;
53        in2 <= 0;
54      #100
55        in0 <= 0;
56        in1 <= 0;
57        in2 <= 1;
58      #100
59        in0 <= 1;
60        in1 <= 0;
61        in2 <= 1;
62      #100
63        in0 <= 0;
64        in1 <= 1;
65        in2 <= 1;
66      #100
67        in0 <= 1;
68        in1 <= 1;
69        in2 <= 1;
70      end
71
72      test_01 mytest(
73      .in2(in2),
```

Source File Properties

```
        in1 <= 0;
        in2 <= 1;
    #100
        in0 <= 0;
        in1 <= 1;
        in2 <= 1;
    #100
        in0 <= 1;
        in1 <= 1;
        in2 <= 1;
    end

    test_01 mytest(
    .in2(in2),
    .in1(in1),
    .in0(in0),
    .out0(out0),
    .out1(out1),
    .out2(out2),
    .out3(out3),
    .out4(out4),
    .out5(out5),
    .out6(out6),
    .out7(out7)
    );
endmodule

```