Mao-chi Weng

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Education

Ph.D. in Electrical and Computer Engineering, University of Michigan **Expected Aug. 2029**
LEAPS: Lab for Efficient Application Processor, Advisor: Prof. Zhengya Zhang *Ann Arbor, MI*

- Cumulative GPA: 4.0/4.0

B.S. in Electrical Engineering, National Taiwan University **Graduated Aug. 2024**
Taipei, Taiwan

- Cumulative GPA: 3.9/4.0

Publication

Y. -C. Yu*, **M. -C. Weng***, M. -G. Lin and A. -Y. A. Wu, "Retraining-free Constraint-aware Token Pruning for Vision Transformer on Edge Devices," 2024 IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, Singapore, 2024

Teaching Experience

Linear Algebra **Fall 2021**
Teaching Assistant *Department of Electrical Engineering, National Taiwan University*

Selected Projects

Graph Neural Network accelerator **Jan. 2025- May. 2025**
Research Project in LEAPS, advisor: Prof. Zhengya Zhang *ASIC Design*

- Designed and taped out a Graph Neural Network accelerator that supports different Conv kernels in Intel 16nm node.

2-Way Superscaler Out-of-Order Processor **Sept. 2025- Dec. 2025**
Course Project of EECS470 Computer Architecture *CPU Design*

- Designed a 2-way superscaler out-of-order R10k-style CPU with early branch resolution, GShare branch predictor, and return address stack(RAS)

Elliptic Curve Cryptography Processor **Sept. 2021- Jan. 2022**
Course Project of Integrated Circuit Design Laboratory *ASIC Design*

- Designed and taped out a CPU-like processor within area constraint by doing SW/HW co-design in UMC 0.18 um node.

Other Research & Work Experience

NTU Access IC Lab, National Taiwan University **Sept. 2022- Oct. 2023**
Undergraduate Researcher, advisor: Prof. An-Yeu Wu *Taipei, Taiwan*

- Introduced Fisher Token Information on Vision Transformer's tokens to evaluate token importance between blocks.
- Proposed an edge-friendly Vision Transformer retraining-free token pruning scheme that performs better than prior pruning schemes.

Industrial Technology Research Institute **Apr. 2023- Present**
Digital Circuit Research Intern *Hsinchu, Taiwan*

- Built extensions for Coarse-Grained Reconfigurable Array (CGRA) framework to visualize Data-Flow Graph mapping.
- Proposed a modified ILP-based hierarchical CGRA mapping algorithm and reduced 50% compilation time of SOTA mapping algorithm.

Honors and Scholarships

Dean's List Award | *National Taiwan University* **Oct. 2022**

- Awarded to top 5% students in the department of electrical engineering

Exchange Students Scholarship | *NTU-YLL Talent Training Project* **July. 2023**

- Won a scholarship of $15,000 available to outgoing exchange students at NTU (out of 300+ students)

Skills

Programming Languages: Python, C/C++, Matlab, Shell script
IC Design Relatives: Verilog/System Verilog, Design Compiler, Innovus, ICCompiler-II, Virtuoso
Natural Languages: English, Mandarin