Mao-chi (Tom) Weng

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Education

National Taiwan University **Sept. 2019 – Dec. 2023**
Bachelor of Science in Electrical Engineering (Cumulative GPA: 3.91/4.0, Last 60: 3.98/4.0) *Taipei, Taiwan*

- **Dean's List award**, Awarded to NTUEE students with top 5% academic standing
- **Teaching Assistant** of Linear Algebra Fall 2021, advisor: Hung-Yi Lee
- **IC-related coursework:** Computer Architecture, Integrated Circuit Design and Laboratory, Digital Circuit Laboratory, Digital Signal Processing in VLSI
- **ML/CS-related coursework**: Linear Algebra, Data Structure and Algorithm, Machine Learning, Computer Vision

Leiden University **Jan. 2024 – June 2024**
International Student Exchange Program *Leiden, Netherlands*

Research Experience

NTU Access IC Lab, National Taiwan University **Sept. 2022 – Oct. 2023**
Undergraduate Researcher, advisor: Prof. An-Yeu Wu *C++/Python*

- Developed extensions of Compute-In-Memory (CIM) simluation framework to analyze energy consumption of Vision Transformer on CIM devices.
- Introduced Fisher Token Information on Vision Transformer's tokens to evaluate token importance between blocks.
- Proposed a threshold token pruning method for Vision Transformer edge inference that reduces 27% FLOPs with less than 0.4% accuracy drop.

Laboratory for Data Processing Systems, National Taiwan University **Sept. 2020 – June 2021**
Undergraduate Researcher, advisor: Prof. Yi-Chang Lu *Verilog*

- Designed a 143MHz, 1.04 mm^2, Banded Smith-Waterman accelerator from RTL design, Gate Synthesis, to APR.
- Researched on random number generators and the effect of their qualities on Monte-Carlo algorithms by OpenCL.

Publication

Yun-Chia Yu*, **Mao-Chi Weng***, Ming-Guang Lin, An-Yue Wu," *Retraining-free Constraint-aware Token Pruning for Vision Transformer on Edge Devices*", IEEE International Symposium on Circuits and Systems (ISCAS) 2024, to appear (co-first author) — paper link

Selected Projects

Elliptic Curve Cryptography Engine - Tapeout **Feb. 2022 – June 2022**
Course Project of Integrated Circuit Design Laboratory, advisor: Tzi-Dar Chiueh *Python/Verilog, ASIC Design*

- Designed & implemented a CPU-like processor that support ECC 163-bit en/decryption within $2mm^2$ area constraint.
- Taped-out the design to Taiwan Semiconductor Research Institute and manufactured with UMC 0.18um technology.

Object Distance Estimator on FPGA **Sept. 2021 – Jan. 2022**
Course Project of Digital Circuit Laboratory, advisor: Chia-Hsiang Yang *SystemVerilog, FPGA Design*

- Designed hardware and utilized several on-chip IPs on Altera's FPGA to accelerate sum of absolute differences(SAD) algorithm, achieving 81.38FPS throughput under 25MHz clock frequency.

Work Experience

Industrial Technology Research Institute **April 2023 – Dec. 2023**
Digital Circuit Research Intern *(Remote) Hsinchu, Taiwan*

- Built extensions for Coarse-Grained Reconfigurable Array (CGRA) framework to visualize Data-Flow Graph mapping.
- Proposed a modified Integer Linear Programming (ILP)-based hierarchical CGRA mapping algorithm and reduced 35%-50% compilation time of SOTA mapping algorithm.

Honors and Scholarships

Exchange Students Scholarship | *NTU-YLL Talent Training Project* **July 2023**

- Won a scholarship of US$15,000 available to outgoing exchange students at NTU (out of 300+ students).

Second Prize Award | *Integrated Circuit Design Contest 2022, Minister of Education Taiwan* **Nov. 2022**

- Designed a full-functionality Burrows Wheeler Transform Engine in 12 hours, with 2^{nd} smallest chip area among 134 teams in Cell-Based Digital Circuit Design Category.

Skills

Software Relatives: Python, C/C++, Matlab, Shell script, JavaScript, OpenCV, PyTorch, TensorFlow, TensorFlowLite

IC Design Relatives: Verilog/SystemVerilog, RISC-V, Quatus II(FPGA), Design Compiler, Innovus(APR), Verdi(Nwave)