# Wenjia Ruan

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Senior Research Engineer, Qualcomm Research
Santa Clara, California, USA

wenjia@alum.lehigh.edu
http://wenjiaruan.com


## Work Interests

I'm interested in a broad area of heterogeneous, parallel and concurrent programming, especially in designing and implementing high-efficient and scalable software and hardware systems.

## Education

- **Lehigh University** — Bethlehem, PA. USA
  *Ph.D in Computer Science* — *2010 - 2015*
  - Advisor: Michael F. Spear
  - Dissertation: Accelerating Transactional Memory by Exploiting Platform Specificity
- **Lehigh University** — Bethlehem, PA. USA
  *M.S in Computer Science* — *2010 - 2013*
- **Ocean University of China** — Qingdao, China
  *B.S in Electronic Engineering* — *2005 - 2009*

## Professional Experience

- **Qualcomm Research Silicon Valley** — Santa Clara, CA. USA

  ***Senior Research Engineer*** — 08/2015 - Present
  ***Interim Engineering Intern*** — 05/2014 - 08/2014

  I work on "Qualcomm Symphony", in which I own 1) low-level data synchronization between CPU, GPU and DSP, and 2) smart programmable power control (for CPU and GPU) parts.

  Symphony is an SDK that contains APIs to enable general programmers to easily write performant heterogeneous, parallel and power-aware code, and a runtime that schedules and launches computational tasks, manages data synchronization between heterogeneous devices on a mobile SoC, and optimizes power consumptions by manipulating power states of these devices, all behind the scene.

- **Lehigh University CSE Department** — Bethlehem, PA. USA

  ***Research Assistant at Parallelism and Concurrency Lab*** — 06/2011 - 07/2015
  ***Teaching Assistant*** — 08/2010 - 05/2011

  I worked on Transactional Memory (TM), its algorithms (Software and Hybrid TM algorithms), runtime (GCC libitm runtime and RSTM library-based TM runtime) and applications (both micro and macro benchmarks and applications).

## Selected Publications

1. *"Hybrid Transactional Memory Revisited"*, by *Wenjia Ruan* and Michael Spear. 29th International Symposium on Distributed Computing **(DISC 2015)**, Tokyo, Japan. October 2015.
2. *"An opaque Hybrid Transactional Memory"*, by *Wenjia Ruan* and Michael Spear. 10th ACM SIGPLAN Workshop on Transactional Computing **(TRANSACT 2015)**, Portland, OR. June 2015.

3. *"Transactional Tools for the Third Decade"*, by Matthew Kilgore, Stephen Louie, Chao Wang, Tingzhe Zhou, *Wenjia Ruan*, Yujie Liu and Michael Spear. 10th ACM SIGPLAN Workshop on Transactional Computing **(TRANSACT 2015)**, Portland, OR. June 2015.

4. *"Case Study: Using Transactions in Memcached"*, by Michael Spear, *Wenjia Ruan*, Yujie Liu and Trilok Vyas. Transactional Memory: Foundations, Algorithms, Tools, and Applications **(LNCS 8913)**. January 2015.

5. *"Transactional Read-Modify-Write Without Aborts"*, by *Wenjia Ruan*, Yujie Liu and Michael Spear. ACM Transactions on Architecture and Code Optimizations **(TACO)**, January 2015.

6. *"STAMP Need Not Be Considered Harmful"*, by *Wenjia Ruan*, Yujie Liu and Michael Spear. 9th ACM SIGPLAN Workshop on Transactional Computing **(TRANSACT 2014)**, Salt Lake City, UT. March 2014.

7. *"Transactionalizing Legacy Code: An Experience Report Using GCC and Memcached"*, by *Wenjia Ruan*, Trilok Vyas, Yujie Liu and Michael Spear. 19th International Conference on Architectural Support for Programming Languages and Operating Systems **(ASPLOS 2014)**, Salt Lake City, UT. March 2014.

8. *"Boosting Timestamp-based Transactional Memory by Exploiting Hardware Cycle Counters"*, by *Wenjia Ruan*, Yujie Liu and Michael Spear. ACM Transactions on Architecture and Code Optimizations **(TACO)**, December 2013.

9. *"Delaying Operators and Language-Level Semantics"*, by *Wenjia Ruan*, Yujie Liu and Michael Spear. 5th Workshop On the Theory of Transactional Memory **(WTTM 2013)**, Jerusalem, Israel. October 2013.

10. *"On the Platform Specificity of STM Instrumentation Mechanisms"*, by *Wenjia Ruan*, Yujie Liu, Chao Wang and Michael Spear. 2013 International Symposium on Code Generation and Optimization **(CGO 2013)**, Shenzhen, China. February 2013.

## Patents

1. *"Geometric Scheduling with Dynamic Work Trimming"*, U.S. Patent filed in 2016.

2. *"Geometric Work Reorganization for Irregularly-shaped Work Items"*, U.S. Patent filed in 2016.

3. *"Fine-grained Power Optimization for Heterogeneous Parallel Constructs"*, filing in preparation.

## Selected Presentations

1. *"An opaque Hybrid Transactional Memory"*, presented at the 10th ACM SIGPLAN Workshop on Transactional Computing, Portland, OR. June 2015.

2. *"Transactional Read-Modify-Write Without Aborts"*, presented at 2015 European conference on High Performance and Embedded Architecture and Compilation (HiPEAC 2015), Amsterdam, Netherlands. January 2015.

3. *"Crafting a Concurrent Logging System for Qualcomm MARE"*, presented at Qualcomm Research Silicon Valley, Santa Clara, CA. August, 2014

4. *"On the Platform Specificity of STM Instrumentation Mechanisms"*, presented at 2013 International Symposium on Code Generation and Optimization, Shenzhen, China. February 2013.