		SW/HW			January	February				March				April		
ID	**Task**		**Who**	**Status**	**30**	**6**	**13**	**20**	**27**	**6**	**13**	**20**	**27**	**3**	**10**	**17**
1	Training/Testing in Caffe	SW	Wen Wen	Done, Verified												
2	Weights/bias extraction + loader	SW	Wen Wen	Done, Verified												
3	MNIST DB input loader	SW	Wen Wen	Done, Verified												
4	FIFO	HW	Wen Wen	Done, Verified												
5	Pooling Layer	HW	Wen Wen	Done, Verified												
6	BRAM	HW	Thibaut	Done, Verified												
7	Test Bench design	HW	Wen Wen + Thibaut	done												
8	Controller	SW	Thibaut	done												
9	Divide into batch	SW/HW	Thibaut	Done												
10	Sigmoid function in LUT & Fully connected	HW	Thibaut + Jieming	started												
11	Research Router & Controller	HW	Thibaut	Done												
12	Axi Bus	HW	Thibaut	Started												
13	FSM ++	HW	Thibaut	Done, Verified												
14	Convolution + Pooling in C	SW	Jieming	Done, Verified												
15	Fully connected in C	SW	Jieming	Done, Verified												
16	Convolution on DSP slice	HW	Jieming + Thibaut	Done, Verified												
17	Fully connected on DSP slice	HW	Jieming	In-progress												
18	Router	HW	Thibaut	Done, Verified												

Advance Features and Testing