Requirements Traceability Matrix								
Members: Thibaut Lanois, Wen Wen, Jieming Pan								
	Test Case 1	status	Test Case 2	status	Test Case 3	status	Test Case 4	status
	Comparison between Matlab and C	done						
Implementing Pooling layer functions in C	Comparison between Matlab and C	done						
Implementing Fully connected layer functions in C	Fully connected propagete convolution	done	Comparison between Matlab and C	some small difference but not sure about row and column for weight				
Obtain LeNet-5 model in C	percentage superior to 80%	done	percentage superior to 90%	done	Same percentage than C (99.8%)	In progress		
Software / hardware								
Implementing Convolution layer functions	function and setup test: Verify individual multiplication and addition in the pipeline. Check if the weights and biases are loaded correctly, and valid bits are propagated correctly.	Done	Design test: With fixed inputs from controller, in every 9 cycles of kernel multiply-add calculation, the data order and number of multiply-add calculation is as supposed. Input: fabricated data. Output: correctly calculated results.	In progress				
Implementing Pooling layer functions	Individual Design Test (FIFO): 2*2*16-bit FIFO with seperate enable signals functions correctly.	done	Individual Design Test (Pooling): Maximum functions correctly. Input: fetched data in two FIFOs. Output: pooled maximum data.	done	Integrated Test (With Router-Controller-Convolution): Pooling function with input data from convolution layer. Input: feature map data (valid) from previous layer. Output: pooled data and valid bit.	In progress		
Finite state machine	fixed size kernel and input. Output waveform	done	Size move through cycle: output waveform	done				
Router-controller	Fixed-size (32*32), 1 input feature map, 1 output feature map. output: 2 hex number	done	Fixed-size (32*32), 1 input feature map, 6 output feature map. output: 2 hex number	done	Fixed-size (32*32), 6 input feature map, 10 output feature map. output: 2 hex number	In progress	paralelize router output	Not started
Router-controller-Convolution	Fixed-size (32*32), 1 input feature map, 6 output feature map. output: file	In progress	Fixed-size (32*32), 6 input feature map, 10 output feature map. output: file	In progress				
Router-controller-convolution-pooling	Fixed-size (32*32), 1 input feature map, 6 output feature map. output: file	In progress	1 input image convolution and pooling for 2 layer. output: file	In progress	1 input image convolution and pooling for every layer. output: file	In progress	1 input image convolution and pooling for every layer but more paralelism. output: file	Not started
Softmax function in LUT	Load features map to the CPU and make softmax with CPU	In progress	Checking loading and unloading of BRAM with exponential lookup table content. Verify Relu function output is achieved	Not started	Design test: Verify each section of the pipeline input and output. Test softmax function calculation results.	Not started		
Axi bus								
Integration								
Route placement								