5.0 Electrical Layer (2D and 2.5D)

Key attributes of electrical specification include:

- Support for 4, 8, 12, 16, 24, and 32 GT/s data rates
- Support for Advanced and Standard package interconnects
- Support for clock and power gating mechanisms
- Single-ended unidirectional data signaling
- DC coupled point-to-point interconnect
- Forwarded clock for transmit jitter tracking
- Matched length interconnect design within a module
- Tx driver strength control and unterminated Rx for Advanced Package
- Tx termination and data rate and channel reach dependent Rx termination for Standard Package

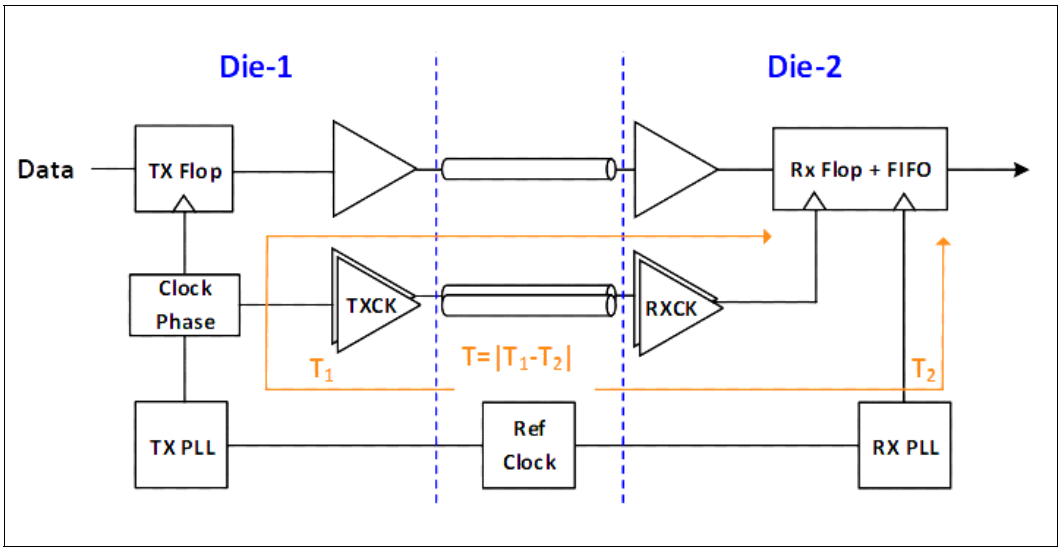
5.1 Interoperability

5.1.1 Data rates

A device must support 4 GT/s and all the data rates data rates between 4 GT/s and the highest supported data rate. For example, a device supporting 16 GT/s must also support 4, 8, and 12 GT/s Data rates.

Spread-Spectrum Clocking (SSC) is permitted. Common reference clock (REFCLK) is required between a UCIe Link Transmitter and the corresponding UCIe Link partner's Receiver with a transport delay difference less than 5 ns to limit the FIFO depth and minimize the latency impact. For the retimer use case, the "Local UCIe Link connection" shall use common REFCLK, while the "Off-Package Link connection" is not required to use or share the common REFCLK. Figure 5-1 shows the transport delay difference and is symmetrical for both directions of a Die's UCIe Link connection. The transport delay represents the delay difference between the Transmitter data to the Receiver data latch and the clock as seen at the receiver's FIFO output data latch. See Section 5.1.2 for REFCLK details.

Figure 5-1. Example Common Reference Clock



IMPLEMENTATION NOTE

In typical implementations, the LCLK for UCIe Link Transmitter and LCLK for the corresponding link partner Receiver, are both generated from the common reference clock. In the example implementation of Figure 5-1, the LCLK for Transmitter in Die-1 can be generated from TX PLL and the LCLK for Receiver in Die-2 can be generated from the RX PLL

5.1.2 Reference Clock (REFCLK)

Common reference clock (REFCLK) uses a single source that is distributed to both the Transmitter and the Receiver. The clock can be supplied from a package pin or be forwarded by another die on the package. In either case, the reference clock used by both dies on the same link must be from the same clock source. Although other reference clocks are possible, it is recommended that every chiplet use a 100-MHz reference clock, including both dies having different reference clock values from the same clock source. Table 5-1 lists the permitted reference clock frequency range. The minimum and maximum frequencies listed in the table indicate the limits, and do not indicate a requirement to support the entire frequency range. It is required for implementations to generate precise I/O clock frequencies for the supported data rates that use the reference clock. Note that this is possible if the I/O clock frequency is an exact integer multiple of the reference clock frequency (if different from 100 MHz). The reference clock may be disabled in low-power states (such as is done in other Standards and Specifications).

Table 5-1. REFCLK Frequency PPMs and SSC PPMs (Sheet 1 of 2)

Symbol	Description	Limits			Unit	Notes
		Min	Rec	Max		
F_{REFCLK}	REFCLK Frequency	25	100	200	MHz	
$F_{REFCLKDEVIATION}$	REFCLK Frequency Deviation	-300		300	ppm	Maximum deviation allowed from ideal target frequency.
F_{SSC}	SSC Modulation Frequency	30		33	kHz	

Table 5-1. REFCLK Frequency PPMs and SSC PPMs (Sheet 2 of 2)

Symbol	Description	Limits			Unit	Notes
		Min	Rec	Max		
$T_{SSC-FREQ-DEVIATION}$	SSC Deviation	-0.5		0	%	Tracks for different frequencies.
$T_{TRANSPORT-DELAY}$	Tx-to-Rx Transport Delay			5	ns	
$T_{SSC-MAX-FREQ-SLEW}$	SSC df/dt			1250	ppm/us	

5.2 Overview

5.2.1 Interface Overview

High-level block diagrams of UCIe PHY are shown in Figure 5-2 and Figure 5-3. The UCIe physical interface consists of building blocks called Modules. A Module that uses advanced packaging technology (e.g., EMIB, CoWoS) called "Advanced Package Module" consists of a pair of clocks, 64 or 32 single-ended data Lanes for x64 or x32 Advanced Package Module, respectively, a data valid Lane each direction (transmit and receive) and a Track Lane. There is a low-speed sideband bus for initialization, Link training, and configuration reads/writes. The sideband consists of a single-ended sideband data Lane and single-ended sideband clock Lane in both directions (transmit and receive).

The x16 or x8 "Standard Package Module" uses a traditional Standard packaging with larger pitch. A Standard Package Module consists of a pair of clocks, 16 or 8 single-ended data Lanes, a data valid Lane and Track Lane in each direction (transmit and receive). There is a low-speed sideband bus for initialization, Link training, and configuration reads/writes. The sideband consists of a single-ended sideband data Lane and single-ended sideband clock Lane in both directions (transmit and receive).

For some applications, multiple modules (2 or 4) can be aggregated to deliver additional bandwidth.

To avoid reliability issues, it is recommended to limit the Transmitter output high (V_{OH}) to a maximum of 100 mV above the receiving chiplet's Receiver front-end circuit power supply rail. An over-stress protection circuit may be implemented in the Receiver when V_{OH} is more than 100 mV above the Receiver power supply rail.

Figure 5-2. x64 or x32 Advanced Package Module

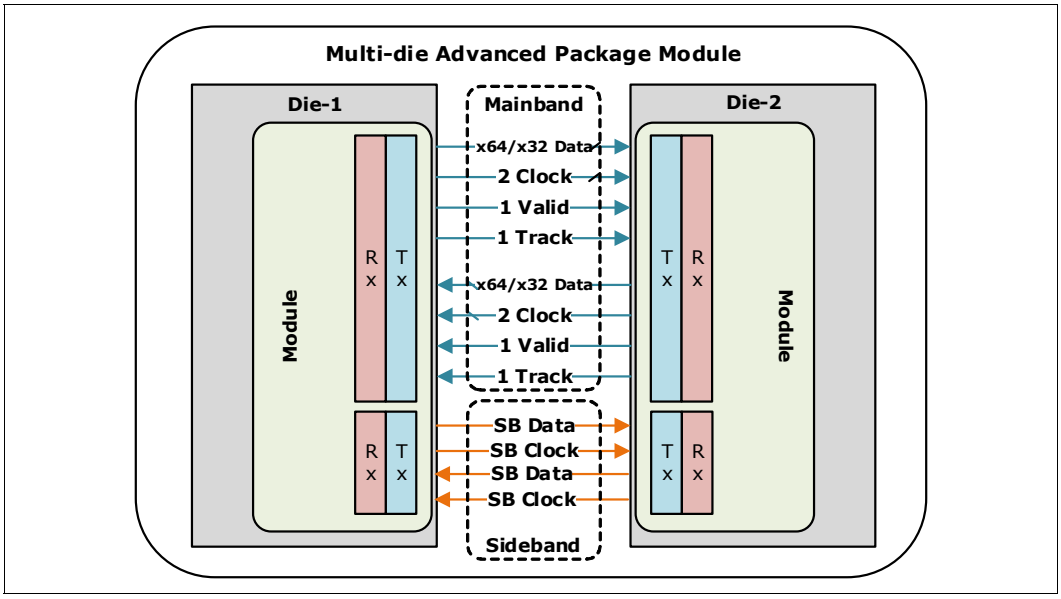
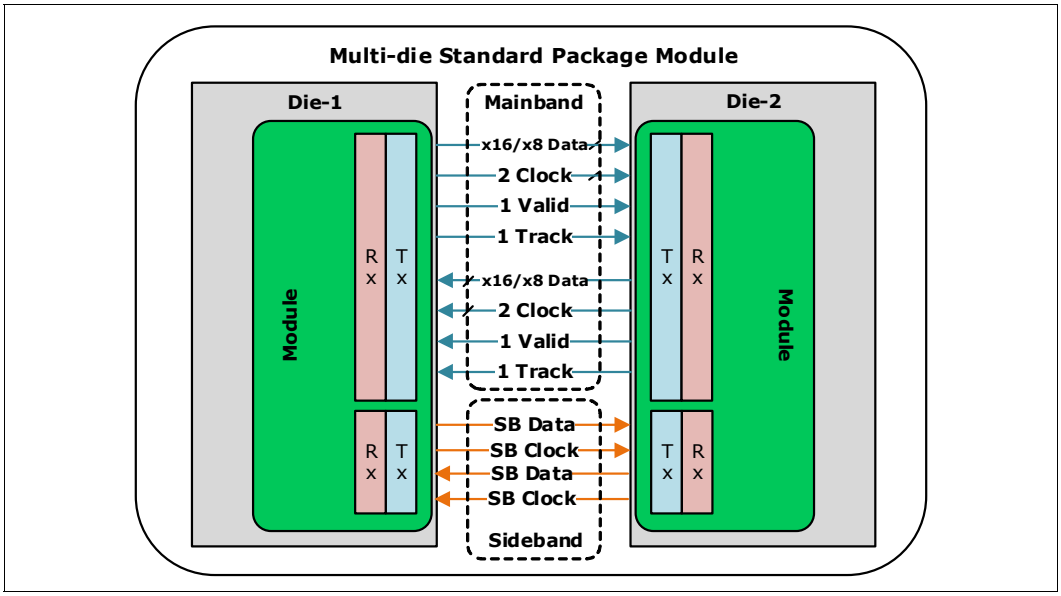


Figure 5-3. x16 or x8 Standard Package Module



5.2.2 Electrical summary

Table 5-2 defines the PHY electrical characteristics of a UCIe device.

Table 5-2. Electrical summary

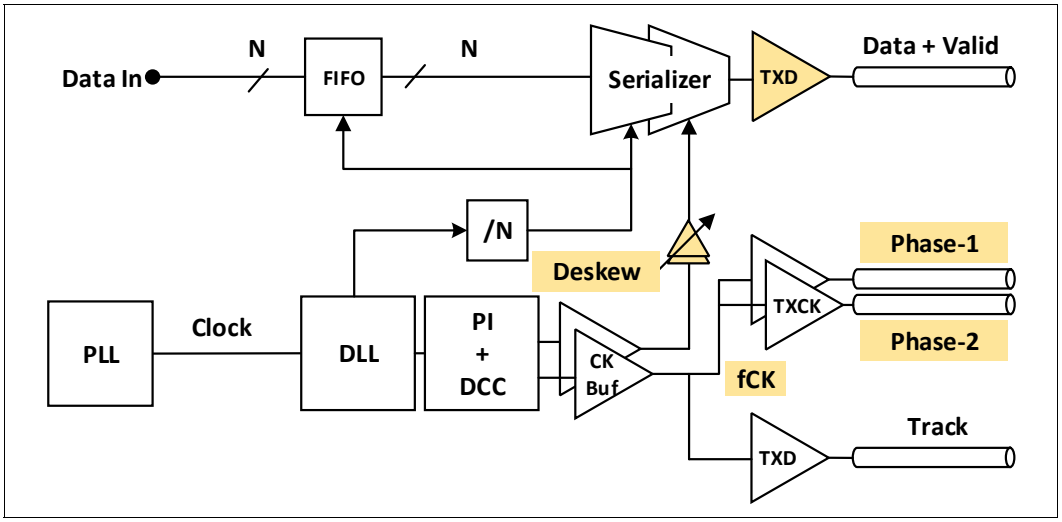
Parameter	Advanced Package (x64)			Standard Package			
Data Width (per module)	64	64	64	16	16	16	16
Data Rate (GT/s)	4/8/12	16	24/32	4-16	4/8/12	16	24/32
Power Efficiency Target (pJ/b)	See Table 1-4						
Latency Target (TX+RX) (UI)[a] (Target upper bound)	12	12	16	12	12	12	16
Idle Exit/Entry Latency (ns) (target upper bound)	0.5	1	1	0.5	0.5	1	1
Idle Power (% of peak power) (target upper bound)	15	15	15	15	15	15	15
Channel Reach (mm)	2	2	2	2-10	25	25	25
Die Edge Bandwidth Density (GB/s/mm)[b]	See Table 1-4						
Bandwidth area density ($GB/s/mm^2$)	158/316/473	631	710/947	21-85	21/42/64	85	109/145
PHY dimension width per module (um)[c]	388.8	388.8	388.8	571.5[d]	571.5[d]	571.5[d]	571.5[d]
PHY dimension Depth (um)[e]	1043	1043		1320	1320	1320	1540
ESD[f]	30V CDM (Anticipating going to 5-10V in Future.)						

a. Electrical PHY latency target. For overall latency target, see Table 1-4.
b. See Table 1-4.
c. For compatibility, PHY dimension width must match spec for Advanced Package. Tolerance of PHY dimension width for Standard Package can be higher because there is more routing flexibility. For best channel performance, it's recommended for width to be close to spec.
d. Standard Package PHY dimension width is the effective width of one (x16) module based on x32 interface (see Figure 5-42 and Figure 5-43).
e. PHY dimension depth is an informative parameter and depends on bump pitch. Number in the table is based on 45-um bump pitch for 10-column x64 Advanced Package and 100-um bump pitch for Standard Package. See Section 5.7.2 for informative values of PHY dimension depth for combinations of the x64 and x32 Advanced Package modules in 10-column, 16-column, and 8-column bump matrix construction.
f. Reference (Industry Council on ESD Target Levels): White Paper 2: A Case for Lowering Component-level CDM ESD Specifications and Requirements.

5.3 Transmitter Specification

The Transmitter topology is shown in Figure 5-4. Each data module consists of N single-ended data Transmitters plus a Valid signal. N is 68 (64 Data + 4 Redundant Data) for a x64 Advanced Package Module. N is 34 (32 Data + 2 Redundant Data) for a x32 Advanced Package Module. N is 16 for a x16 Standard Package Module. N is 8 for a x8 Standard Package Module. There is a pair of Transmitters for clocking and a Track signal in each module. The clock rates and phases are discussed in detail in Section 5.5.

Figure 5-4. Transmitter



The Valid signal is used to gate the clock distribution to all data Lanes to enable fast idle exit and entry. The signal also serves the purpose of Valid framing, see Section 4.1.2 for details. The Transmitter implementation for Valid signal is expected to be the same as for regular Data.

The Track signal can be used for PHY to compensate for slow-changing variables such as voltage or temperature. Track is a unidirectional signal similar to a data bit. The UCIe Module sends a clock pattern (1010…) aligned with Phase-1 of the forwarded clock signal on its Track Transmitter when requested over the sideband by the UCIe Module Partner for its Track Receiver. See Section 4.6 for more details on Runtime Recalibration steps and Section 5.5.1 for Track usage.

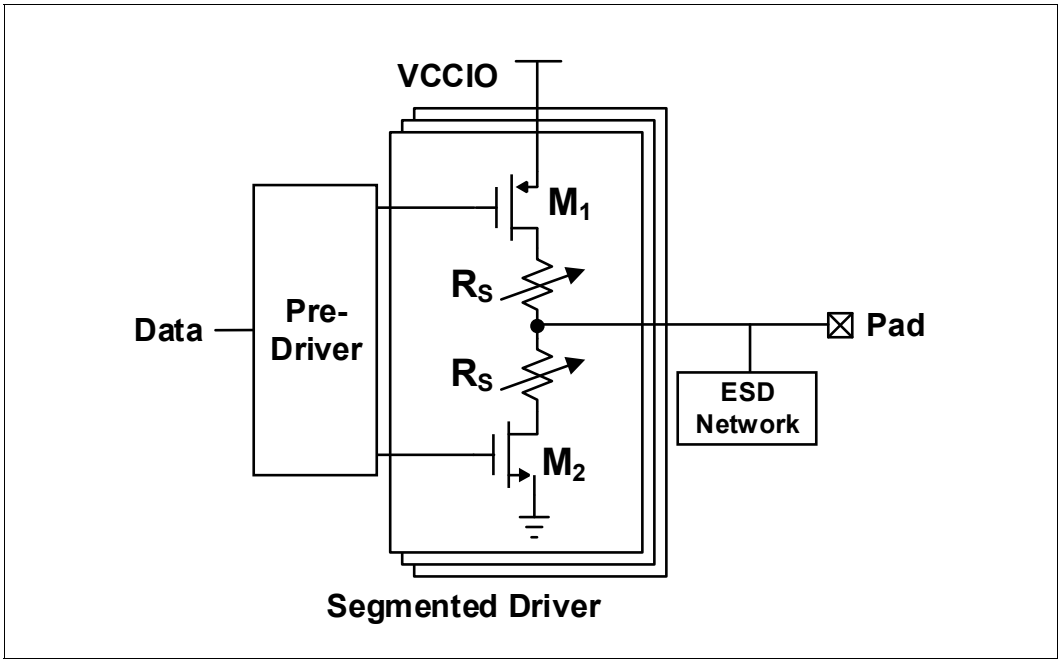
5.3.1 Driver Topology

The Transmitter is optimized for simplicity and low power operation. An example of a low power Transmitter driver is shown in Figure 5-5. Separate pull-up and pull-down network strengths are permitted to achieve optimal performance across different channel configurations.

A control loop or training is recommended to adjust output impedance to compensate for the process, voltage and temperature variations. Control loop and training are implementation specific and beyond the scope of this specification. In low power states, the implementation must be capable of tri-stating the output.

It is recommended to optimize the ESD network to minimize pad capacitance. Inductive peaking technique such as T-coil may be needed at higher data rates.

Figure 5-5. Transmitter driver example circuit



5.3.2 Transmitter Electrical parameters

Table 5-3 defines the Transmitter electrical parameters.

Table 5-3. Transmitter Electrical Parameters (Sheet 1 of 2)

Parameter	Min	Typ	Max	Unit
Data Lane TX Swing[a]	0.4			V
Fwd Clock Tx Swing (single ended)	0.4			V
Incoming Clock Rise/Fall time[b]	0.1	0.22	0.25	UI
Incoming Differential Clock Overlap[b]	-	-	30	mUI
Incoming Data Rise/Fall time[b]	-	0.35	-	UI
Driver Pull-up/Pull-down Impedance for Advanced Package[c]	22	25	28	Ohms
Impedance Step Size for Advanced Package[d]			0.5	Ohms
Driver Pull-up/Pull-down Impedance for Standard Package[e]	27	30	33	Ohms
Impedance Step Size for Standard Package[d]	-	-	0.5	Ohms
1-UI Total Jitter[f]	-	-	96/113	mUI pk-pk
1-UI Deterministic Jitter (Dual Dirac)[g]	-	-	48	mUI pk-pk
Tx Data/clock Differential Jitter (Divergent Path)[h]			60	mUI pk-pk
Duty Cycle Error[i]	-0.02	-	0.02	UI
Lane-to-Lane Skew Correction Range (up to 16 GT/s)[j]	-0.1	-	0.1	UI
Lane-to-Lane Skew Correction Range (up to 32 GT/s)[j]	-0.15	-	0.15	UI
Lane-to-Lane Skew Correction Range (up to 16 GT/s)[k]	-0.14	-	0.14	UI
Lane-to-Lane Skew Correction Range (up to 32 GT/s)[k]	-0.22	-	0.22	UI
Lane-to-Lane Skew[i]	-0.02	-	0.02	UI

Table 5-3. Transmitter Electrical Parameters (Sheet 2 of 2)

Parameter	Min	Typ	Max	Unit
Clock to Mean Data Training Accuracy[l]	-0.07	-	0.07	UI
Phase Adjustment Step[m]	-	-	16	mUI
TX Pad Capacitance (for all speeds)[n]	-	-	250	fF
TX Pad Capacitance (8 GT/s capable design)[14]	-	-	300	fF
TX Pad Capacitance (16 GT/s capable design)[o]	-	-	200	fF
TX Pad Capacitance (32 GT/s capable design)[o]	-	-	125	fF

a. For recommended maximum Transmitter voltage, see Section 1.5.
b. Expected input (informative). Measured 20% to 80%. Differential clock overlap is deviation from the ideal differential phase (180 degrees apart).
c. Driver pull-up/down impedance is calibrated at midpoint of Transmitter signal swing.
d. Impedance step size is an informative parameter and can be implementation specific to meet Driver pull-up/pull-down impedance.
e. Driver pull-up/pull-down impedance is calibrated at midpoint of Transmitter signal swing (with nominal Rx termination when applicable).
f. At BER 1E-15/1E-27.
g. Data dependent jitter excluding Duty Cycle Error.
h. Includes absolute random jitter and untracked deterministic jitter of the divergent path due to delay mismatch (in the matched architecture).
i. Post correction.
j. Advanced Package.
k. Standard Package.
l. Includes static and tracking error.
m. Informative parameter. Phase adjustment step size must be chosen to meet other timing parameters, including Clock-to-Mean Data Training Accuracy, Lane-to-Lane skew, and Duty cycle error (if applicable).
n. Effective pad capacitance Advanced Package.
o. Effective pad capacitance Standard Package.

5.3.3 24 GT/s and 32 GT/s Transmitter Equalization

Transmitter equalization is recommended for 16 GT/s and must be supported at 24 GT/s and 32 GT/s data rates to mitigate the channel ISI impact. Tx equalization is de-emphasis only for all applicable Data rates.

Tx equalization coefficients for 24 GT/s and 32 GT/s are based on the FIR filter shown in Figure 5-6. Equalization coefficient is subject to maximum unity swing constraint.

The Transmitter must support the equalization settings shown in Table 5-4. Determination of de-emphasis setting is based on initial configuration or training sequence, where the value with larger eye opening will be selected.

Figure 5-6. Transmitter de-emphasis

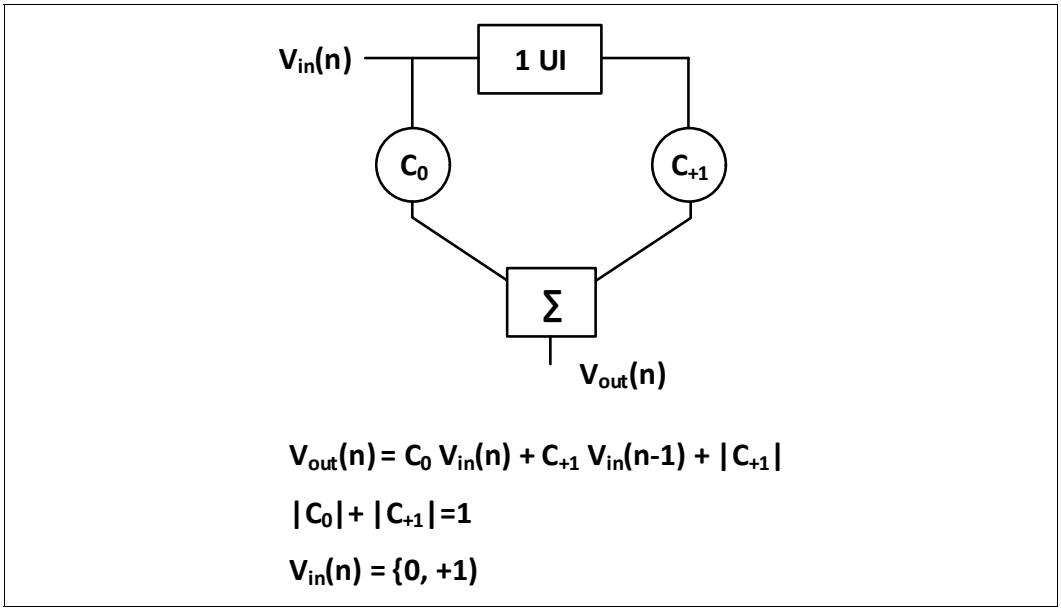


Figure 5-7. Transmitter de-emphasis waveform

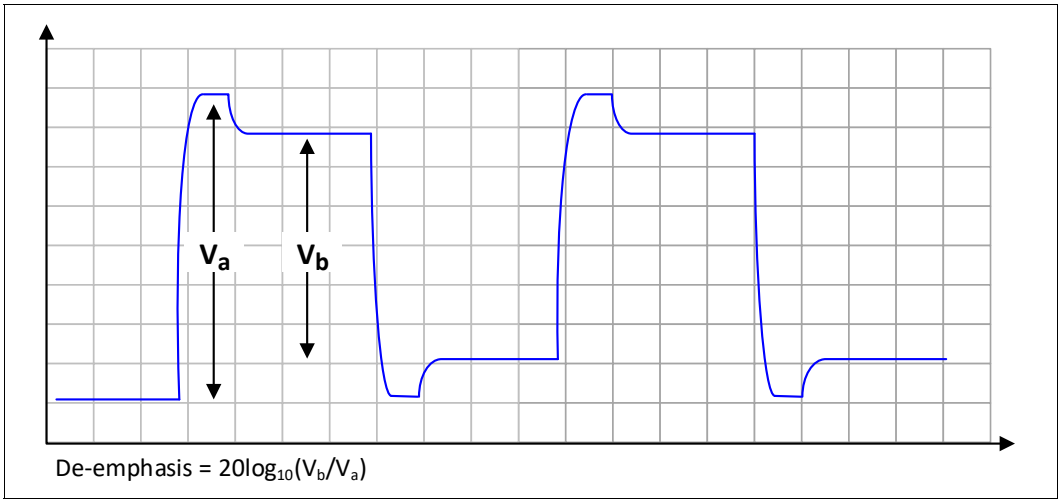


Table 5-4. Transmitter de-emphasis values

Setting	De-emphasis	Accuracy	C_{+1}	V_b/V_a
1	0.0 dB	-	0.000	1.000
2	-2.2 dB	+/- 0.5 dB	-0.112	0.776

5.4 Receiver Specification

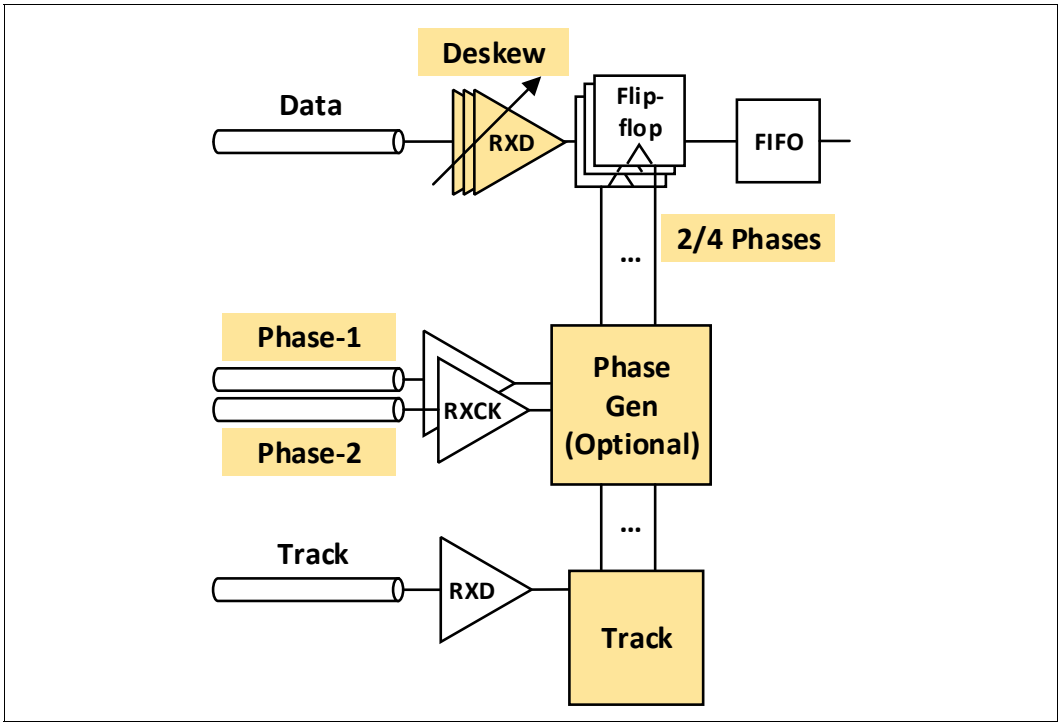
The Receiver topology is illustrated in Figure 5-8. Each Module (Advanced Package and Standard Package) consists of clocks Receivers, data Receivers, and Track Receiver.

The received clock is used to sample the incoming data. The Receiver must match the delays between the clock path and the data/valid path to the sampler. This is to minimize the impact of power supply noise induced jitter. The data Receivers may be implemented as 2-way or 4-way interleaved. For 4-way interleaved implementation the Receiver needs to generate required phases internally from the two phase of the forwarded clock. This may require duty cycle correction capability on the Receiver. The supported forwarded clock frequencies and phases are described in Section 5.5.

At higher data rates, deskew capability may be needed in the receiver to achieve the matching requirements between the data Lanes. Receiver Deskew, when applicable, can be performed during mainband training. More details are provided in Section 4.5.

The UCIe Module, upon requesting the Track signal, receives a clock pattern (1010…) aligned with Phase-1 of the forwarded clock signal on its Track Receiver from the UCIe Module Partner's Track Transmitter and may use the Track signal to track the impact of slow varying voltage and temperature changes on sampling phase.

Figure 5-8. Receiver topology



5.4.1 Receiver Electrical Parameters

The specified Receiver electrical parameters are shown in Table 5-5.

Table 5-5. Receiver Electrical parameters

Parameter	Min	Typ	Max	Unit
RX Input Impedance[a]	45	50	55	Ohms
Impedance Step Size[a]	-	-	1	Ohms
Data/Clock Total Differential Jitter[b c]	-	-	60	mUI pk-pk
Lane-to-Lane skew (up to 16 GT/s)[d]	-0.07	-	0.07	UI
Lane-to Lane skew (> 16 GT/s)[d]	-0.12	-	0.12	UI
Phase error[e] (Including Duty cycle error and in-phase quadrature mismatch)	-0.04	-	0.04	UI
Per-Lane deskew adjustment step[f]	-	-	16	mUI
Output Rise Time[g]	-	-	0.1	UI
Output Fall Time[g]	-	-	0.1	UI
RX Pad Capacitance[h]	-	-	200	fF
RX Pad Capacitance (up to 8 GT/s)[a]	-	-	300	fF
RX Pad Capacitance (up to 16 GT/s)[a i]	-	-	200	fF
RX Pad Capacitance (24 and 32 GT/s)[a i]	-	-	125	fF
Rx Voltage sensitivity	-	-	40	mV

a. Standard Package mode with termination. Impedance step size is an informative parameter and can be implementation specific to meet Rx Input Impedance.
b. Based on matched architecture.
c. Includes absolute random jitter and untracked deterministic jitter of the divergent path due to delay mismatch (in the matched architecture).
d. Require Rx per-Lane deskew if limit is exceeded.
e. Residual error post training and correction.
f. When applicable (informative).
g. Expected output (informative). Measured 20% to 80%.
h. Advanced Package.
i. Effective Pad capacitance.

5.4.2 Rx Termination

Rx termination is applicable only to Standard Package modules. All Receivers on Advanced Package modules must be unterminated.

Receiver termination on Standard Package is data rate and channel dependent. Table 5-6 shows the maximum data rate and channel reach combinations for which the Receivers in Standard Package Modules are recommended to remain unterminated for a minimally compliant Transmitter. Figure 5-9 shows an alternate representation of termination requirement. The area below the curve in Figure 5-9 shows the speed and channel-reach combinations for which the Receivers in Standard Package Modules are recommended to remain unterminated. Termination is required for all other combinations. Receivers must be ground-terminated when applicable, as shown in Figure 5-10.

Table 5-6. Maximum channel reach for unterminated Receiver (Tx Swing = 0.4 V)

Data Rate (GT/s)	Channel Reach (mm)
12	3
8	5
4	10

Figure 5-9. Receiver Termination Map for Table 5-6 (Tx Swing = 0.4 V)

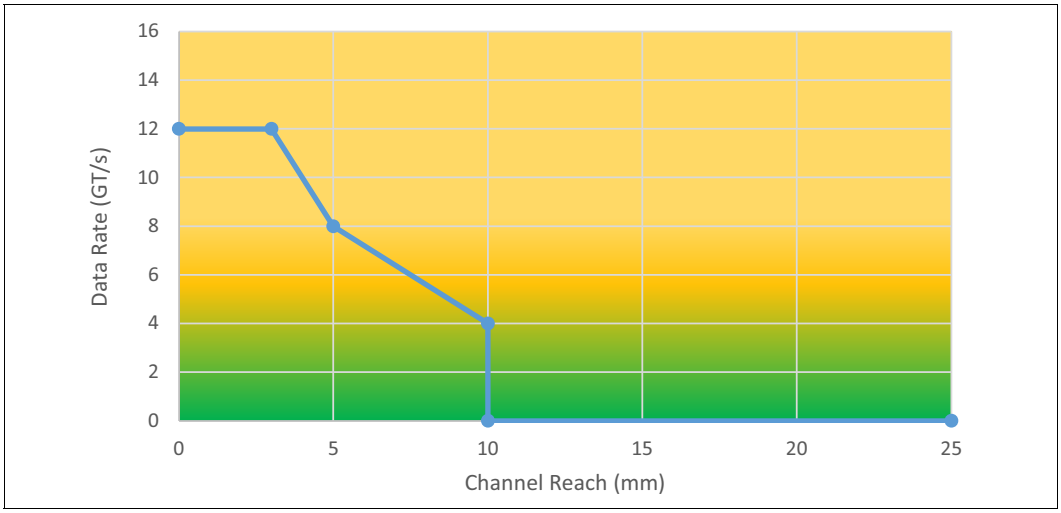
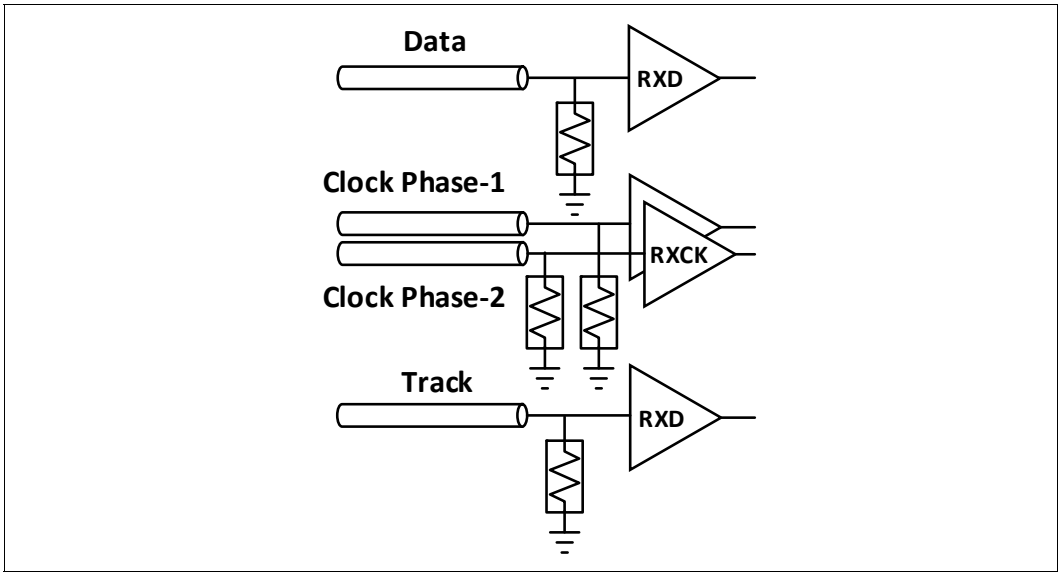


Figure 5-10. Receiver termination



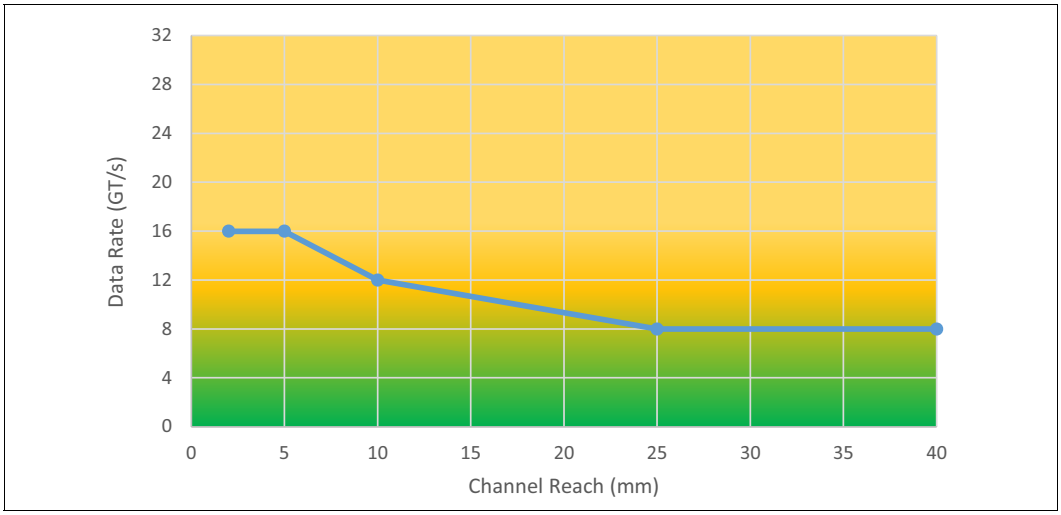
For higher Transmitter swing, unterminated Receiver can be extended to longer channel and high data rate. Table 5-7 shows the maximum data rate and channel reach combinations for Transmitter swing and 0.85 V (maximum recommended swing). Figure 5-11 shows an alternate representation of termination requirement. The area below the curve in Figure 5-11 shows the speed and channel reach

combinations for which the Receivers in Standard Package Modules are recommended to remain unterminated.

Table 5-7. Maximum Channel reach for unterminated Receiver (TX swing = 0.85V)

Data Rate (GT/s)	Channel Reach (mm)
16	5
12	10
8 and below	All supported Lengths

Figure 5-11. Receiver termination map for Table 5-7 (TX Swing = 0.85 V)



IMPLEMENTATION NOTE

When the Transmitter is tri-stated and the Receiver is not required to be enabled (e.g., SBINIT, and some MBINIT states):

- Disabled Receivers must be tolerant of a floating input pad
- Receivers are permitted to enable weak-termination directly on the input pad to prevent crowbar current in the receiver and to lower noise sensitivity at the receiver trip point

When the Transmitter is tri-stated and the Receiver is required to be enabled (e.g., REPAIRCLK and REPAIRVAL states for Advanced Package):

- Enabled Receivers for (CLKP, CLKN, CLKRD, TRK, VLD, VLDRD) must be tolerant of a floating input signal on the pad
- Receivers are permitted to enable weak-termination directly on the input pad to prevent crowbar current in the receiver and to lower noise sensitivity at the receiver trip point

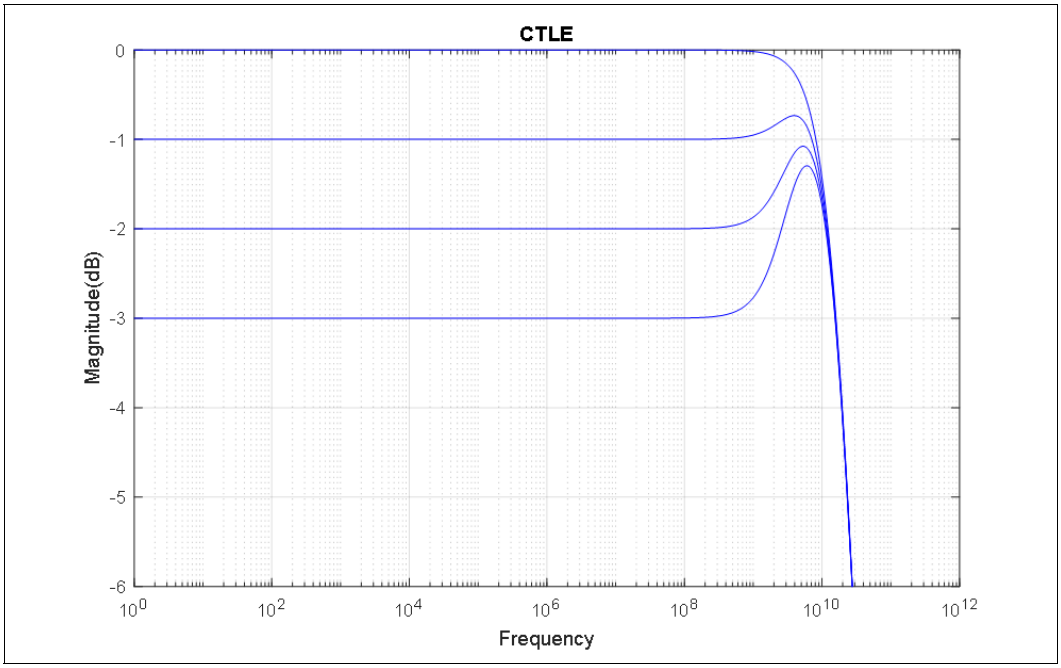
5.4.3 24 and 32 GT/s Receiver Equalization

Receiver equalization may be implemented at 24 GT/s and 32 GT/s data rates. This enables Link operation even when TX equalization is not available. Implementation can be CTLE, inductive peaking, 1-tap DFE, or others. Expected RX equalization capability is equivalent of 1st order CTLE. Example transfer function curves of a first order CTLE are shown in Figure 5-12 and the corresponding equation is shown below:

$$H(s) = \omega_{p2}\left(\frac{s + A_{DC}\omega_{p1}}{(s + \omega_{p1})(s + \omega_{p2})}\right)$$

where, ω_{p2} = 2π*DataRate, ω_{p1} = 2π*DataRate /4, and A_{DC} is the DC gain.

Figure 5-12. Example CTLE



5.5 Clocking

Figure 5-13 shows the forwarded clocking architecture. Each module supports a two-phase forwarded clock. It is critical to maintain matching between all data Lanes and valid signal within the module. The Receiver must provide matched delays between the Receiver clock distribution and Data/Valid Receiver path. This is to minimize the impact of power supply noise-induced jitter on Link performance. Phase adjustment is performed on the Transmitter as shown in Figure 5-13. Link training is required to set the position of phase adjustment to maximize the Link margin.

At higher data rates, Receiver eye margins may be small and any skew between the data Lanes (including Valid) may further degrade Link performance. Per-Lane deskew must be supported on the Transmitter at high data rates.

This specification supports quarter-rate clock frequencies at data rates (24 GT/s and 32 GT/s). The forwarded clock Transmitter must support quadrature phases in addition to differential clock at these data rates (to enable either quarter-rate or half-rate Receiver implementations). Table 5-8 shows the clock frequencies and phases that must be supported at different data rates. Forwarded Clock Phase is negotiated during Link Initialization and Training (see Section 4.5.3.3.1). At 24 GT/s and 32 GT/s,

Receiver has the options to support differential clock or quadrature clock. The capability register is defined in Table 9-47, and advertised at the beginning of link negotiation. Note that to achieve interoperability with designs of lower max data rate, differential clock must always be used at 16 GT/s and below, independent of the choice at 24 GT/s and 32 GT/s.

5.5.1 Track

Track signal can be used to perform Runtime Recalibration to adjust the Receiver clock path against slow varying voltage, temperature and transistor aging conditions.

When requested by the UCIe Module, the UCIe Module Partner sends a clock pattern (1010…) aligned with Phase-1 of the forwarded clock on its Track Transmitter, as shown in Figure 5-13.

Figure 5-13. Clocking architecture

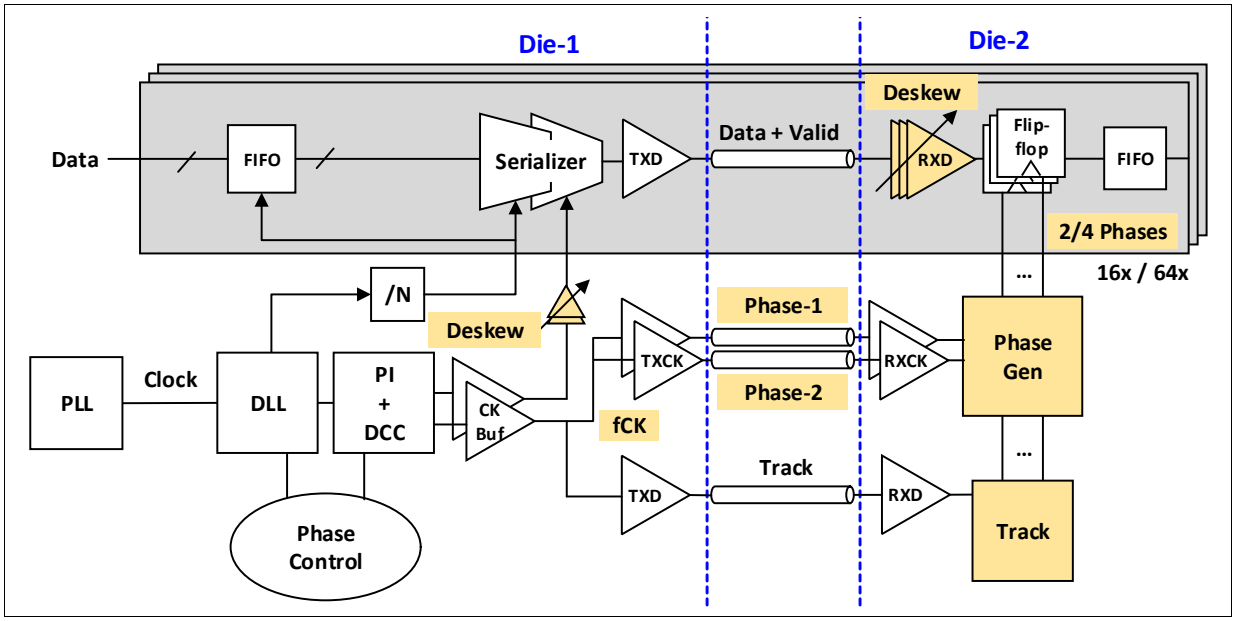


Table 5-8. Forwarded clock frequency and phase

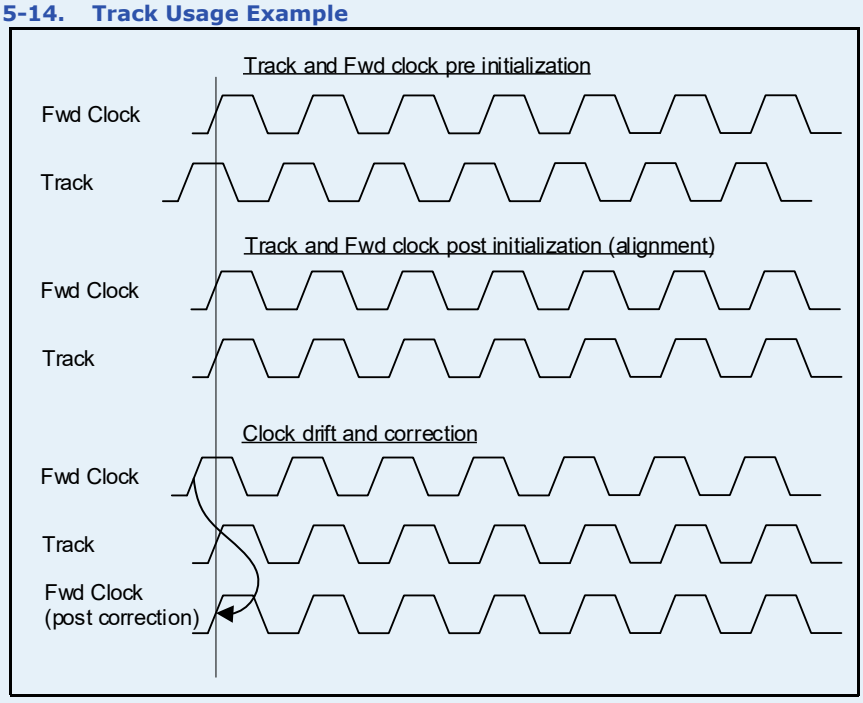
Data rate (GT/s)	Clock freq. (fCK) (GHz)	Phase-1	Phase-2	Deskew (Req/Opt)
32	16	90	270	Required
	8	45	135	Required
24	12	90	270	Required
	6	45	135	Required
16	8	90	270	Required
12	6	90	270	Required
8	4	90	270	Optional
4	2	90	270	Optional

IMPLEMENTATION NOTE

This implementation note provides an example usage for Track signal to calibrate out slow varying temperature- and voltage-related delay drift between Data and Clock on the Receiver.

Track uses the same type of Tx driver and Rx receiver as Data (see Figure 5-13). A clock pattern aligned with Phase-1 of the forwarded clock is sent from Track Transmitter and received on the Track Receiver. Any initial skew can be calibrated out during initialization and training (MBTRAIN.RXCLKCAL) on the Receiver side. During run-time, any drift between Data and the forwarded clock can be detected. One method for detecting the drift is to sample Track with the forwarded clock. An implementation-specific number of samples can be collected, averaged if needed, and used for drift detection. This drift can then be corrected on the forwarded clock (if needed).

Figure 5-14. Track Usage Example



5.6 Supply noise and clock skew

I/O Vcc noise and the clock skew between data modules shall be within the range specified in Table 5-9.

Table 5-9. I/O Noise and Clock Skew

Parameter	Min	Nom	Max	Unit
I/O Vcc noise for 4 GT/s and 8 GT/s[a]	-	-	80	mVpp
I/O Vcc noise for 12 GT/s[a]	-	-	50	mVpp
I/O Vcc noise for 16 GT/s	-	-	40	mVpp
I/O Vcc noise for 24 GT/s and 32 GT/s[a]	-	-	30	mVpp
Module to module clock skew[b]	-	-	60	ps

a. I/O VCC noise includes all noise at the I/O supply bumps relative to VSS bumps. This noise includes all DC and AC fluctuations at all applicable frequencies.
b. Applies only to multi-module instantiations.

IMPLEMENTATION NOTE

Due to different micro bump max current capacity and power delivery requirements, PHY in Advanced Package may have TX providing I/O power supply to RX circuits.

Due to low current draw, sideband supply voltage is strongly recommended to be on an always-on power domain.

5.7 Ball-out and Channel Specification

UCIe interconnect channel needs to meet the requirement of minimum rectangular eye open as specified in Table 5-10 under channel compliance simulation conditions with noiseless and jitter-less behavioral TX and RX models.

Figure 5-15. Example Eye diagram

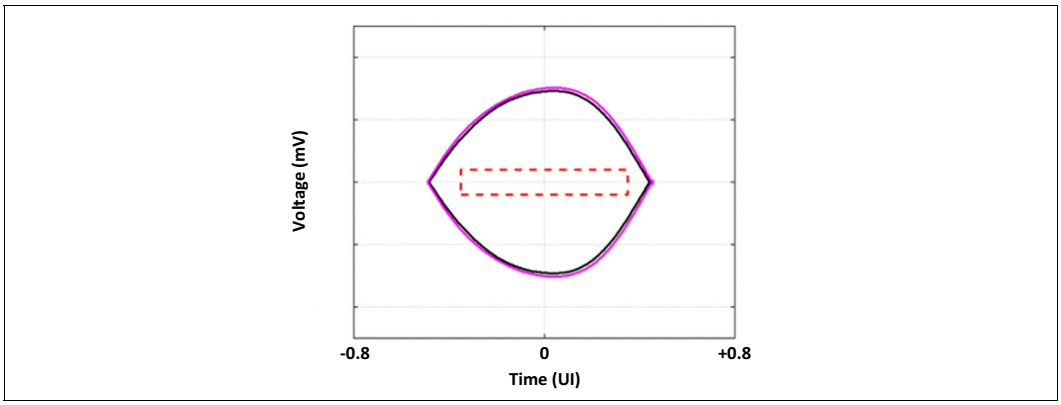


Table 5-10. Eye requirements

Data Rate (GT/s)	Eye Height (mV)	Eye width (UI)
4, 8, 12, 16[a] [c]	40	0.75
24, 32[a] [b] [c]	40	0.65

a. Rectangular mask.
b. With equalization enabled.
c. Based on minimum Tx swing specification.

IMPLEMENTATION NOTE

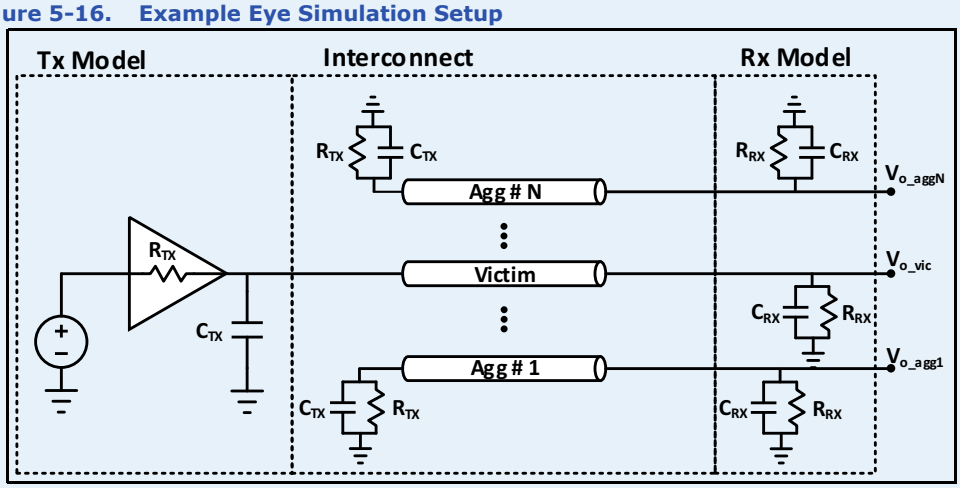
Figure 5-16 shows an example circuit setup that can be used to generate the statistical eye diagram shown in Figure 5-15. RTX is the Transmitter impedance and RRX represents the Receiver termination. CTX, CRX represent effective Transmitter and Receiver capacitance, respectively. For crosstalk, the 19-largest aggressors need to be included. Transmitter equalization (TXEQ) is enabled at 24 GT/s and 32 GT/s.

The eye diagram was generated using a two-step process.

1. Generate ISI and XTALK channel step response using circuit setup shown in Figure 5-16.
2. Use the generated channel response in a signal-integrity or channel-simulation tool to generate a statistical eye diagram (see Figure 5-15)

Other equivalent methods may be used, depending on the signal-integrity or channel-simulation tool.

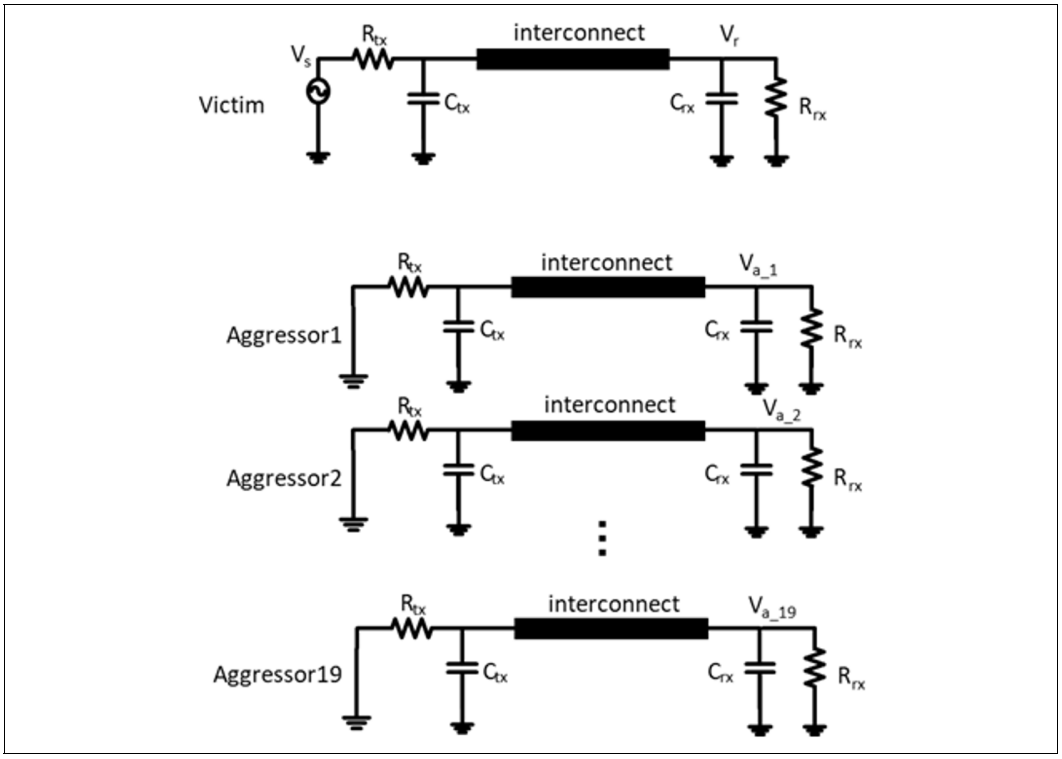
Figure 5-16. Example Eye Simulation Setup



5.7.1 Voltage Transfer Function

Voltage Transfer Function (VTF) based metrics are used to define insertion loss and crosstalk. VTF metrics incorporate both resistive and capacitive components of TX and RX terminations. Figure 5-17 shows the circuit diagram for VTF calculations.

Figure 5-17. Circuit for VTF calculation



VTF loss is defined as the ratio of the Receiver voltage and the Source voltage, as shown in Equation 5-1 and Equation 5-2.

Equation 5-1.

$$L(f) = 20\log 10\left|\frac{V_r(f)}{V_s(f)}\right|$$

Equation 5-2.

$$L(0) = 20\log 10\left(\frac{R_{rx}}{R_{tx}+R_{channel}+R_{rx}}\right)$$

L(f) is the frequency dependent loss and L(0) is the DC loss. For unterminated channel, L(0) is effectively 0.

VTF crosstalk is defined as the power sum of the ratios of the aggressor Receiver voltage to the source voltage. 19 aggressors are included in the calculation. Based on crosstalk reciprocity, VTF crosstalk can be expressed as shown in Equation 5-3.

Equation 5-3.

$$XT(f) = 10\log 10\left(\sum_{i=1}^{19}\left|\frac{V_{ai}(f)}{V_s(f)}\right|^2\right)$$

5.7.2 Advanced Package

Table 5-11. Channel Characteristics

Data Rate	4-16 GT/s	24, 32 GT/s
VTF Loss (dB)	$L(f_N) > -3$	$L(f_N) > -5$
VTF Crosstalk (dB)[a]	$XT(f_N) < 1.5\ L(f_N) - 21.5$ and $XT(f_N) < -23$	$XT(f_N) < 1.5\ L(f_N) - 19$ and $XT(f_N) < -24$

a. Based on Voltage Transfer Function Method (Tx: 25 ohm / 0.25 pF; Rx: 0.2 pF).

f_N is the Nyquist frequency. The equations in the table form a segmented line in the loss-crosstalk coordinate plane, defining the pass/fail region.

Table 5-12. x64 Advanced Package Module Signal List (Sheet 1 of 2)[a]

Signal Name	Count	Description
Data		
TXDATA[63:0]	64	Transmit Data
TXVLD	1	Transmit Data Valid; Enables clocking in corresponding module
TXTRK	1	Transmit Track signal
TXCKP	1	Transmit Clock Phase-1
TXCKN	1	Transmit Clock Phase-2
TXCKRD	1	Redundant for Clock and Track Lane repair
TXDATARD[3:0]	4	Redundant for Data Lane repair
TXVLDRD	1	Redundant for Valid
RXDATA[63:0]	64	Receive Data
RXVLD	1	Receive Data Valid; Enables clocking in corresponding module
RXTRK	1	Receive Track.
RXCKP	1	Receive Clock Phase-1
RXCKN	1	Receive Clock Phase-2
RXDATARD[3:0]	4	Redundant for Data Lane repair
RXCKRD	1	Redundant for Clock Lane repair
RXVLDRD	1	Redundant for Valid
Sideband		
TXDATASB	1	Sideband Transmit Data
RXDATASB	1	Sideband Receiver Data
TXCKSB	1	Sideband Transmit Clock
RXCKSB	1	Sideband Receive Clock
TXDATASBRD	1	Redundant Sideband Transmit Data

Table 5-12. x64 Advanced Package Module Signal List (Sheet 2 of 2)[a]

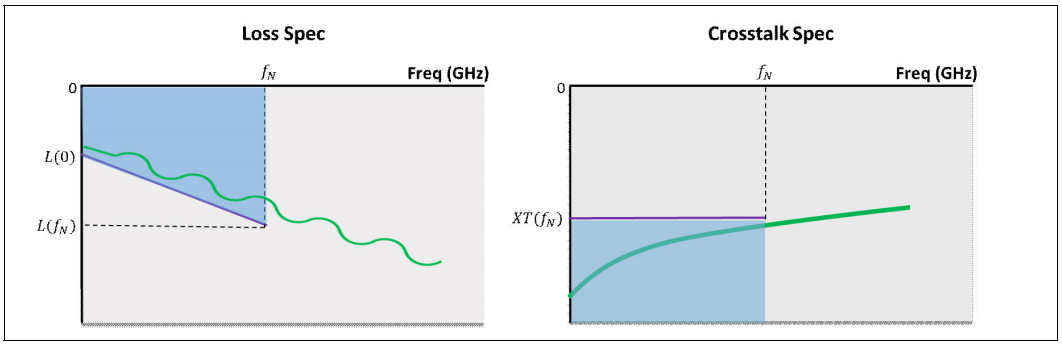
Signal Name	Count	Description
RXDATASBRD	1	Redundant Sideband Receiver Data
TXCKSBRD	1	Redundant Sideband Transmit Clock
RXCKSBRD	1	Redundant Sideband Receive Clock
Power and Voltage		
VSS		Ground Reference
VCCIO		I/O supply
VCCFWDIO		Forwarded power supply from remote Transmitter supply to local Receiver AFE (see Tightly Coupled mode in Section 5.8)
VCCAON		Always on Aux supply (sideband)

a. For x32 Advanced Package module, the **TXDATA[63:32]**, **TXRD[3:2]**, **RXDATA[63:32]**, and **RXRD[3:2]** signals do not apply. All other signals are the same as the x64 Advanced Package Module signals.

5.7.2.1 Loss and Crosstalk Mask

Loss and crosstalk are specified by a mask defined by the $L(f_N)$ and $XT(f_N)$ at Nyquist frequency. It is a linear mask from DC to f_N for loss and flat mask for crosstalk, illustrated by Figure 5-18. Loss from DC to f_N needs to be above the spec line. Crosstalk from DC to f_N needs to be below the spec line. The green line in Figure 5-18 is a representative passing signal.

Figure 5-18. Loss and Crosstalk Mask



5.7.2.2 x64 Advanced Package Module Bump Map

All bump matrices in this section and hereinafter are defined with "dead bug" view which means the viewer is looking directly at the UCIe micro bumps facing up, with the die flipped like a "dead bug" as illustrated in Figure 5-19.

Figure 5-19. Viewer Orientation Looking at the Defined UCIe Bump Matrix

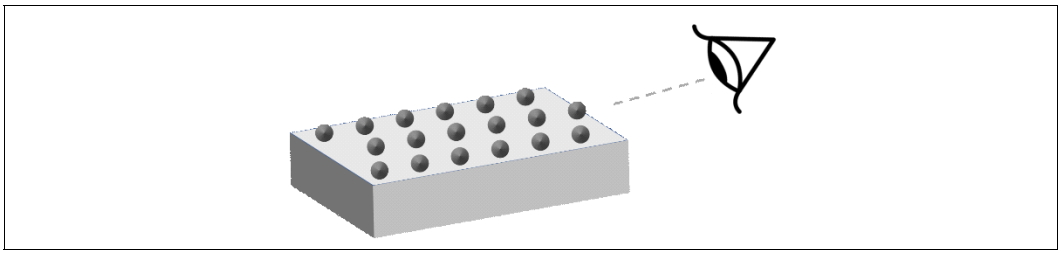


Figure 5-20, Figure 5-21, and Figure 5-22 show the reference bump matrix for the 10-column, 16-column, and 8-column x64 Advanced Package Modules, respectively. The lower left corner of the bump map will be considered "origin" of a bump matrix and the leftmost column is Column 0.

It is strongly recommended to follow the bump matrices provided in Figure 5-20, Figure 5-21, and Figure 5-22 for x64 Advanced Package interfaces.

The 10-column bump matrix is optimal for bump pitch range of 38 to 50 um. To achieve optimal area scaling with different bump pitches, the optional 16-column and 8-column bump matrices are defined for bump ranges of 25 to 37 um and 51 to 55 um, respectively, which will result in optimal Module depth while maintaining Module width of 388.8 um, as shown in Figure 5-21 and Figure 5-22, respectively.

The following rule must be followed for the 10-column x64 Advanced Package bump matrix:

- The signal order within a column must be preserved. For example, Column 0 must contain the signals: **txdataRD0**, **txdata0**, **txdata1**, **txdata2**, **txdata3**, **txdata4**, …, **rxdata59**, **rxdata60**, **rxdata61**, **rxdata62**, **rxdata63**, **rxdataRD3**, and **txdatasbRD**. Similarly, 16-column and 8-column x64 Advanced Packages must preserve the signal order within a column of the respective bump matrices.

It is strongly recommended to follow the supply and **ground** pattern shown in the bump matrices. It must be ensured that sufficient supply and **ground** bumps are provided to meet channel characteristics (FEXT and NEXT) and power-delivery requirements.

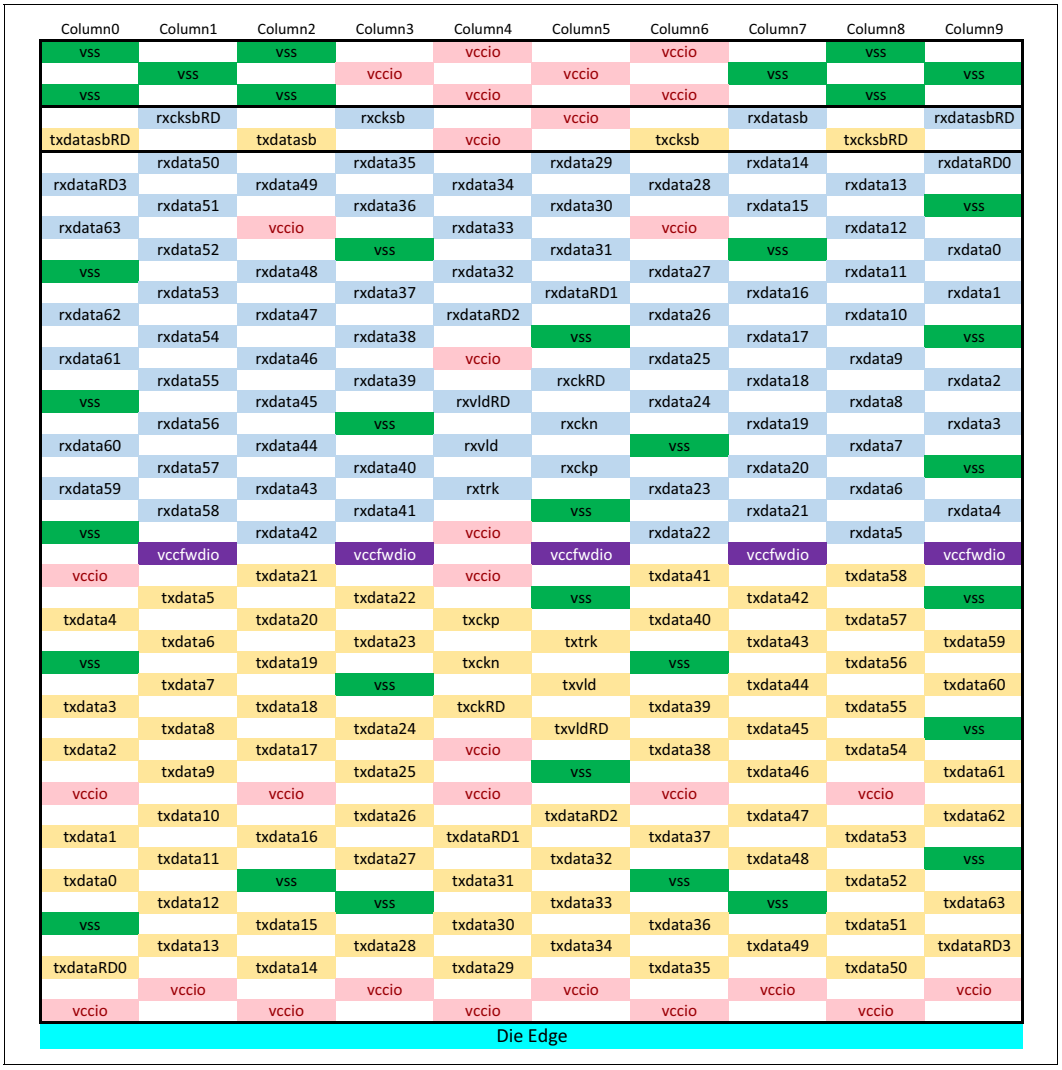
The following rules must be followed when instantiating multiple modules of Advanced Package bump matrix:

- Modules must be stepped in the same orientation and abutted.
- Horizontal or vertical mirroring is not permitted.
- Module stacking is not permitted.

Additionally, in multi-module instantiations it is strongly recommended to add one column of **VSS** bumps on each outside edge of the multi-module instantiation.

Mirror die implementation may necessitate a jog or additional metal layers for proper connectivity.

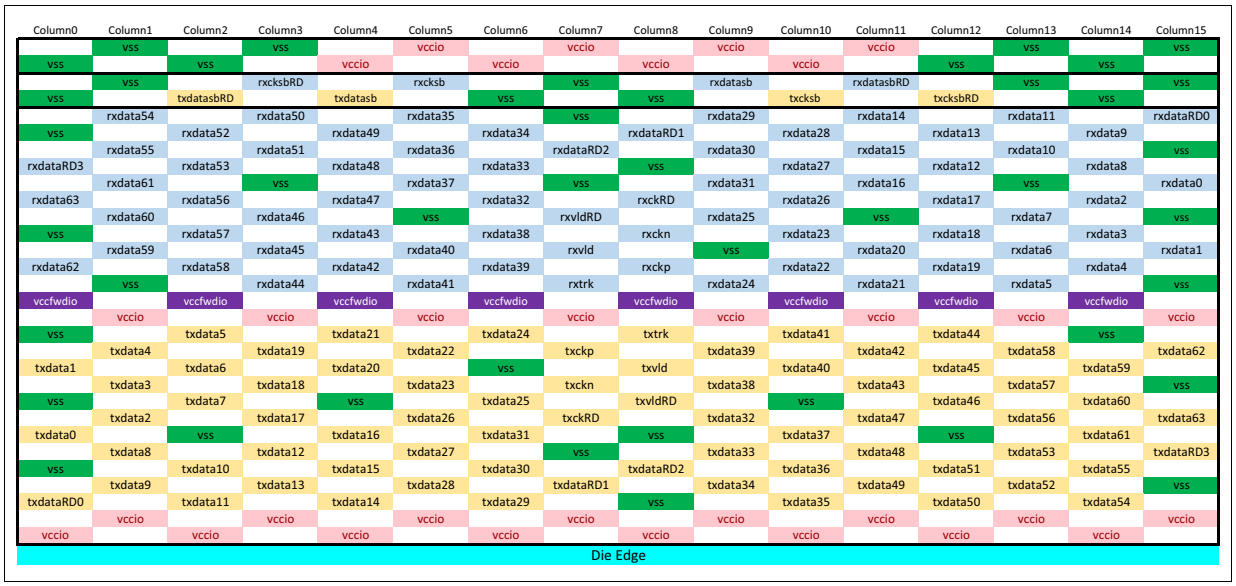
Figure 5-20. 10-column x64 Advanced Package Bump Map



Column0	Column1	Column2	Column3	Column4	Column5	Column6	Column7	Column8	Column9
vss		vss		vccio		vccio		vss	
	vss		vccio		vccio		vss		vss
vss		vss		vccio		vccio		vss	
	rxcksbRD		rxcksb		vccio		rxdatasb		rxdatasbRD
txdatasbRD		txdatasb		vccio		txcksb		txcksbRD	
	rxdata50		rxdata35		rxdata29		rxdata14		rxdataRD0
rxdataRD3		rxdata49		rxdata34		rxdata28		rxdata13	
	rxdata51		rxdata36		rxdata30		rxdata15		vss
rxdata63		vccio		rxdata33		vccio		rxdata12	
	rxdata52		vss		rxdata31		vss		rxdata0
vss		rxdata48		rxdata32		rxdata27		rxdata11	
	rxdata53		rxdata37		rxdataRD1		rxdata16		rxdata1
rxdata62		rxdata47		rxdataRD2		rxdata26		rxdata10	
	rxdata54		rxdata38		vss		rxdata17		vss
rxdata61		rxdata46		vccio		rxdata25		rxdata9	
	rxdata55		rxdata39		rxckRD		rxdata18		rxdata2
vss		rxdata45		rxvldRD		rxdata24		rxdata8	
	rxdata56		vss		rxckn		rxdata19		rxdata3
rxdata60		rxdata44		rxvld		vss		rxdata7	
	rxdata57		rxdata40		rxckp		rxdata20		vss
rxdata59		rxdata43		rxtrk		rxdata23		rxdata6	
	rxdata58		rxdata41		vss		rxdata21		rxdata4
vss		rxdata42		vccio		rxdata22		rxdata5	
	vccfwdio		vccfwdio		vccfwdio		vccfwdio		vccfwdio
vccio		txdata21		vccio		txdata41		txdata58	
	txdata5		txdata22		vss		txdata42		vss
txdata4		txdata20		txckp		txdata40		txdata57	
	txdata6		txdata23		txtrk		txdata43		txdata59
vss		txdata19		txckn		vss		txdata56	
	txdata7		vss		txvld		txdata44		txdata60
txdata3		txdata18		txckRD		txdata39		txdata55	
	txdata8		txdata24		txvldRD		txdata45		vss
txdata2		txdata17		vccio		txdata38		txdata54	
	txdata9		txdata25		vss		txdata46		txdata61
vccio		vccio		vccio		vccio		vccio	
	txdata10		txdata26		txdataRD2		txdata47		txdata62
txdata1		txdata16		txdataRD1		txdata37		txdata53	
	txdata11		txdata27		txdata32		txdata48		vss
txdata0		vss		txdata31		vss		txdata52	
	txdata12		vss		txdata33		vss		txdata63
vss		txdata15		txdata30		txdata36		txdata51	
	txdata13		txdata28		txdata34		txdata49		txdataRD3
txdataRD0		txdata14		txdata29		txdata35		txdata50	
	vccio		vccio		vccio		vccio		vccio
vccio		vccio		vccio		vccio		vccio	
Die Edge									

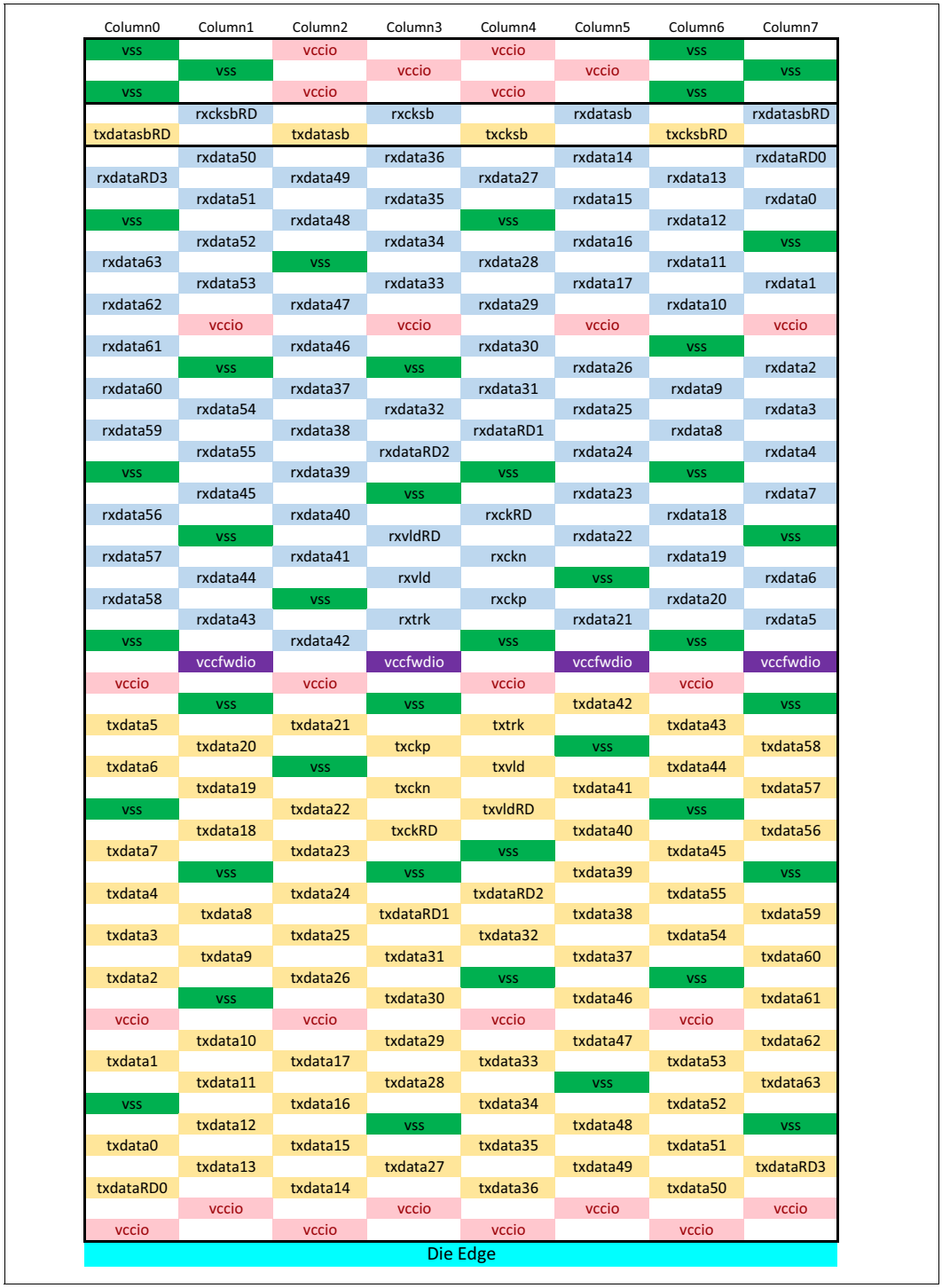
Note: In Figure 5-20, at 45-um pitch, the module depth of the 10-column reference bump matrix as shown is approximately 1043 um.

Figure 5-21. 16-column x64 Advanced Package Bump Map



Note: In Figure 5-21, at 25-um pitch, the module depth of the 16-column reference bump matrix as shown is approximately 388 um.

Figure 5-22. 8-column x64 Advanced Package Bump Map



Note: In Figure 5-22, at 55-um pitch, the module depth of the 8-column reference bump matrix as shown is approximately 1,585 um.

Figure 5-23 shows the signal exit order for the 10-column x64 Advanced Package bump map.

Figure 5-23. 10-column x64 Advanced Package Bump map: Signal exit order

Tx Breakout	Left to Right																
		txdataRD0	txdata0	txdata1	txdata2	txdata3	txdata4	txdata5	txdata6	txdata7	txdata8	txdata9	txdata10	txdata11	txdata12	txdata13	Cont…
	Cont…	txdata14	txdata15	txdata16	txdata17	txdata18	txdata19	txdata20	txdata21	txdata22	txdata23	txdata24	txdata25	txdata26	txdata27	txdata28	Cont1…
	Cont1…	txdata29	txdata30	txdata31	txdataRD1	txckRD	txckn	txckp	txtrk	txvld	txvldRD	txdataRD2	txdata32	txdata33	txdata34	txdata35	Cont2…
	Cont2…	txdata36	txdata37	txdata38	txdata39	txdata40	txdata41	txdata42	txdata43	txdata44	txdata45	txdata46	txdata47	txdata48	txdata49	txdata50	Cont3…
	Cont3…	txdata51	txdata52	txdata53	txdata54	txdata55	txdata56	txdata57	txdata58	txdata59	txdata60	txdata61	txdata62	txdata63	txdataRD3		
Rx Breakout	Left to Right																
		rxdataRD3	rxdata63	rxdata62	rxdata61	rxdata60	rxdata59	rxdata58	rxdata57	rxdata56	rxdata55	rxdata54	rxdata53	rxdata52	rxdata51	rxdata50	Cont…
	Cont…	rxdata49	rxdata48	rxdata47	rxdata46	rxdata45	rxdata44	rxdata43	rxdata42	rxdata41	rxdata40	rxdata39	rxdata38	rxdata37	rxdata36	rxdata35	Cont1…
	Cont1…	rxdata34	rxdata33	rxdata32	rxdataRD2	rxvldRD	rxvld	rxtrk	rxckp	rxckn	rxckRD	rxdataRD1	rxdata31	rxdata30	rxdata29	rxdata28	Cont2…
	Cont2…	rxdata27	rxdata26	rxdata25	rxdata24	rxdata23	rxdata22	rxdata21	rxdata20	rxdata19	rxdata18	rxdata17	rxdata16	rxdata15	rxdata14	rxdata13	Cont3…
	Cont3…	rxdata12	rxdata11	rxdata10	rxdata9	rxdata8	rxdata7	rxdata6	rxdata5	rxdata4	rxdata3	rxdata2	rxdata1	rxdata0	rxdataRD0		

IMPLEMENTATION NOTE — x64 BUMP MAPS FOR MAX SPEED

Three reference bump maps in Figure 5-20, Figure 5-21, and Figure 5-22 are recommended for different ranges of bump pitch, while PHY implementations have the flexibility to adjust the power and ground bumps to meet channel characteristics and power delivery requirements, which largely depend on the target speed and the advanced packaging technology capabilities.

At higher speeds, the PHY circuits draw larger current through the bumps and require better signal and power integrity of the packaging solution. This typically requires adding power and ground bumps and optimizing the distribution of them, but the implementation also needs to minimize the lane-to-lane length skew and preserve the assignment and relative order of the signals in each column to comply with the bump matrix rules in Section 5.7.2.2.

Table 5-13. Bump Map Options and the Recommended Bump Pitch Range and Max Speed

Bump Map	Bump Pitch (um)	Max Speed (GT/s)
16 column	25-30	12
	31-37	16
10 column	38-44	24
	45-50	32
8 column	51-55	32

This Implementation Note is formulated to provide PHY implementations a set of reference x64 bump maps to encompass the max speed specified. Table 5-13 summarizes the corresponding max speed for these bump map options and their recommended bump pitch ranges.

Bump maps in Figure 5-24, Figure 5-25, and Figure 5-26 are the x64 implementation references for the corresponding max speed with an enhancement of the power and ground bumps. They all comply with the bump matrix rules in Section 5.7.2.2, and they maintain the backward compatibility in terms of signal exit order. These reference examples have been optimized for signal integrity, power integrity, lane-to-lane skew, electro-migration stress and bump area based on most of the advanced packaging technologies in the industry. Please note that technology requirements vary, and it is still required to verify the bump map with the technology provider for actual implementation requirements and performance targets.

Figure 5-24. 10-column x64 Advanced Package Bump Map Example for 32 GT/s Implementation

	1	2	3	4	5	6	7	8	9	10
1	vss		vss		vccio		vccio		vss	
2		vss		vccio		vccio		vss		vss
3	vss		vss		vccio		vccio		vss	
4		rxcksbRD		rxcksb		vccio		rxdatasb		rxdatasbRD
5	txdatasbRD		txdatasb		vss		txcksb		txcksbRD	
6		rxdata50		rxdata35		rxdata29		rxdata14		rxdataRD0
7	rxdataRD3		rxdata49		rxdata34		rxdata28		rxdata13	
8		rxdata51		vccio		vccio		vccio		vccio
9	vccio		vss		rxdata33		vss		rxdata12	
10		rxdata52		rxdata36		rxdata30		rxdata15		vss
11	vss		rxdata48		vss		rxdata27		rxdata11	
12		rxdata53		rxdata37		rxdata31		rxdata16		rxdata0
13	rxdata63		rxdata47		rxdata32		rxdata26		rxdata10	
14		vccio		vccio		vccio		vccio		vccio
15	rxdata62		rxdata46		rxdataRD2		rxdata25		rxdata9	
16		rxdata54		rxdata38		rxdataRD1		rxdata17		rxdata1
17	vss		vss		vss		vss		vss	
18		rxdata55		rxdata39		vccio		rxdata18		rxdata2
19	rxdata61		rxdata45		rxvldRD		rxdata24		rxdata8	
20		vccio		vccio		vccio		vccio		vccio
21	rxdata60		rxdata44		rxvld		rxdata23		rxdata7	
22		rxdata56		rxdata40		rxckRD		rxdata19		rxdata3
23	vss		vss		vss		vss		vss	
24		rxdata57		rxdata41		rxckn		rxdata20		rxdata4
25	rxdata59		rxdata43		rxtrk		rxdata22		rxdata6	
26		rxdata58		vss		rxckp		rxdata21		vss
27	vss		rxdata42		vss		vss		rxdata5	
28		vccfwdio		vccfwdio		vccfwdio		vccfwdio		vccfwdio
29	vss		vss		vss		vss		vss	
30		txdata5		vccio		vccio		txdata42		vccio
31	vccio		txdata21		txckp		vccio		txdata58	
32		txdata6		txdata22		txtrk		txdata43		txdata59
33	txdata4		txdata20		txckn		txdata41		txdata57	
34		vccio		vccio		vccio		vccio		vccio
35	txdata3		txdata19		txckRD		txdata40		txdata56	
36		txdata7		txdata23		txvld		txdata44		txdata60
37	vss		vss		vss		vss		vss	
38		txdata8		txdata24		txvldRD		txdata45		txdata61
39	txdata2		txdata18		vss		txdata39		txdata55	
40		vccio		vccio		vccio		vccio		vccio
41	txdata1		txdata17		txdataRD1		txdata38		txdata54	
42		txdata9		txdata25		txdataRD2		txdata46		txdata62
43	vss		vss		vss		vss		vss	
44		txdata10		txdata26		txdata32		txdata47		txdata63
45	txdata0		txdata16		txdata31		txdata37		txdata53	
46		txdata11		txdata27		vccio		txdata48		vccio
47	vccio		txdata15		txdata30		txdata36		txdata52	
48		txdata12		vccio		txdata33		vccio		vss
49	vss		vss		vss		vss		txdata51	
50		txdata13		txdata28		txdata34		txdata49		txdataRD3
51	txdataRD0		txdata14		txdata29		txdata35		txdata50	
52		vccio		vss		vss		vccio		vccio
53	vccio		vccio		vccio		vccio		vccio	
	Die Edge									

Note: In Figure 5-24, at 45-um pitch, the module depth of the 10-column bump map as shown is approximately 1225 um. Rows 1, 2, and 53 are required for packaging solutions using floating bridges without through-silicon vias (TSVs). They can be optional for packaging solutions with TSVs.

Figure 5-25. 16-column x64 Advanced Package Bump Map Example for 16 GT/s Implementation

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	vss		vccio		vccio		vss		vss		vccio		vccio		vss	
2		vss		vccio		vccio		vss		vss		vccio		vccio		vss
3	txdatasbRD		rxcksbRD		txdatasb		rxcksb		txcksb		rxdatasb		txcksbRD		rxdatasbRD	
4		rxdata54		rxdata50		rxdata35		vss		rxdata29		rxdata14		rxdata11		rxdataRD0
5	rxdataRD3		rxdata52		rxdata49		rxdata34		vss		rxdata28		rxdata13		rxdata9	
6		rxdata55		rxdata51		rxdata36		rxdataRD2		rxdata30		rxdata15		rxdata10		vss
7	vss		rxdata53		rxdata48		rxdata33		rxdataRD1		rxdata27		rxdata12		rxdata8	
8		rxdata61		vss		rxdata37		vss		rxdata31		vss		rxdata7		vss
9	rxdata63		rxdata56		vss		rxdata32		vss		rxdata26		vss		rxdata2	
10		vccio		rxdata46		vccio		rxvldRD		vccio		rxdata16		vccio		rxdata0
11	vss		vccio		rxdata47		vccio		rxckRD		vccio		rxdata17		vccio	
12		rxdata60		rxdata45		rxdata40		rxvld		rxdata25		rxdata20		rxdata6		vss
13	rxdata62		rxdata57		rxdata43		rxdata38		rxckn		rxdata23		rxdata18		rxdata3	
14		rxdata59		rxdata44		rxdata41		rxtrk		rxdata24		rxdata21		rxdata5		rxdata1
15	vss		rxdata58		rxdata42		rxdata39		rxckp		rxdata22		rxdata19		rxdata4	
16		vccfwdio		vss		vccfwdio		vss		vccfwdio		vss		vccfwdio		vss
17	vss		vccfwdio		vss		vccfwdio		vss		vccfwdio		vss		vccfwdio	
18		txdata4		txdata19		txdata22		txckp		txdata39		txdata42		txdata58		vss
19	txdata1		txdata5		txdata21		txdata24		txtrk		txdata41		txdata44		txdata59	
20		txdata3		txdata18		txdata23		txckn		txdata38		txdata43		txdata57		txdata62
21	vss		txdata6		txdata20		txdata25		txvld		txdata40		txdata45		txdata60	
22		vccio		txdata17		vccio		txckRD		vccio		txdata47		vccio		vss
23	txdata0		vccio		txdata16		vccio		txvldRD		vccio		txdata46		vccio	
24		txdata2		vss		txdata26		vss		txdata32		vss		txdata56		txdata63
25	vss		txdata7		vss		txdata31		vss		txdata37		vss		txdata61	
26		txdata8		txdata12		txdata27		txdataRD1		txdata33		txdata48		txdata53		vss
27	vss		txdata10		txdata15		txdata30		txdataRD2		txdata36		txdata51		txdata55	
28		txdata9		txdata13		txdata28		vss		txdata34		txdata49		txdata52		txdataRD3
29	txdataRD0		txdata11		txdata14		txdata29		vss		txdata35		txdata50		txdata54	
30		vccio		vccio		vccio		vccio		vccio		vccio		vccio		vccio
31	vccio		vccio		vccio		vccio		vccio		vccio		vccio		vccio	
	Die Edge															

Note: In Figure 5-25, at 25-um pitch, the module depth of the 16-column bump map as shown is approximately 400 um. Rows 1 and 31 are required for packaging solutions using floating bridges without TSVs. They can be optional for packaging solutions with TSVs.

Figure 5-26. 8-column x64 Advanced Package Bump Map Example for 32 GT/s Implementation

	1	2	3	4	5	6	7	8
1	vss		vccio		vccio		vss	
2		vss		vccio		vccio		vss
3	vss		vccio		vccio		vss	
4		rxcksbRD		rxcksb		rxdatasb		rxdatasbRD
5	txdatasbRD		txdatasb		txcksb		txcksbRD	
6		rxdata50		vss		rxdata14		rxdataRD0
7	rxdataRD3		rxdata49		rxdata27		rxdata13	
8		vccio		rxdata36		vss		vccio
9	rxdata63		rxdata48		rxdata28		rxdata12	
10		rxdata51		rxdata35		rxdata15		rxdata0
11	vss		vss		vss		vss	
12		rxdata52		rxdata34		rxdata16		rxdata1
13	rxdata62		rxdata47		rxdata29		rxdata11	
14		vccio		vccio		vccio		vccio
15	rxdata61		rxdata46		rxdata30		rxdata10	
16		rxdata53		rxdata33		rxdata17		rxdata2
17	rxdata60		rxdata37		rxdata31		rxdata9	
18		rxdata54		rxdata32		rxdata26		rxdata3
19	vss		vss		vss		vss	
20		rxdata55		rxdataRD2		rxdata25		rxdata4
21	rxdata59		rxdata38		rxdataRD1		rxdata8	
22		vccio		vccio		rxdata24		vccio
23	rxdata56		rxdata39		vccio		rxdata18	
24		rxdata45		rxvldRD		rxdata23		rxdata7
25	vss		rxdata40		vss		vss	
26		vccio		rxvld		rxdata22		rxdata6
27	rxdata57		vss		rxckRD		rxdata19	
28		rxdata44		vccio		vccio		vccio
29	rxdata58		rxdata41		rxckn		rxdata20	
30		rxdata43		rxtrk		rxdata21		rxdata5
31	vss		rxdata42		rxckp		vss	
32		vccfwdio		vccfwdio		vccfwdio		vccfwdio
33	vss		vss		vss		vss	
34		vccio		txckp		txdata42		vccio
35	txdata5		txdata21		txtrk		txdata43	
36		txdata20		txckn		txdata41		txdata58
37	vss		vss		vss		txdata44	
38		txdata19		txckRD		vccio		txdata57
39	txdata6		txdata22		txvld		vss	
40		vccio		vccio		txdata40		vccio
41	txdata7		txdata23		txvldRD		txdata45	
42		txdata18		vss		txdata39		txdata56
43	vss		txdata24		vss		vss	
44		txdata8		txdataRD1		txdata38		txdata59
45	txdata4		txdata25		txdataRD2		txdata55	
46		vccio		vccio		vccio		vccio
47	txdata3		txdata26		txdata32		txdata54	
48		txdata9		txdata31		txdata37		txdata60
49	txdata2		txdata17		txdata33		txdata53	
50		txdata10		txdata30		txdata46		txdata61
51	vss		vss		vss		vss	
52		txdata11		txdata29		txdata47		txdata62
53	txdata1		txdata16		txdata34		txdata52	
54		vccio		vccio		vccio		vccio
55	txdata0		txdata15		txdata35		txdata51	
56		txdata12		txdata28		txdata48		txdata63
57	vss		vss		txdata36		vss	
58		txdata13		txdata27		txdata49		txdataRD3
59	txdataRD0		txdata14		vss		txdata50	
60		vccio		vccio		vccio		vccio
61	vccio		vccio		vccio		vccio	
	Die Edge							

Note: In Figure 5-26, at 55-um pitch, the module depth of the 8-column bump map as shown is approximately 1705 um. Rows 1, 2, and 61 are required for packaging solutions using floating bridges without TSVs. They can be optional for packaging solutions with TSVs.

5.7.2.3 x32 Advanced Package Module Bump Map

UCIe also defines a x32 Advanced Package Module that supports 32 Tx and 32 Rx data signals and two redundant bumps each for Tx and two for Rx (total of four) for lane-repair functions. All other signals, including the sidebands, are the same as those of the x64 Advanced Package.

Figure 5-27, Figure 5-28, and Figure 5-29 show the reference bump matrix for the 10-column, 16-column, and 8-column x32 Advanced Package Modules, respectively. The lower left corner of the bump map will be considered "origin" of a bump matrix and the leftmost column is Column 0.

It is strongly recommended to follow the bump matrices provided in Figure 5-27, Figure 5-28, and Figure 5-29 for x32 Advanced Package Modules.

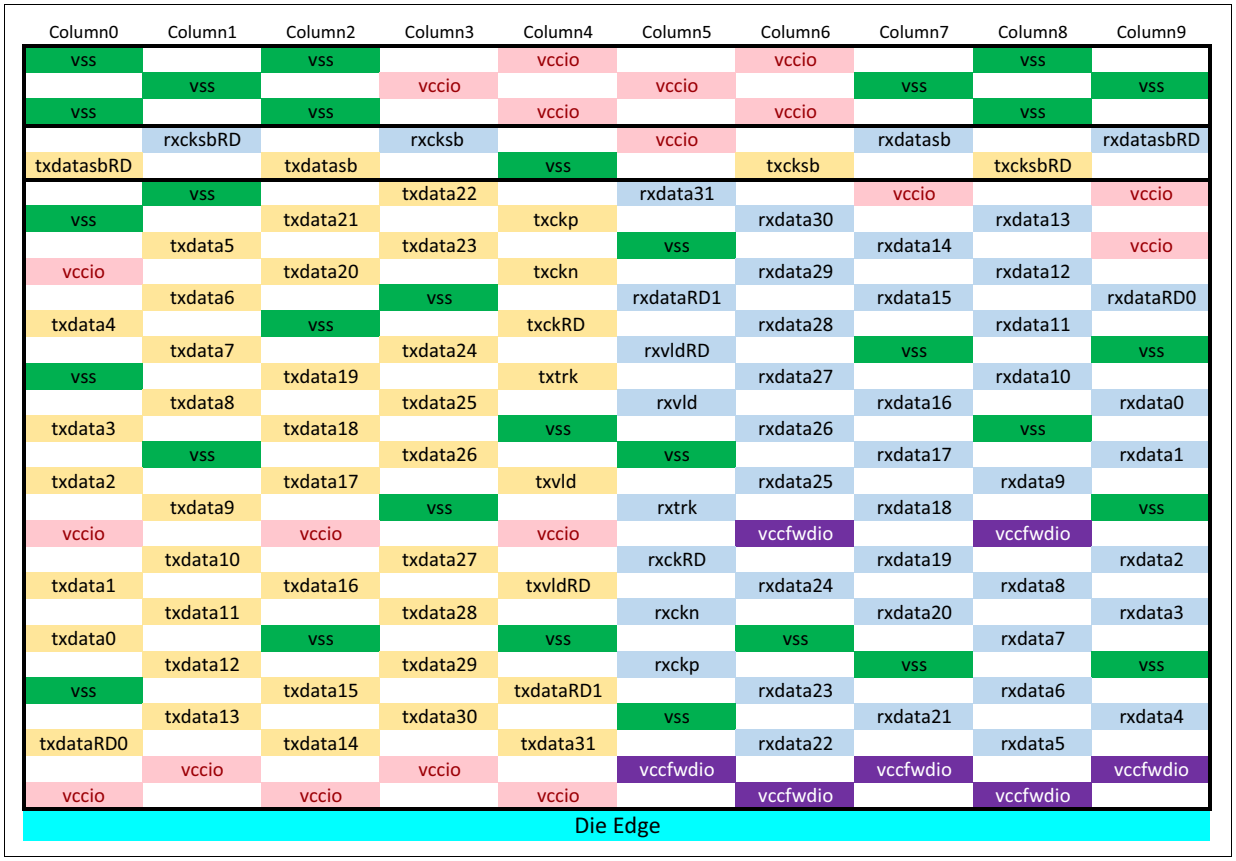
The following rule must be followed for the 10-column x32 Advanced Package bump matrix:

- The signals order within a column must be preserved. For example, Column 0 must contain the signals: **txdataRD0**, **txdata0**, **txdata1**, **txdata2**, **txdata3**, **txdata4**, and **txdatasbRD**. Similarly, 16-column and 8-column x32 Advanced Packages must preserve the signal order within a column of the respective bump matrices.

It is strongly recommended to follow the supply and **ground** pattern shown in the bump matrices. It must be ensured that sufficient supply and **ground** bumps are provided to meet channel characteristics (FEXT and NEXT) and power-delivery requirements.

When instantiating multiple x32 Advanced Package Modules, the same rules as defined in Section 5.7.2.2 must be followed.

Figure 5-27. 10-column x32 Advanced Package Bump Map

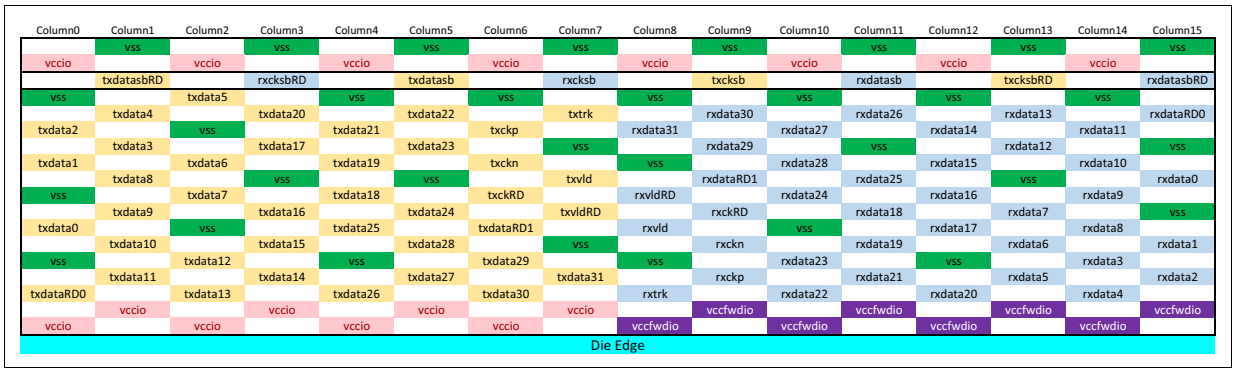


Column0	Column1	Column2	Column3	Column4	Column5	Column6	Column7	Column8	Column9
vss		vss		vccio		vccio		vss	
	vss		vccio		vccio		vss		vss
vss		vss		vccio		vccio		vss	
	rxcksbRD		rxcksb		vccio		rxdatasb		rxdatasbRD
txdatasbRD		txdatasb		vss		txcksb		txcksbRD	
	vss		txdata22		rxdata31		vccio		vccio
vss		txdata21		txckp		rxdata30		rxdata13	
	txdata5		txdata23		vss		rxdata14		vccio
vccio		txdata20		txckn		rxdata29		rxdata12	
	txdata6		vss		rxdataRD1		rxdata15		rxdataRD0
txdata4		vss		txckRD		rxdata28		rxdata11	
	txdata7		txdata24		rxvldRD		vss		vss
vss		txdata19		txtrk		rxdata27		rxdata10	
	txdata8		txdata25		rxvld		rxdata16		rxdata0
txdata3		txdata18		vss		rxdata26		vss	
	vss		txdata26		vss		rxdata17		rxdata1
txdata2		txdata17		txvld		rxdata25		rxdata9	
	txdata9		vss		rxtrk		rxdata18		vss
vccio		vccio		vccio		vccfwdio		vccfwdio	
	txdata10		txdata27		rxckRD		rxdata19		rxdata2
txdata1		txdata16		txvldRD		rxdata24		rxdata8	
	txdata11		txdata28		rxckn		rxdata20		rxdata3
txdata0		vss		vss		vss		rxdata7	
	txdata12		txdata29		rxckp		vss		vss
vss		txdata15		txdataRD1		rxdata23		rxdata6	
	txdata13		txdata30		vss		rxdata21		rxdata4
txdataRD0		txdata14		txdata31		rxdata22		rxdata5	
	vccio		vccio		vccfwdio		vccfwdio		vccfwdio
vccio		vccio		vccio		vccfwdio		vccfwdio	

Die Edge

Note: In Figure 5-27, at 45-um pitch, the module depth of the 10-column reference bump matrix as shown is approximately 680.5 um.

Figure 5-28. 16-column x32 Advanced Package Bump Map

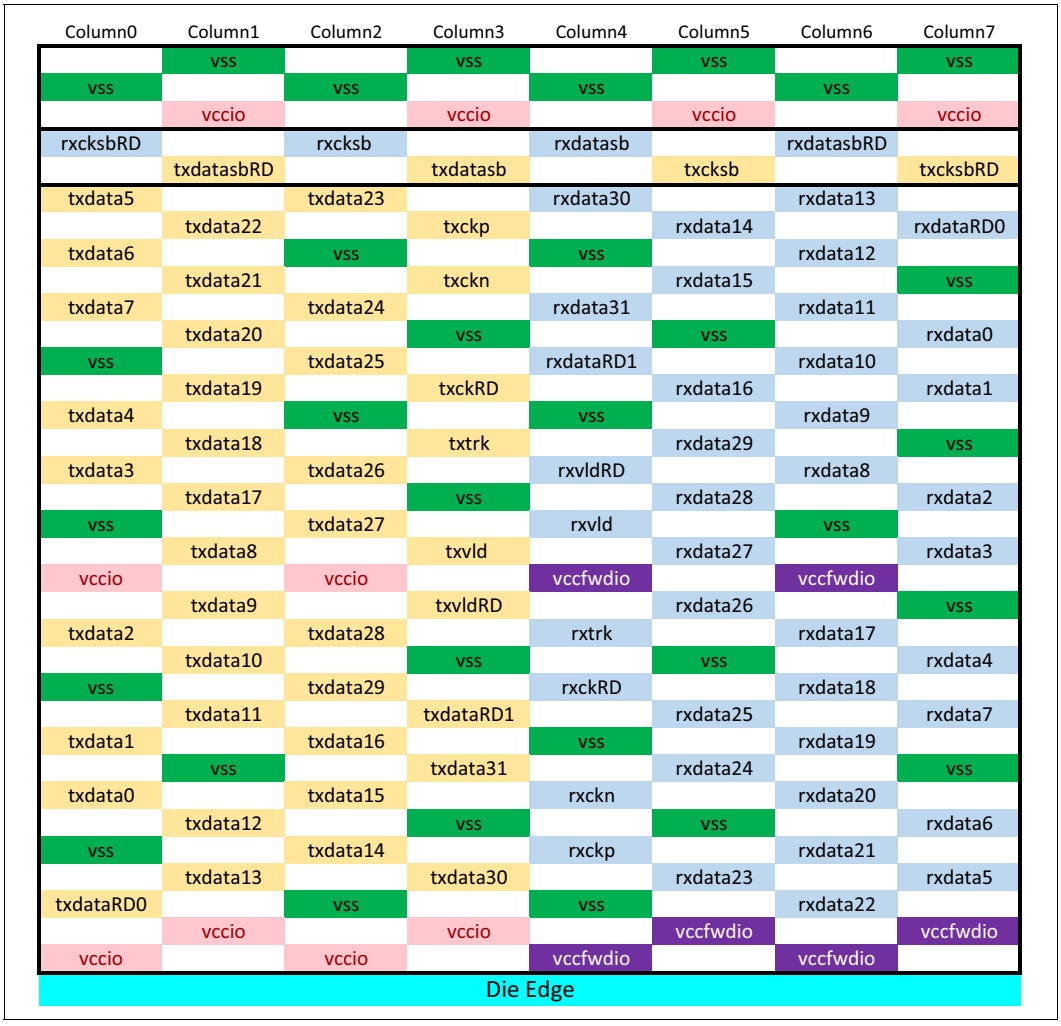


Column0	Column1	Column2	Column3	Column4	Column5	Column6	Column7	Column8	Column9	Column10	Column11	Column12	Column13	Column14	Column15
	vss		vss		vss		vss		vss		vss		vss		vss
vccio		vccio		vccio		vccio		vccio		vccio		vccio		vccio	
	txdatasbRD		rxcksbRD		txdatasb		rxcksb		txcksb		rxdatasb		txcksbRD		rxdatasbRD
vss		txdata5		vss		vss		vss		vss		vss		vss	
	txdata4		txdata20		txdata22		txtrk		rxdata30		rxdata26		rxdata13		rxdataRD0
txdata2		vss		txdata21		txckp		rxdata31		rxdata27		rxdata14		rxdata11	
	txdata3		txdata17		txdata23		vss		rxdata29		vss		rxdata12		vss
txdata1		txdata6		txdata19		txckn		vss		rxdata28		rxdata15		rxdata10	
	txdata8		vss		vss		txvld		rxdataRD1		rxdata25		vss		rxdata0
vss		txdata7		txdata18		txckRD		rxvldRD		rxdata24		rxdata16		rxdata9	
	txdata9		txdata16		txdata24		txvldRD		rxckRD		rxdata18		rxdata7		vss
txdata0		vss		txdata25		txdataRD1		rxvld		vss		rxdata17		rxdata8	
	txdata10		txdata15		txdata28		vss		rxckn		rxdata19		rxdata6		rxdata1
vss		txdata12		vss		txdata29		vss		rxdata23		vss		rxdata3	
	txdata11		txdata14		txdata27		txdata31		rxckp		rxdata21		rxdata5		rxdata2
txdataRD0		txdata13		txdata26		txdata30		rxtrk		rxdata22		rxdata20		rxdata4	
	vccio		vccio		vccio		vccio		vccfwdio		vccfwdio		vccfwdio		vccfwdio
vccio		vccio		vccio		vccio		vccfwdio		vccfwdio		vccfwdio		vccfwdio	

Die Edge

Note: In Figure 5-28, at 25-um pitch, the module depth of the 16-column reference bump matrix as shown is approximately 237.5 um.

Figure 5-29. 8-column x32 Advanced Package Bump Map



Note: In Figure 5-29, at 55-um pitch, the module depth of the 8-column reference bump matrix as shown is approximately 962.5 um.

Figure 5-30 shows the signal exit order for the 10-column x32 Advanced Package bump map.

Figure 5-30. 10-column x32 Advanced Package Bump Map: Signal Exit Order

Tx Breakout	**Left to Right**											
		txdataRD0	txdata0	txdata1	txdata2	txdata3	txdata4	txdata5	txdata6	txdata7	txdata8	Cont…
	Cont…	txdata9	txdata10	txdata11	txdata12	txdata13	txdata14	txdata15	txdata16	txdata17	txdata18	Cont1…
	Cont1…	txdata19	txdata20	txdata21	txdata22	txdata23	txdata24	txdata25	txdata26	txdata27	txdata28	Cont2…
	Cont2…	txdata29	txdata30	txdata31	txdataRD1	txvldRD	txvld	txtrk	txckRD	txckn	txckp	
Rx Breakout	**Left to Right**											
		rxckp	rxckn	rxckRD	rxtrk	rxvld	rxvldRD	rxdataRD1	rxdata31	rxdata30	rxdata29	Cont…
	Cont…	rxdata28	rxdata27	rxdata26	rxdata25	rxdata24	rxdata23	rxdata22	rxdata21	rxdata20	rxdata19	Cont1…
	Cont1…	rxdata18	rxdata17	rxdata16	rxdata15	rxdata14	rxdata13	rxdata12	rxdata11	rxdata10	rxdata9	Cont2…
	Cont2…	rxdata8	rxdata7	rxdata6	rxdata5	rxdata4	rxdata3	rxdata2	rxdata1	rxdata0	rxdataRD0	

IMPLEMENTATION NOTE — x32 Bump Maps for Max Speed

This Implementation Note is formulated to provide PHY implementations a set of reference x32 bump maps to encompass the max speed specified.

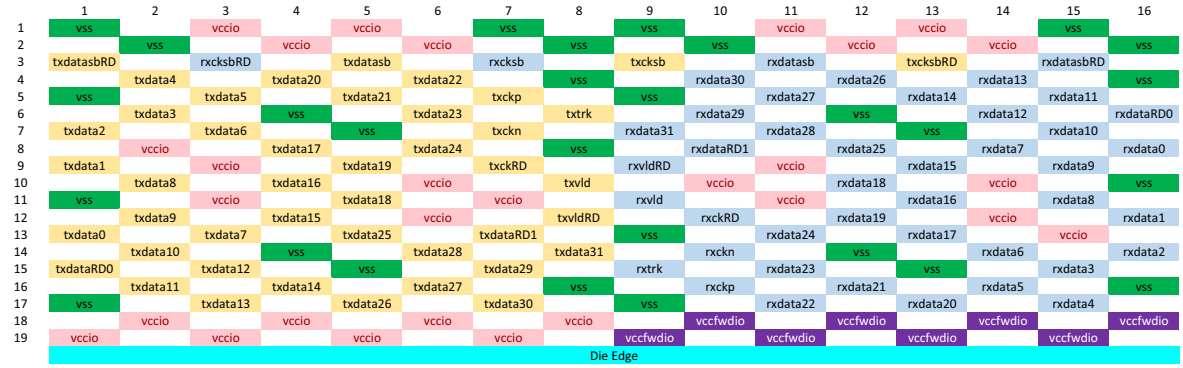
Bump maps in Figure 5-31, Figure 5-32, and Figure 5-33 are the x32 implementation references for the corresponding max speed with an enhancement of the power and ground bumps. They all comply with the bump matrix rules in Section 5.7.2.3, and they maintain the backward compatibility in terms of signal exit order. These reference examples have been optimized for signal integrity, power integrity, lane-to-lane skew, electro-migration stress and bump area based on most of the advanced packaging technologies in the industry. Please note that technology requirements vary, and it is still required to verify the bump map with the technology provider for actual implementation requirements and performance targets.

Figure 5-31. 10-column x32 Advanced Package Bump Map Example for 32 GT/s Implementation

	1	2	3	4	5	6	7	8	9	10
1	vss		vss		vccio		vccio		vss	
2		vss		vccio		vccio		vss		vss
3	vss		vss		vccio		vccio		vss	
4		rxcksbRD		rxcksb		vccio		rxdatasb		rxdatasbRD
5	txdatasbRD		txdatasb		vss		txcksb		txcksbRD	
6		txdata5		vccio		vss		rxdata14		vccio
7	txdata4		txdata21		txckp		rxdata30		rxdata13	
8		txdata6		txdata22		vccio		vccio		rxdataRD0
9	vss		vss		txckn		rxdata29		rxdata12	
10		txdata7		txdata23		rxdata31		rxdata15		vccio
11	vccio		txdata20		txckRD		rxdata28		vss	
12		vccio		vccio		vccio		rxdata16		rxdata0
13	txdata3		txdata19		txtrk		rxdata27		rxdata11	
14		txdata8		txdata24		rxdataRD1		vccio		rxdata1
15	vss		vss		vss		vss		rxdata10	
16		txdata9		txdata25		rxvldRD		rxdata17		vss
17	txdata2		txdata18		txvld		rxdata26		vss	
18		vccio		txdata26		rxvld		rxdata18		rxdata2
19	vccio		txdata17		txvldRD		rxdata25		rxdata9	
20		txdata10		vccio		vccio		vccio		vccio
21	txdata1		vss		txdataRD1		rxdata24		rxdata8	
22		txdata11		txdata27		rxtrk		rxdata19		rxdata3
23	txdata0		txdata16		vss		vccfwdio		vccfwdio	
24		vccio		txdata28		rxckRD		rxdata20		vss
25	vss		txdata15		txdata31		rxdata23		rxdata7	
26		txdata12		txdata29		rxckn		vss		vss
27	txdataRD0		vss		vss		rxdata22		rxdata6	
28		txdata13		txdata30		rxckp		rxdata21		rxdata4
29	vss		txdata14		vss		vss		rxdata5	
30		vccio		vccio		vccfwdio		vccfwdio		vccfwdio
31	vccio		vccio		vccio		vccfwdio		vccfwdio	
	Die Edge									

Note: In Figure 5-31, at 45-um pitch, the module depth of the 10-column bump map as shown is approximately 725 um. Rows 1, 2, and 31 are required for packaging solutions using floating bridges without through-silicon vias (TSVs). They can be optional for packaging solutions with TSVs. The vccfwdio bumps are required for the tightly coupled mode up to 16 GT/s. For higher speeds, the vccfwdio bumps may be connected to the vccio bumps in package.

Figure 5-32. 16-column x32 Advanced Package Bump Map Example for 16 GT/s Implementation



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	vss		vccio		vccio		vss		vss		vccio		vccio		vss	
2		vss		vccio		vccio		vss		vss		vccio		vccio		vss
3	txdatasbRD		rxcksbRD		txdatasb		rxcksb		txcksb		rxdatasb		txcksbRD		rxdatasbRD	
4		txdata4		txdata20		txdata22		vss		rxdata30		rxdata26		rxdata13		vss
5	vss		txdata5		txdata21		txckp		vss		rxdata27		rxdata14		rxdata11	
6		txdata3		vss		txdata23		txtrk		rxdata29		vss		rxdata12		rxdataRD0
7	txdata2		txdata6		vss		txckn		rxdata31		rxdata28		vss		rxdata10	
8		vccio		txdata17		txdata24		vss		rxdataRD1		rxdata25		rxdata7		rxdata0
9	txdata1		vccio		txdata19		txckRD		rxvldRD		vccio		rxdata15		rxdata9	
10		txdata8		txdata16		vccio		txvld		vccio		rxdata18		vccio		vss
11	vss		vccio		txdata18		vccio		rxvld		vccio		rxdata16		rxdata8	
12		txdata9		txdata15		vccio		txvldRD		rxckRD		rxdata19		vccio		rxdata1
13	txdata0		txdata7		txdata25		txdataRD1		vss		rxdata24		rxdata17		vccio	
14		txdata10		vss		txdata28		txdata31		rxckn		vss		rxdata6		rxdata2
15	txdataRD0		txdata12		vss		txdata29		rxtrk		rxdata23		vss		rxdata3	
16		txdata11		txdata14		txdata27		vss		rxckp		rxdata21		rxdata5		vss
17	vss		txdata13		txdata26		txdata30		vss		rxdata22		rxdata20		rxdata4	
18		vccio		vccio		vccio		vccio		vccfwdio		vccfwdio		vccfwdio		vccfwdio
19	vccio		vccio		vccio		vccio		vccfwdio		vccfwdio		vccfwdio		vccfwdio	
	Die Edge															

Note: In Figure 5-32, at 25-um pitch, the module depth of the 16-column bump map as shown is approximately 250 um. Rows 1 and 19 are required for packaging solutions using floating bridges without TSVs. They can be optional for packaging solutions with TSVs. The vccfwdio bumps are required for the tightly coupled mode up to 16 GT/s. For higher speeds, the vccfwdio bumps may be connected to the vccio bumps in package.

Figure 5-33. 8-column x32 Advanced Package Bump Map Example for 32 GT/s Implementation

	1	2	3	4	5	6	7	8
1	vss		vccio		vccio		vss	
2		vss		vccio		vccio		vss
3	vss		vccio		vccio		vss	
4		txdatasbRD		txdatasb		txcksb		txcksbRD
5	rxcksbRD		rxcksb		rxdatasb		rxdatasbRD	
6		txdata22		txckp		rxdata14		rxdataRD0
7	vss		txdata23		vss		rxdata13	
8		txdata21		txckn		vccio		vccio
9	txdata5		vss		rxdata30		rxdata12	
10		vccio		vccio		rxdata15		rxdata0
11	txdata6		txdata24		rxdata31		rxdata11	
12		txdata20		txckRD		rxdata16		rxdata1
13	vss		vss		vss		vss	
14		txdata19		txtrk		rxdata29		rxdata2
15	txdata7		txdata25		rxdataRD1		rxdata10	
16		txdata18		vccio		rxdata28		rxdata3
17	vccio		txdata26		vss		rxdata9	
18		txdata17		txvld		rxdata27		vccio
19	txdata4		vss		rxvldRD		rxdata8	
20		txdata8		txvldRD		vccio		rxdata4
21	vss		txdata27		rxvld		rxdata17	
22		txdata9		vccio		rxdata26		vss
23	txdata3		txdata28		vss		rxdata18	
24		txdata10		txdataRD1		rxdata25		rxdata7
25	txdata2		txdata29		rxtrk		rxdata19	
26		vccio		vccio		vccio		vccfwdio
27	txdata1		txdata16		rxckRD		rxdata20	
28		txdata11		txdata31		rxdata24		rxdata6
29	txdata0		txdata15		vss		vss	
30		txdata12		txdata30		vccfwdio		rxdata5
31	vss		vss		rxckn		rxdata21	
32		txdata13		vss		rxdata23		vss
33	txdataRD0		txdata14		rxckp		rxdata22	
34		vccio		vccio		vccfwdio		vccfwdio
35	vccio		vccio		vccfwdio		vccfwdio	
	Die Edge							

Note: In Figure 5-33, at 55-um pitch, the module depth of the 8-column bump map as shown is approximately 990 um. Rows 1, 2, and 35 are required for packaging solutions using floating bridges without TSVs. They can be optional for packaging solutions with TSVs. The vccfwdio bumps are required for the tightly coupled mode up to 16 GT/s. For higher speeds, the vccfwdio bumps may be connected to the vccio bumps in package.

These bump maps have been optimized to minimize the lane to-lane routing mismatch, which is not avoidable when two different bumps at different bump pitches interoperate. Table 5-14 summarizes the max skew due to bump locations for the representative cases. As a rule of thumb, each 150-um mismatch causes about 1-ps timing skew. This skew can be reduced or eliminated by the length matching effort in package channel layout design.

Table 5-14. Maximum Systematic Lane-to-lane Length Mismatch in um between the Reference Bump Maps in the Implementation Note

Rx / Tx	16-column x64 at 25 um	16-column x32 at 25 um	10-column x64 at 45 um	10-column x32 at 45 um	8-column x64 at 55 um	8-column x32 at 55 um
16-column x64 at 25 um	0	125	351	399	560	605
16-column x32 at 25 um		0	351	393	563	618
10-column x64 at 45 um			0	159	351	463
10-column x32 at 45 um				0	428	398
8-column x64 at 55 um					0	468
8-column x32 at 55 um						0

5.7.2.4 x64 and x32 Advanced Package Module Interoperability

x64 and x32 Advanced Package Module bump maps enable interoperability between all Tx and Rx combinations of x64 or x32, 10-column, 16-column, or 8-column Modules, in both Normal-to-Normal module orientation or Normal-to-Mirrored module orientation.

However, if x64 to x32 modules or x32 to x32 modules have normal and mirrored orientation as shown in Figure 5-34 and Figure 5-35, respectively, signal traces between the TX half and RX half will crisscross and require swizzling technique which refers to rearranging the physical connections between signal bumps of two chiplets to optimize the layout and routing on the interposer or substrate. It involves changing the order of the connections or route on different layers without altering the netlist or the electrical functionality of the design. Moreover, connections between 8-column, 16-column, and 10-column modules may need to be routed to adjacent columns (swizzle and go across). In all cases, the electrical spec must be met for all these connections.

It is optional for a x64 Module to support interoperability with a x32 Module. The following requirements apply when a x64 module supports x32 interoperability:

- When a x64 module connects to x32 module, the connection shall always be contained to the lower half of the x64 module. This must be followed even with x32 lane reversal described below.
- Electrical specifications must be met for combinations that require signal-routing swizzling.
- Lane reversal will not be permitted on **CKP-**, **CKN-**, **CKRD-**, **VLD-**, **VLDRD-**, **TRK-**, and sideband-related pins. These pins need to be connected appropriately. Swizzling for these connections is acceptable.
- x64 module must support a lane-reversal mode in a x32 manner (i.e., **TD_P[31:0]** = **TD_L[0:31]**. When a x64 module is connected to a x32 module, in either Normal or Mirrored orientation, the upper 32 bits are not used and should be disabled.
- It is not permitted for a single module of larger width to simultaneously interop with two or more modules of a lower width. For example, a x64 Advanced Package module physically connected to two x32 Advanced Package modules is prohibited.

Additional technological capabilities or layers may be needed to accomplish swizzling on data/auxiliary signals.

Table 5-15 summarizes the connections between combinations of x64 and x32 modules in both Normal-to-Normal and Normal-to-Mirrored module orientations. The table applies to all combinations of 10-column, 16-column, or 8-column modules on either side of the Link.

Table 5-15. x64 and x32 Advanced Package Connectivity Matrix

–			Normal Module		Mirrored Module	
–			Rx			
			x64	x32	x64	x32
Normal Module	Tx	x64	TX[63:0] – RX[63:0][a]	TX[31:0] – RX[31:0][b]	rTX[63:0] – RX[0:63][c d]	rTX[31:0] – RX[0:31][c e]
		x32	TX[31:0] – RX[31:0][b]	TX[31:0] – RX[31:0][b]	rTX[31:0] – RX[0:31][c e]	rTX[31:0] – RX[0:31][c e]

a. Entry "TX[63:0] – RX[63:0]" is for Normal Module connections between two x64 modules without lane reversal. This applies to x64–to–x64 combination.
b. Entry "TX[31:0] – RX[31:0]" is for Normal Module connections between lower 32-bit half without lane reversal. This applies to x64-to-x32, x32-to-x64, and x32-to-x32 combinations.
c. The prefix "r" means lane reversal is enabled on the Transmitter lanes, and:
   - "rTX[63:0]" means TD_P[63:0] = TD_L[0:63], to be connected with RD_P[0:63]
   - "rTX[31:0]" means TD_P[31:0] = TD_L[0:31], to be connected with RD_P[0:31].
d. Entry "rTX[63:0] – RX[0:63]" = Normal-to-Mirrored Module connections between two x64 modules with TX lane reversal. This applies to x64-to-x64 Normal-to-Mirrored combinations.
e. Entry "rTX[31:0] – RX[0:31]" = Normal-to-Mirrored Module connections between lower 32-bit half with TX lane reversal. This applies to x64-to-x32, x32-to-x64, and x32-to-x32 Normal-to-Mirrored combinations.

The defined bump matrices can achieve optimal skew between bump matrices of differing depths, and the worst-case trace-reach skews are expected to be within the maximum lane-to-lane skew limit for the corresponding data rates as defined in Section 5.3 and Section 5.4.

Figure 5-34 and Figure 5-35 show examples of normal and mirrored x64-to-x32 and x32-to-x32 Advanced Package Module connections, respectively.

Figure 5-34. Example of Normal and Mirrored x64-to-x32 Advanced Package Module Connection

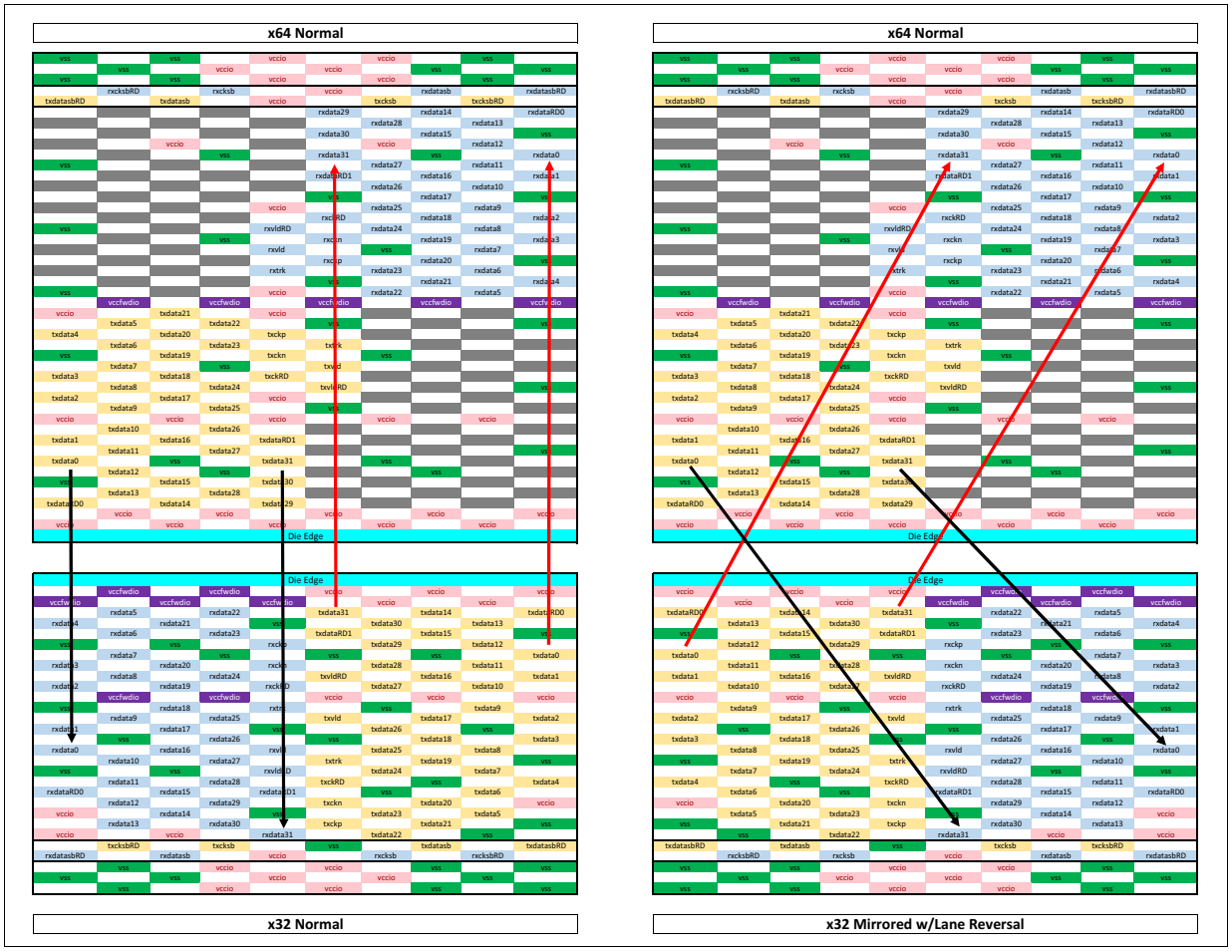
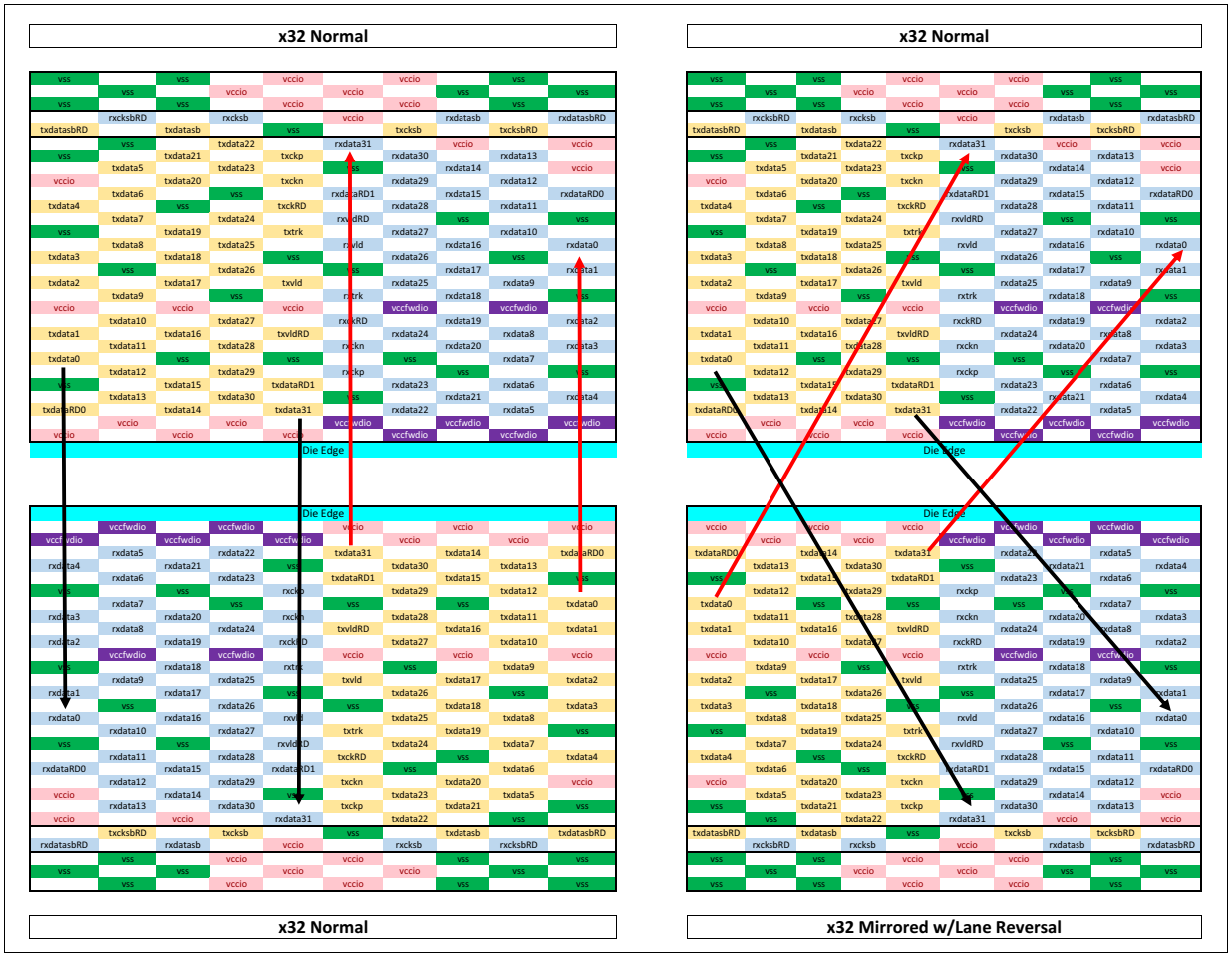


Figure 5-35. Example of Normal and Mirrored x32-to-x32 Advanced Package Module Connection



5.7.2.5 Module Naming of Advanced Package Modules

This section describes the Module naming convention of x64 and x32 Advanced Package modules in a multi-module configuration.

The Module naming is defined to help with connecting the Modules deterministically which, in turn, will help minimize the multiplexing requirements in the Multi-module PHY Logic (MMPL).

The naming of M0, M1, M2, and M3 will apply to 1, 2, or 4 Advanced Package modules that are aggregated through the MMPL.

Figure 5-36 shows the naming convention for 1, 2, or 4 Advanced Package Modules when they are connected to their "Standard Die Rotate" Module counterparts that have same number of Advanced Package Modules.

Note: The double-ended arrows in Figure 5-36 through Figure 5-39 indicate Module-to-Module connections.

Figure 5-36. Naming Convention for One-, Two-, and Four-module Advanced Package Paired with "Standard Die Rotate" Configurations

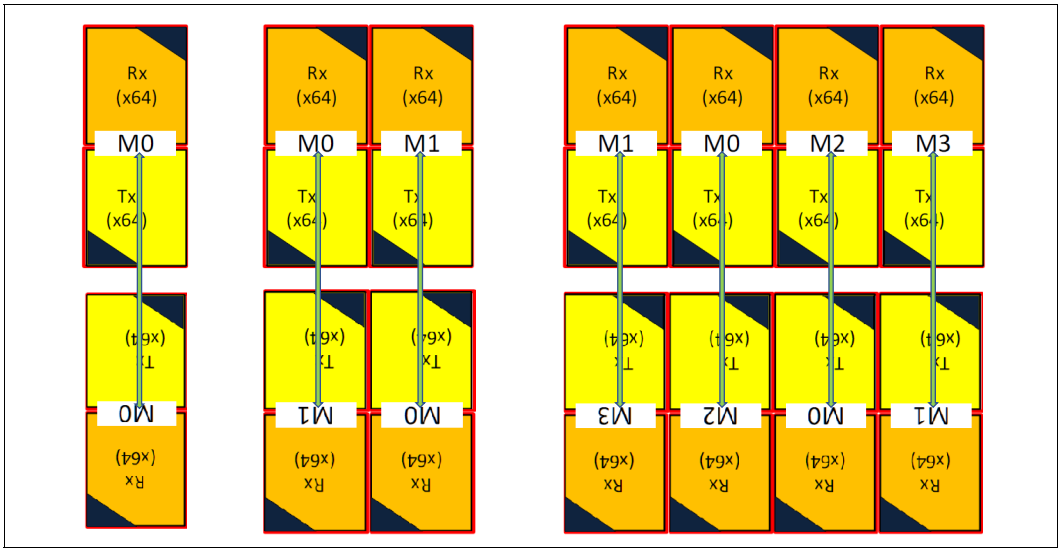


Figure 5-37 shows the naming convention for 1, 2, or 4 Advanced Package modules when they are connected to their "Mirrored Die Rotate" counterparts with the same number of Advanced Package modules.

Figure 5-37. Naming Convention for One-, Two-, and Four-module Advanced Package Paired with "Mirrored Die Rotate" Configurations

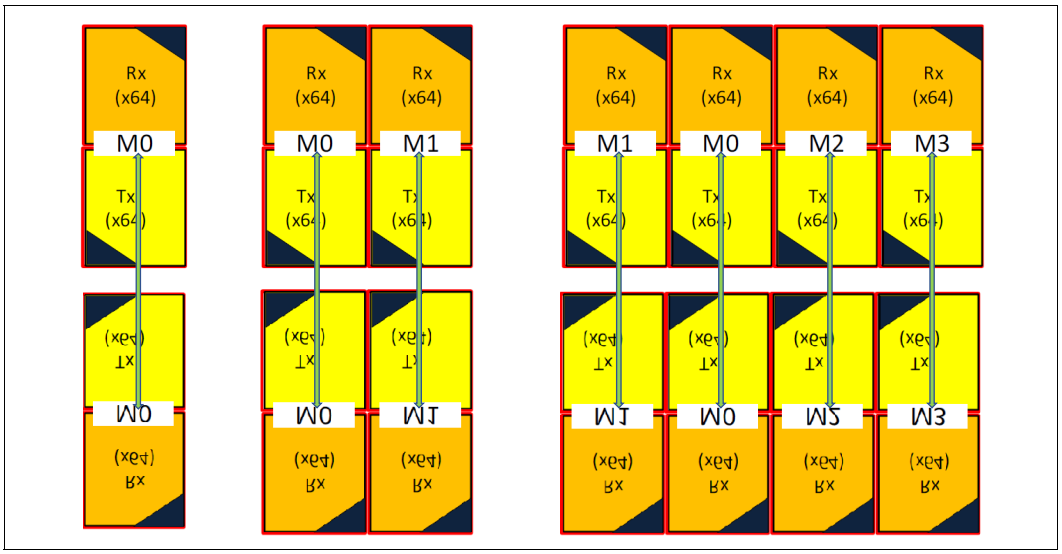


Table 5-16 summarizes the connections between the combinations shown in Figure 5-36 and Figure 5-37.

Table 5-16. Summary of Advanced Package Module Connection Combinations with Same Number of Modules on Both Sides

Advanced Package Module Connections (Same # of Modules on Both Sides)	Standard Die Rotate Counterpart	Mirrored Die Rotate Counterpart
x1 – x1	• M0 – M0	• M0 – M0
x2 – x2	• M0 – M1 • M1 – M0	• M0 – M0 • M1 – M1
x4 – x4	• M0 – M2 • M1 – M3 • M3 – M1 • M2 – M0	• M0 – M0 • M1 – M1 • M2 – M2 • M3 – M3

Figure 5-38 shows the naming convention for 1, 2, or 4 Advanced Package modules when they are connected to their "Standard Die Rotate" counterparts that have a different number of Advanced Package modules.

Figure 5-38. Examples for Advanced Package Configurations Paired with "Standard Die Rotate" Counterparts, with a Different Number of Modules

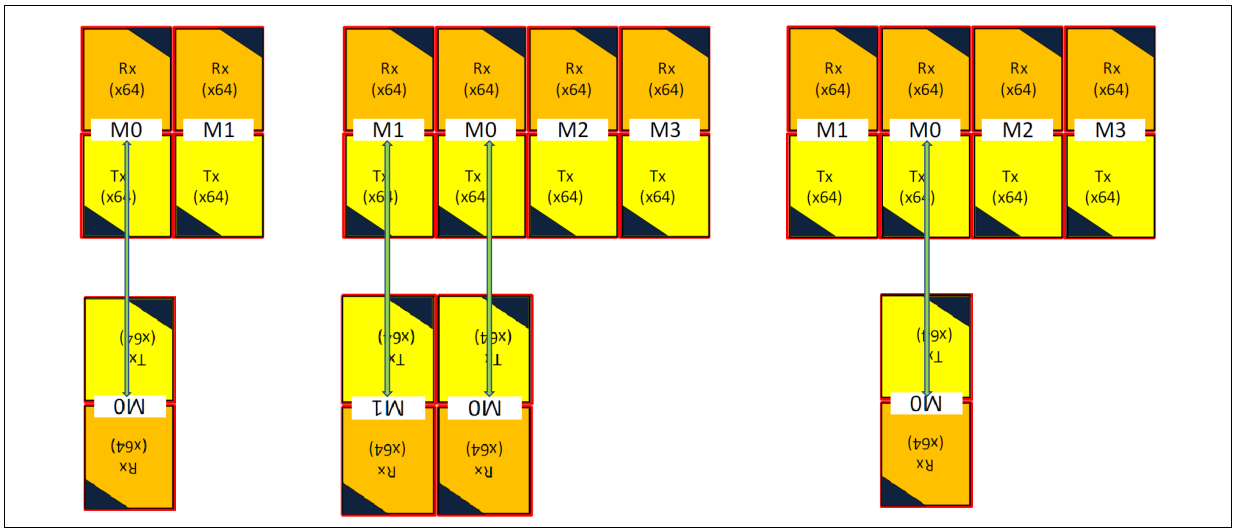


Figure 5-39 shows the naming convention for 1, 2, or 4 Advanced Package modules when they are connected to their "Mirrored Die Rotate" counterparts that have a different number of Advanced Package modules.

Figure 5-39. Examples for Advanced Package Configurations Paired with "Mirrored Die Rotate" Counterparts, with a Different Number of Modules

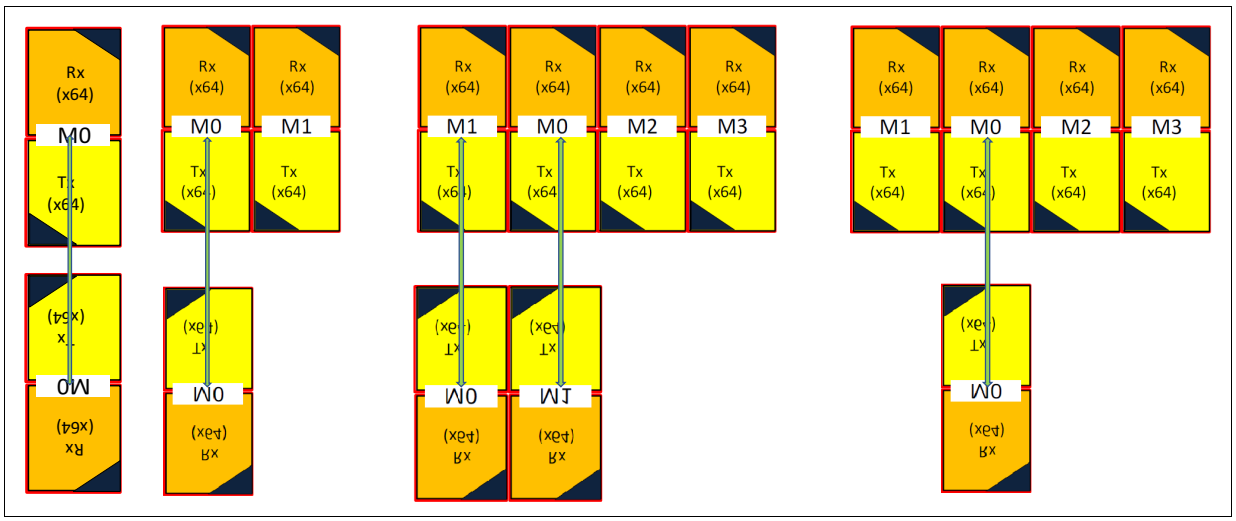


Table 5-17 summarizes the connections between the combinations shown in Figure 5-38 and Figure 5-39.

Table 5-17. Summary of Advanced Package Module Connection Combinations with Different Number of Modules on Both Sides

Advanced Package Module Connections (Different # of Modules on Both Sides)	Standard Die Rotate Counterpart[a]	Mirrored Die Rotate Counterpart[a]
x2 – x1	• M0 – M0 • M1 – NC	• M0 – M0 • M1 – NC
x4 – x2	• M0 – M0 • M1 – M1 • M3 – NC • M2 – NC	• M0 – M1 • M1 – M0 • M2 – NC • M3 – NC
x4 – x1	• M0 – M0 • M1 – NC • M3 – NC • M2 – NC	• M0 – M0 • M1 – NC • M2 – NC • M3 – NC

a. NC indicates no connection.

5.7.3 Standard Package

Interconnect channel should be designed with 50 ohm characteristic impedance. Insertion loss and crosstalk for requirement at Nyquist frequency with Receiver termination is defined in Table 5-18.

Table 5-18. IL and Crosstalk for Standard Package: With Receiver Termination Enabled

Data Rate	4, 8 GT/s	12, 16 GT/s	24, 32 GT/s
VTF Loss (dB)[a b c]	L(0) > -4.5 $L(f_N)$ > -7.5	L(0) > -4.5 $L(f_N)$ > -6.5	L(0) > -4.5 $L(f_N)$ > -7.5
VTF Crosstalk (dB)	$XT(f_N) < 3 * L(f_N) - 11.5$ and $XT(f_N) < -25$	$XT(f_N) < 3 * L(f_N) - 11.5$ and $XT(f_N) < -25$	$XT(f_N) < 2.5 * L(f_N) - 10$ and $XT(f_N) < -26$

a. Voltage Transfer Function for 4 GT/s and 8 GT/s (Tx: 30 ohm / 0.3pF; Rx: 50 ohm / 0.3pF).
b. Voltage Transfer Function for 12 GT/s and 16 GT/s (Tx: 30 ohm / 0.2pF; Rx: 50 ohm / 0.2pF).
c. Voltage Transfer Function for 24 GT/s and 32 GT/s (Tx: 30 ohm / 0.125pF; Rx: 50 ohm / 0.125pF).

IL and crosstalk for requirement at Nyquist frequency without Receiver termination is defined by Table 5-19. Loss and crosstalk specifications between DC and Nyquist f_N follow the same methodology defined in Section 5.7.2.1.

Table 5-19. IL and Crosstalk for Standard Package: No Rx Termination

Data Rate	4-12 GT/s	16 GT/s
VTF Loss (dB)[a b]	$L(f_N)$ > -1.25	$L(f_N)$ > -1.15
VTF Crosstalk (dB)	$XT(f_N) < 7 * L(f_N) - 12.5$ and $XT(f_N) < -15$	$XT(f_N) < 4 * L(f_N) - 13.5$ and $XT(f_N) < -17$

a. Voltage Transfer Function for 4 GT/s and 8 GT/s (Tx: 30 ohm / 0.3pF; Rx: 0.2 pF).
b. Voltage Transfer Function for 12 GT/s and 16 GT/s (Tx: 30 ohm / 0.2pF; Rx: 0.2 pF).

Table 5-20. Standard Package Module Signal List (Sheet 1 of 2)

Signal Name	Count	Description
Data		
TXDATA[15:0]	16	Transmit Data
TXVLD	1	Transmit Data Valid; Enables clocking in corresponding module
TXTRK	1	Transmit Track signal
TXCKP	1	Transmit Clock Phase-1
TXCKN	1	Transmit Clock Phase-2
RXDATA[15:0]	16	Receive Data
RXVLD	1	Receive Data Valid; Enables clocking in corresponding module
RXTRK	1	Receive Track
RXCKP	1	Receive Clock Phase-1
RXCKN	1	Receive Clock Phase-2
Sideband		
TXDATASB	1	Sideband Transmit Data
RXDATASB	1	Sideband Receiver Data
TXCKSB	1	Sideband Transmit Clock

Table 5-20. Standard Package Module Signal List (Sheet 2 of 2)

Signal Name	Count	Description
RXCKSB	1	Sideband Receive Clock
Power and Voltage		
VSS		Ground Reference
VCCIO		I/O supply
VCCAON		Always on Aux supply (sideband)

5.7.3.1 x16 Standard Package Module Bump Map

Figure 5-40 and Figure 5-42 show the reference bump matrices for x16 (one module) and x32 (two module) Standard Packages, respectively.

It is strongly recommended to follow the bump matrices provided in Figure 5-40 for one module and Figure 5-42 for two module Standard Packages. The lower left corner of the bump map will be considered "origin" of a bump matrix.

Signal exit order for x16 and x32 Standard Package bump matrices are shown in Figure 5-41 and Figure 5-43, respectively.

The following rules must be followed for Standard Package bump matrices:

- The signals within a column must be preserved. For example, for a x16 (one module Standard Package) shown in Figure 5-40, Column 1 must contain the signals: **txdata0**, **txdata1**, **txdata4**, **txdata5**, and **txdatasb**.
- The signals must exit the bump field in the order shown in Figure 5-41. Layer 1 and Layer 2 are two different signal routing layers in a Standard Package.

It is strongly recommended to follow the supply and **ground** pattern shown in the bump matrices. It must be ensured that sufficient supply and **ground** bumps are provided to meet channel characteristics (FEXT and NEXT) and power-delivery requirements.

The following rules must be followed for instantiating multiple modules of Standard Package bump matrix:

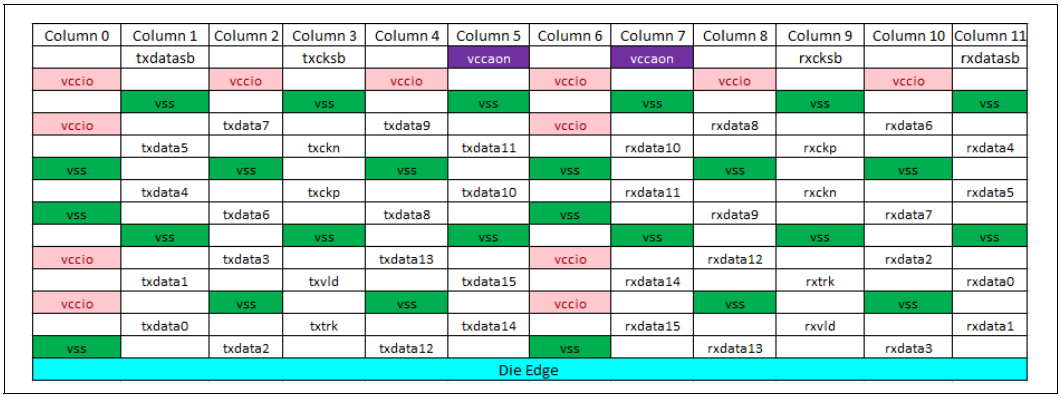
- When looking at a die such that the UCIe Modules are on the south side, Tx should always precede Rx within a module along the die's edge when going from left to right.
- When instantiating multiple modules, the modules must be stepped in the same orientation and abutted. Horizontal or vertical mirroring is not permitted.

If more Die Edge Bandwidth density is required, it is permitted to stack two modules before abutting. If two modules are stacked, the package may need to support at least four routing layers for UCIe signal routing. An example of stacked Standard Package Module instantiations is shown in Figure 5-42.

- If only one stacked module is instantiated, when looking at a die such that the UCIe Modules are on the south side, Tx should always precede Rx within a module along the die's edge when going from left to right.
- When instantiating multiple stacked modules, the modules must be stepped in the same orientation and abutted. Horizontal or vertical mirroring is not permitted.

Note: An example of signal routing for stacked module is shown in Figure 5-44.

Figure 5-40. Standard Package Bump Map: x16 interface

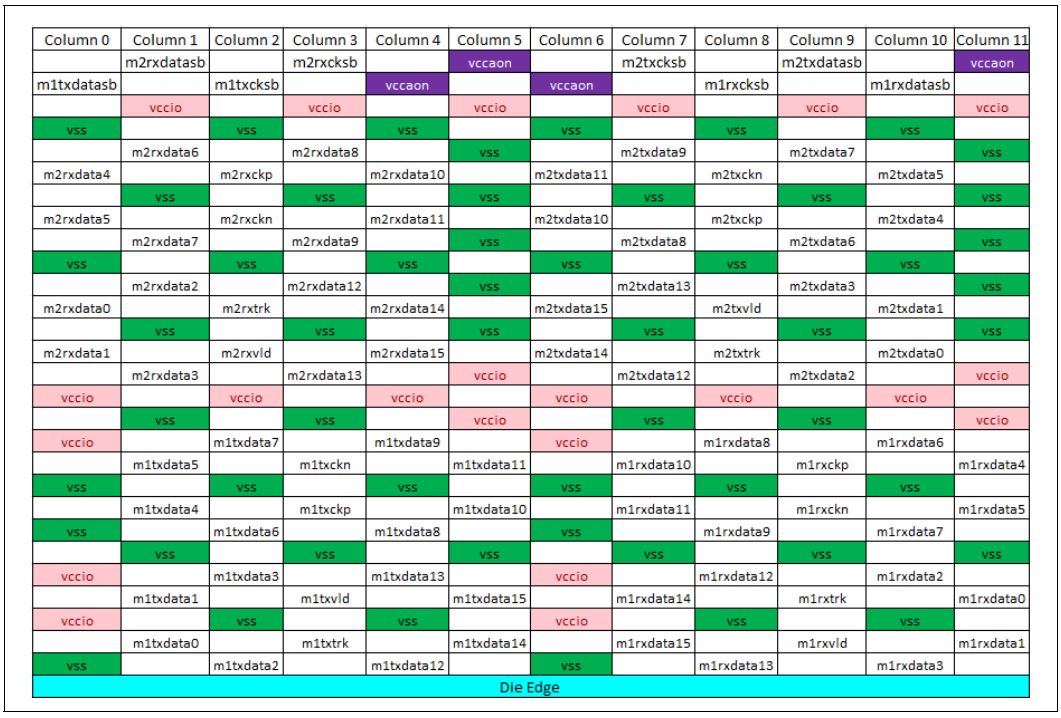


Column 0	Column 1	Column 2	Column 3	Column 4	Column 5	Column 6	Column 7	Column 8	Column 9	Column 10	Column 11
	txdatasb		txcksb		vccaon		vccaon		rxcksb		rxdatasb
vccio		vccio		vccio		vccio		vccio		vccio	
	vss		vss		vss		vss		vss		vss
vccio		txdata7		txdata9		vccio		rxdata8		rxdata6	
	txdata5		txckn		txdata11		rxdata10		rxckp		rxdata4
vss		vss		vss		vss		vss		vss	
	txdata4		txckp		txdata10		rxdata11		rxckn		rxdata5
vss		txdata6		txdata8		vss		rxdata9		rxdata7	
	vss		vss		vss		vss		vss		vss
vccio		txdata3		txdata13		vccio		rxdata12		rxdata2	
	txdata1		txvld		txdata15		rxdata14		rxtrk		rxdata0
vccio		vss		vss		vccio		vss		vss	
	txdata0		txtrk		txdata14		rxdata15		rxvld		rxdata1
vss		txdata2		txdata12		vss		rxdata13		rxdata3	
Die Edge											

Figure 5-41. Standard Package x16 interface: Signal exit order

Layer 1	Tx	0	1	2	3	trk	vld	12	13	14	15	15	14	13	12	vld	trk	3	2	1	0	Rx
Layer 2	Module	4	5	6	7	ckp	ckn	8	9	10	11	11	10	9	8	ckn	ckp	7	6	5	4	Module
Sideband		txdatasb					txcksb							rxcksb					rxdatasb			

Figure 5-42. Standard Package Bump Map: x32 interface

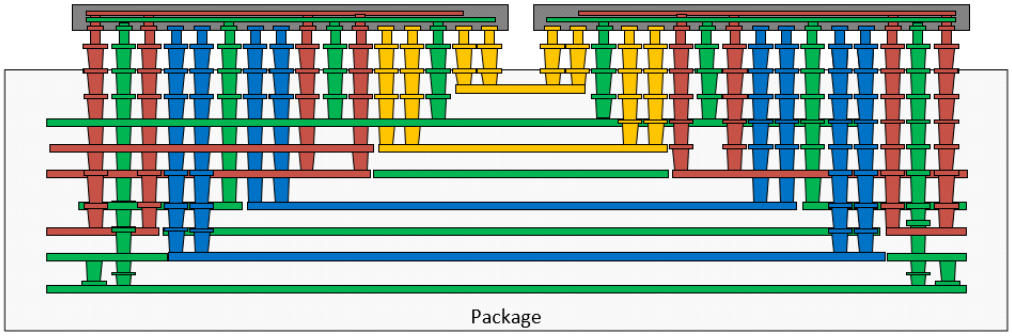


Column 0	Column 1	Column 2	Column 3	Column 4	Column 5	Column 6	Column 7	Column 8	Column 9	Column 10	Column 11
	m2rxdatasb		m2rxcksb		vccaon		m2txcksb		m2txdatasb		vccaon
m1txdatasb		m1txcksb		vccaon		vccaon		m1rxcksb		m1rxdatasb	
	vccio		vccio		vccio		vccio		vccio		vccio
vss		vss		vss		vss		vss		vss	
	m2rxdata6		m2rxdata8		vss		m2txdata9		m2txdata7		vss
m2rxdata4		m2rxckp		m2rxdata10		m2txdata11		m2txckn		m2txdata5	
	vss		vss		vss		vss		vss		vss
m2rxdata5		m2rxckn		m2rxdata11		m2txdata10		m2txckp		m2txdata4	
	m2rxdata7		m2rxdata9		vss		m2txdata8		m2txdata6		vss
vss		vss		vss		vss		vss		vss	
	m2rxdata2		m2rxdata12		vss		m2txdata13		m2txdata3		vss
m2rxdata0		m2rxtrk		m2rxdata14		m2txdata15		m2txvld		m2txdata1	
	vss		vss		vss		vss		vss		vss
m2rxdata1		m2rxvld		m2rxdata15		m2txdata14		m2txtrk		m2txdata0	
	m2rxdata3		m2rxdata13		vccio		m2txdata12		m2txdata2		vccio
vccio		vccio		vccio		vccio		vccio		vccio	
	vss		vss		vccio		vss		vss		vccio
vccio		m1txdata7		m1txdata9		vccio		m1rxdata8		m1rxdata6	
	m1txdata5		m1txckn		m1txdata11		m1rxdata10		m1rxckp		m1rxdata4
vss		vss		vss		vss		vss		vss	
	m1txdata4		m1txckp		m1txdata10		m1rxdata11		m1rxckn		m1rxdata5
vss		m1txdata6		m1txdata8		vss		m1rxdata9		m1rxdata7	
	vss		vss		vss		vss		vss		vss
vccio		m1txdata3		m1txdata13		vccio		m1rxdata12		m1rxdata2	
	m1txdata1		m1txvld		m1txdata15		m1rxdata14		m1rxtrk		m1rxdata0
vccio		vss		vss		vccio		vss		vss	
	m1txdata0		m1txtrk		m1txdata14		m1rxdata15		m1rxvld		m1rxdata1
vss		m1txdata2		m1txdata12		vss		m1rxdata13		m1rxdata3	
Die Edge											

Figure 5-43. Standard Package x32 interface: Signal exit routing

Layer 1	Tx	0	1	2	3	trk	vld	12	13	14	15	15	14	13	12	vld	trk	3	2	1	0	Rx
Layer 2	Module 1	4	5	6	7	ckp	ckn	8	9	10	11	11	10	9	8	ckn	ckp	7	6	5	4	Module 1
Layer 3	Rx	0	1	2	3	trk	vld	12	13	14	15	15	14	13	12	vld	trk	3	2	1	0	Tx
Layer 4	Module 2	4	5	6	7	ckp	ckn	8	9	10	11	11	10	9	8	ckn	ckp	7	6	5	4	Module 2
Sideband		m1txdatasb			m2rxdatasb			m1txcksb		m2rxcksb		m2txcksb		m1rxcksb		m2txdatasb			m1rxdatasb			Sideband

Figure 5-44. Standard Package cross section for stacked module

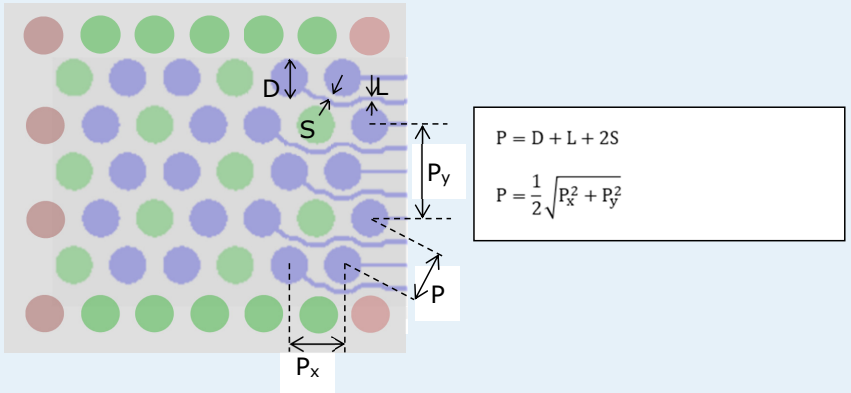


Orange – Tx signals on Die 1 talking to Rx on Die 2 in Layer 1
Orange - Tx signals on Die 1 talking to Rx on Die 2 in Layer 2
Blue - Tx signals on Die 2 talking to Rx on Die 1 in Layer 3
Blue - Tx signals on Die 2 talking to Rx on Die 1 in Layer 4
Brown – VCCIO
Green - VSS

IMPLEMENTATION NOTE

Figure 5-45 shows a breakout design reference with the Standard Package channel based on the bump pitch and on routing design rules.

Figure 5-45. Standard Package reference configuration



- 4-row deep breakout per routing layer
- Example 1: P_y = 190.5 um, P_x ≈ 111.5 um, P ≈ 110 um
- Example 2: P_y = 190.5 um, P_x ≈ 177 um, P ≈ 130 um

5.7.3.2 x8 Standard Package Module Bump Map

Designs can choose to add a UCIe-S port for sort/pre-bond test purposes in scenarios where they need the high bandwidth of UCIe, but the design is an advanced package design, or for any other reason. To reduce the chiplet's die edge when supporting such a UCIe-S usage, a x8 version of UCIe-S is provided. This is an additional option that goes beyond the available standard x16 UCIe-S port options. A UCIe-S x16 Module can optionally support connecting to a UCIe-S x8 Module and when supported, the connection is always on its lower x8 lanes (i.e., Lanes 7:0). UCIe-S x8 designs must support lane reversal and degraded mode operation to x4. UCIe-S x16 designs that support connection to a x8 Module must support lane reversal, and must support degraded mode operation to x4 on its lower 8 lanes when connected to a x8 Module.

UCIe-S x8 support is limited to a single module configuration. When a UCIe-S x8 port is connected to a multi-module x16 port, it is always connected to Module 0 UCIe-S x16.

Figure 5-46 shows the reference bump matrix for a x8 Standard Package.

Figure 5-46. Standard Package Bump Map: x8 Interface

Column 0	Column 1	Column 2	Column 3	Column 4	Column 5	Column 6	Column 7
txdatasb		txcksb		rxcksb		rxdatasb	
	vccio		vccio		vccio		vccio
vss		vss		vss		vss	
	Txdata0		Txdata7		Rxdata6		Rxdata1
vss		Txckn		vss		Rxckp	
	vss		vss		vss		vss
vccio		Txckp		vccio		Rxckn	
	Txdata1		Txdata6		Rxdata7		Rxdata0
vccio		vss		vccio		vss	
	Txdata3		Txdata4		Rxdata5		Rxdata2
vccio		Txvld		vccio		Rxtrk	
	vss		vss		vss		vss
vss		Txtrk		vss		Rxvld	
	Txdata2		Txdata5		Rxdata4		Rxdata3
Die Edge							

It is strongly recommended to follow the bump matrix provided in Figure 5-46. The lower left corner of the bump map will be considered "origin" of a bump matrix.

The same rules as mentioned for x16 and x32 Standard Package bump matrices in Section 5.7.3.1 must be followed for the x8 bump matrix.

5.7.3.3 x16 and x8 Standard Package Module Interoperability

A x8 bump matrix will either connect to another x8 bump matrix or to bits [7:0] of a x16 bump matrix.

5.7.3.4 Module Naming of Standard Package Modules

This section describes the Module naming convention of Standard Package Modules in a multi-module configuration.

The naming of M0, M1, M2, and M3 will apply to 1, 2, or 4 Standard Package modules that are aggregated through MMPL, in stacked and unstacked configuration combinations.

Figure 5-47 shows the naming convention for 1, 2, or 4 Standard Package modules when they are connected to their "Standard Die Rotate" module counterparts with the same number of Standard Package modules, with either same stack or same unstacked configuration.

Note: The double-ended arrows in Figure 5-47 through Figure 5-51 indicate Module-to-Module connections.

Figure 5-47. Naming Convention for One-, Two-, and Four-module Standard Package Paired with "Standard Die Rotate" Configurations

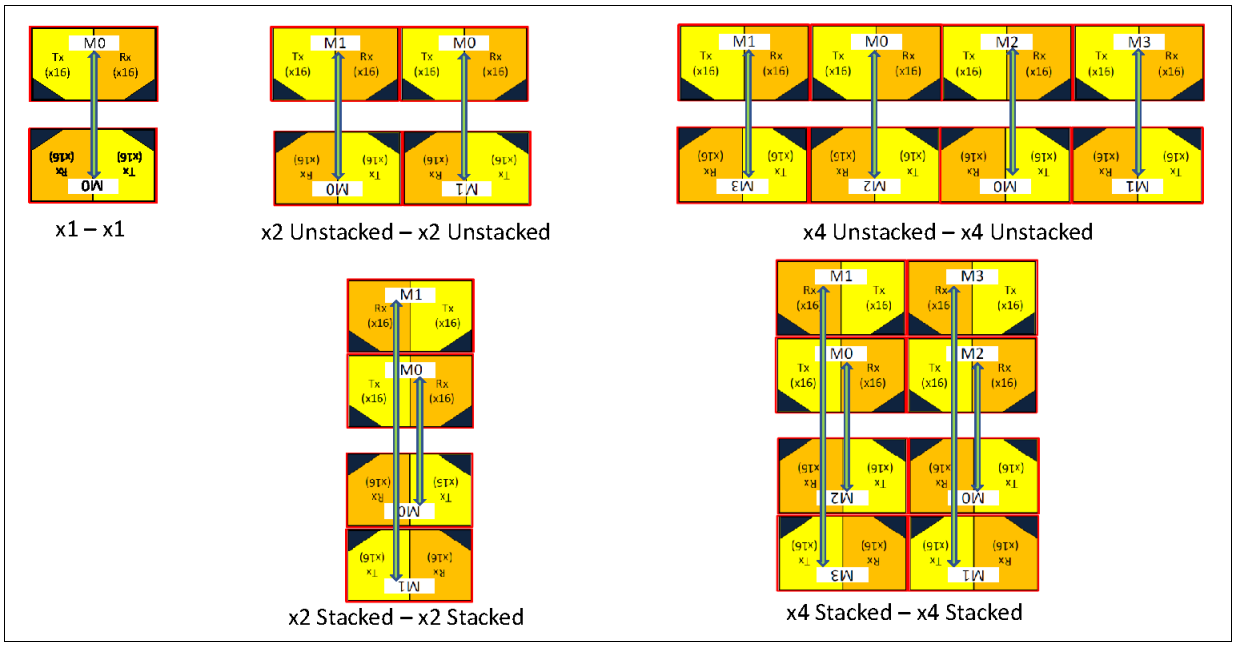


Figure 5-48 shows the naming convention for 1, 2, or 4 Standard Package modules when they are connected to their "Mirrored Die Rotate" counterparts that have same number of Standard Package modules, with either same stack or same unstacked configuration.

Figure 5-48. Naming Convention for One-, Two-, and Four-module Standard Package Paired with "Mirrored Die Rotate" Configurations

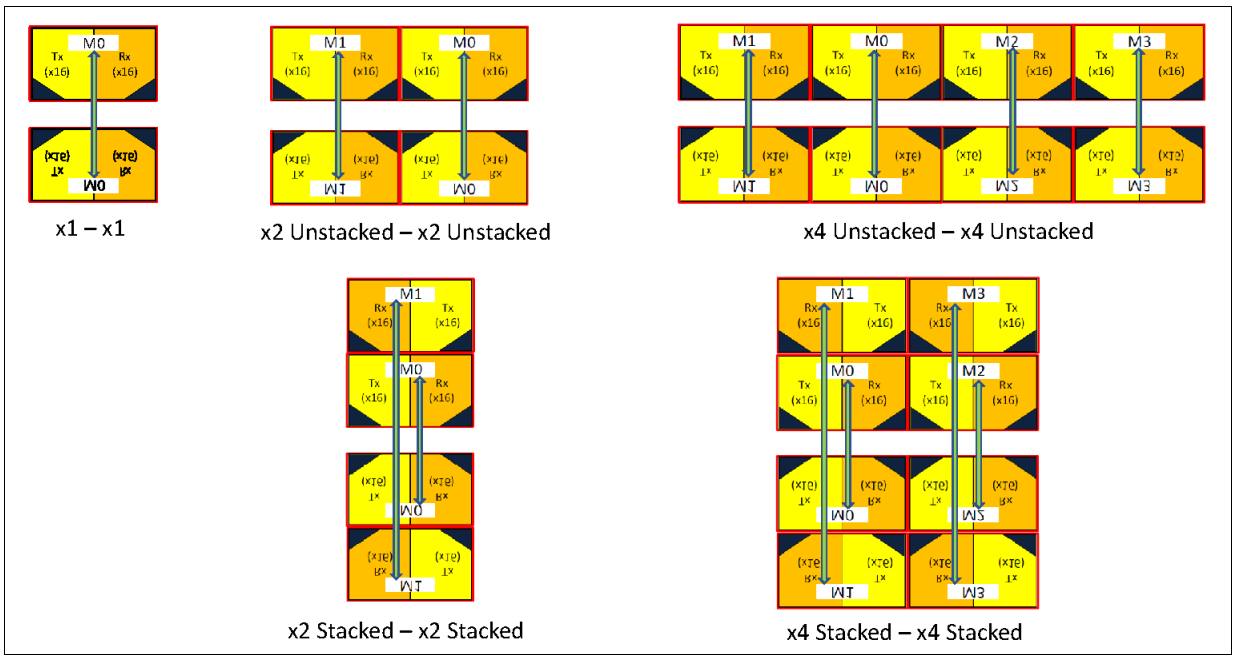


Table 5-21 summarizes the connections between the combinations shown in Figure 5-47 and Figure 5-48.

Table 5-21. Summary of Standard Package Module Connection Combinations with Same Number of Modules on Both Sides [a] [b]

Standard Package Module Connections (Same # of Modules on Both Sides)	Standard Die Rotate Counterpart	Mirrored Die Rotate Counterpart	
		Option 1 (See Figure 5-48)	Option 2[c] (See Figure 5-51)
x1 – x1	• M0 – M0	• M0 – M0	
x2 Unstacked – x2 Unstacked	• M0 – M1 • M1 – M0	• M0 – M0 • M1 – M1	
x2 Stacked – x2 Stacked	• M0 – M0 • M1 – M1	• M0 – M0 • M1 – M1	• M0 – M1 • M1 – M0
x4 Unstacked – x4 Unstacked	• M0 – M2 • M1 – M3 • M3 – M1 • M2 – M0	• M0 – M0 • M1 – M1 • M2 – M2 • M3 – M3	
x4 Stacked – x4 Stacked	• M0 – M2 • M1 – M3 • M3 – M1 • M2 – M0	• M0 – M0 • M1 – M1 • M2 – M2 • M3 – M3	• M0 – M1 • M1 – M0 • M2 – M3 • M3 – M2

a. Mirror-to-Mirror connection will be same as non-mirrored case.
b. Mirror die connectivity may have jogs and need additional layers on package.

c. For some mirrored cases, there are possible alternative connections to allow design choices between more routing layers vs. max data rates, shown as Option 1 and Option 2 in Table 5-21. For x2 – x2 Stacked and x4 – x4 Stacked cases, Option 1 typically requires 2x the routing layers and enables nominal data rates, while Option 2 enables same the layer count but at reduced max data rates due to potential crosstalk. See Figure 5-50 for Option 2 connection illustrations.

Figure 5-49 shows the naming convention for 1, 2, or 4 Standard Package modules when they are connected to their "Standard Die Rotate" counterparts that have a different number of Standard Package modules.

Figure 5-49. Examples for Standard Package Configurations Paired with "Standard Die Rotate" Counterparts, with a Different Number of Modules

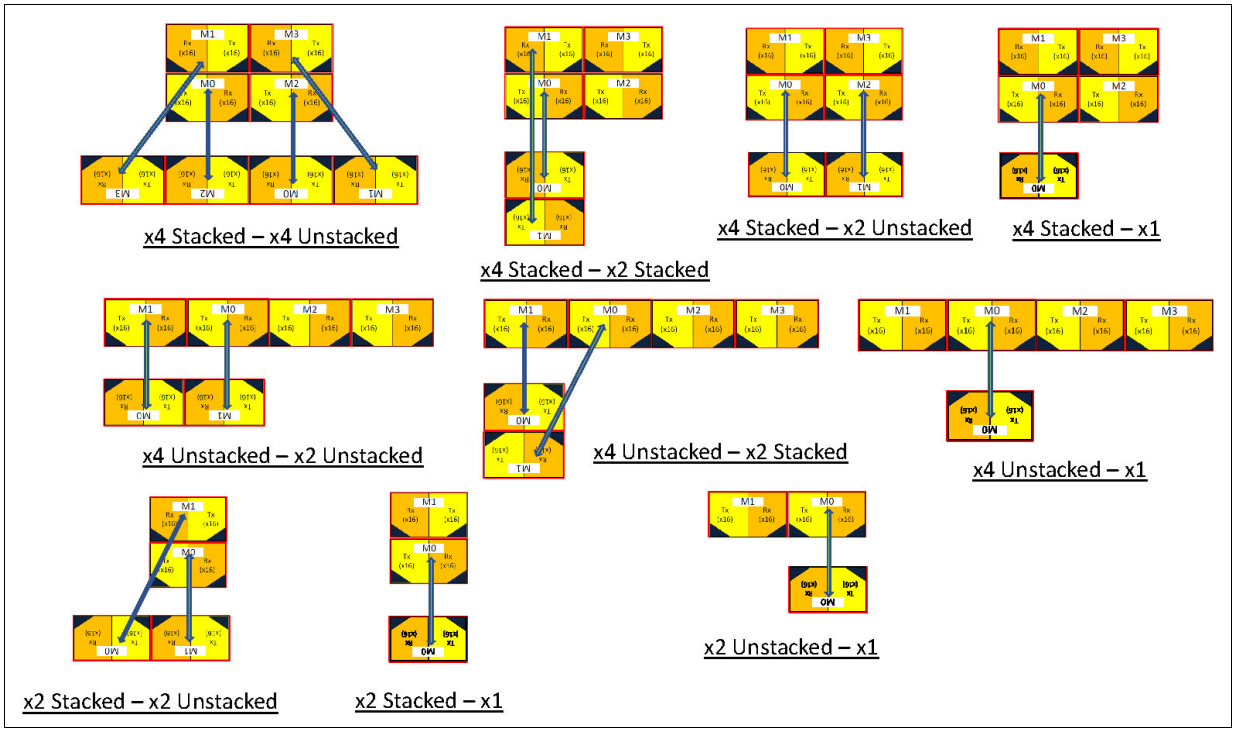


Figure 5-50 shows the naming convention for 1, 2, or 4 Standard Package Modules when they are connected to their "Mirrored Die Rotate" counterparts that have a different number of Standard Package Modules.

Figure 5-50. Examples for Standard Package Configurations Paired with "Mirrored Die Rotate" Counterparts, with a Different Number of Modules

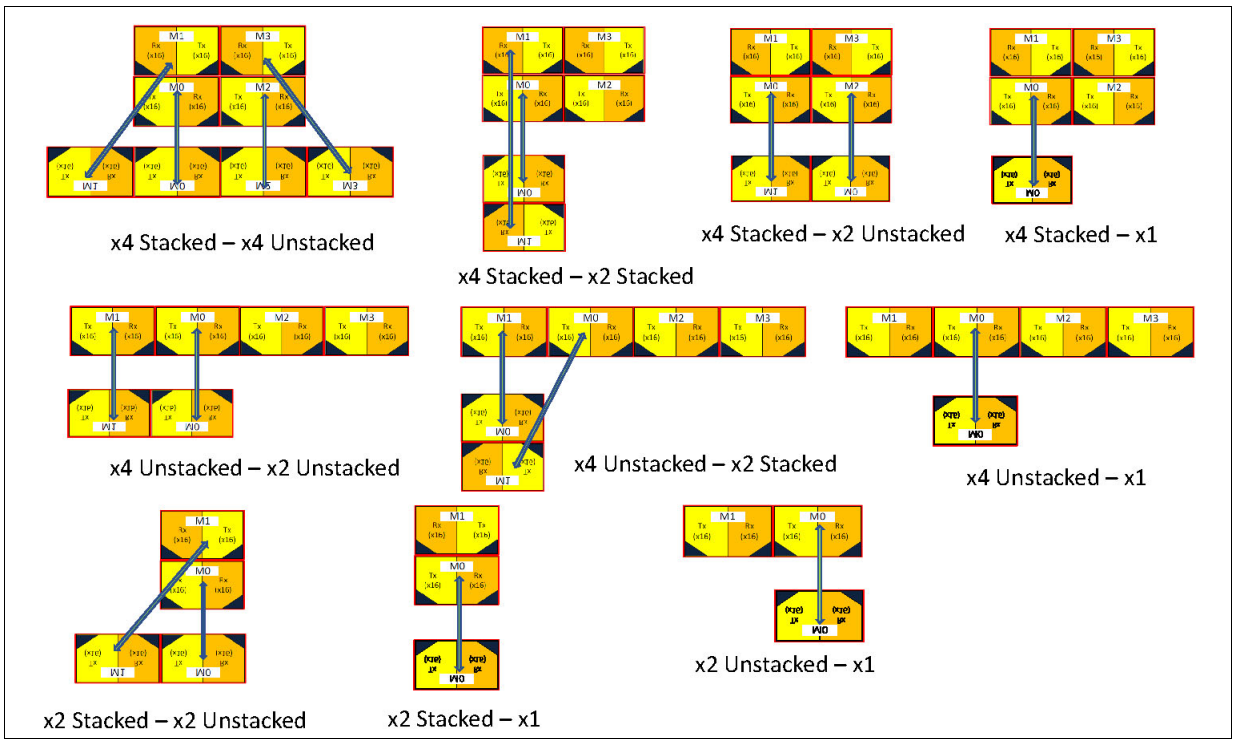


Figure 5-51 illustrates the possible alternative connections for some mirrored cases to allow design choices between more routing layers vs. reduced max data rates due to potential crosstalk, shown as Option 2 in Table 5-21 and Table 5-22.

Figure 5-51. Additional Examples for Standard Package Configurations Paired with "Mirrored Die Rotate" Counterparts, with a Different Number of Modules

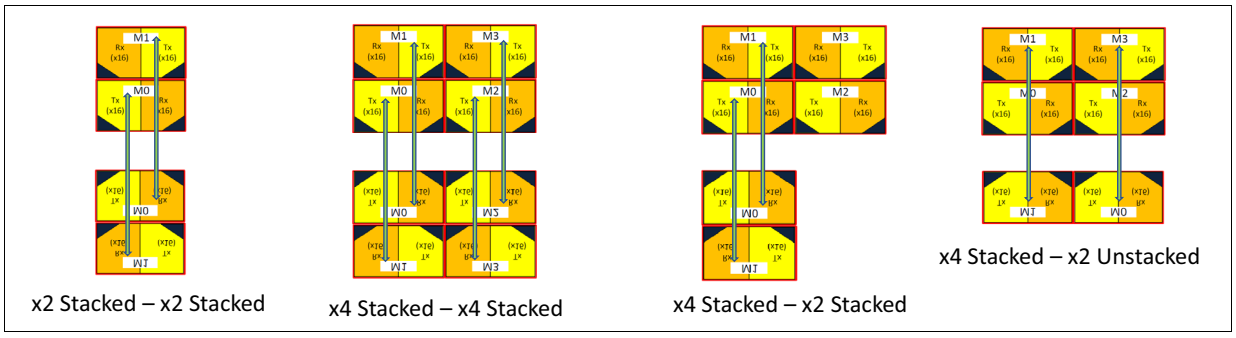


Table 5-22 summarizes the connections between the combinations shown in Figure 5-49, Figure 5-50, and Figure 5-51.

5.7.3.4.1 Module Degrade Rules

Table 5-22. Summary of Standard Package Module Connection Combinations with Different Number of Modules on Both Sides

Standard Package Module Connections (Different # of Modules on Both Sides)	Standard Die Rotate Counterpart[a]	Mirrored Die Rotate Counterpart[a]	
		Option 1 (See Figure 5-50)	Option 2 (See Figure 5-51)
x4 Stacked – x4 Unstacked	• M0 – M2 • M1 – M3 • M3 – M1 • M2 – M0	• M0 – M0 • M1 – M1 • M2 – M2 • M3 – M3	
x4 Stacked – x2 Stacked	• M0 – M0 • M1 – M1 • M3 – NC • M2 – NC	• M0 – M0 • M1 – M1 • M2 – NC • M3 – NC	• M0 - M1 • M1 - M0 • M2 – NC • M3 – NC
x4 Stacked – x2 Unstacked	• M0 – M0 • M1 – NC • M3 – NC • M2 – M1	• M0 – M1 • M1 – NC • M2 – M0 • M3 - NC	• M0 – NC • M1 – M1 • M2 – NC • M3 – M0
x4 Stacked – x1	• M0 – M0 • M1 – NC • M3 – NC • M2 – NC	• M0 – M0 • M1 – NC • M3 – NC • M2 – NC	
x4 Unstacked – x2 Unstacked	• M0 – M1 • M1 – M0 • M3 – NC • M2 – NC	• M0 – M0 • M1 – M1 • M2 – NC • M3 – NC	
x4 Unstacked – x2 Stacked	• M0 – M1 • M1 – M0 • M3 – NC • M2 – NC	• M0 – M1 • M1 – M0 • M2 – NC • M3 – NC	
x4 Unstacked – x1	• M0 – M0 • M1 – NC • M3 – NC • M2 – NC	• M0 – M0 • M1 – NC • M3 – NC • M2 – NC	
x2 Stacked – x2 Unstacked	• M0 – M1 • M1 – M0	• M0 – M0 • M1 – M1	
x2 Stacked – x1	• M0 – M0 • M1 – NC	• M0 – M0 • M1 – NC	
x2 Unstacked – x1	• M0 – M0 • M1 – NC	• M0 – M0 • M1 – NC	

a. NC indicates no connection.

On a 2-module or 4-module link, if one or more module-pairs have failed, the link will be degraded and shall comply with the following rules:

1. The degraded link shall be either one or two modules, and shall not be three modules.
   a. For a 4-module link:
      i. If any one module-pair failed, it shall be degraded to a 2-module link.

ii. If any two module-pairs failed, it shall be degraded to a 2-module link.

iii. If any three module-pairs failed, it shall be degraded to a 1-module link.

b. For a 2-module link:

i. If any one module-pair failed, it shall be degraded to a 1-module link.

2. For a 4-module link, if only one module-pair failed, one additional module-pair that belongs to the "same half" (along the Die Edge) of the 4-module will be disabled/degraded.

Figure 5-52 illustrates an example with a x4 Unstacked connected to a x4 Unstacked "Standard Die Rotate" counterpart with one M0 – M2 pair failed. The M1 – M3 pair on its left shall be disabled accordingly to comply with the rules defined above, which will be denoted as "x (d)" in Table 5-23.

Note: The double-ended arrows in Figure 5-52 indicate Module-to-Module connections.

Figure 5-52. Example of a Configuration for Standard Package, with Some Modules Disabled

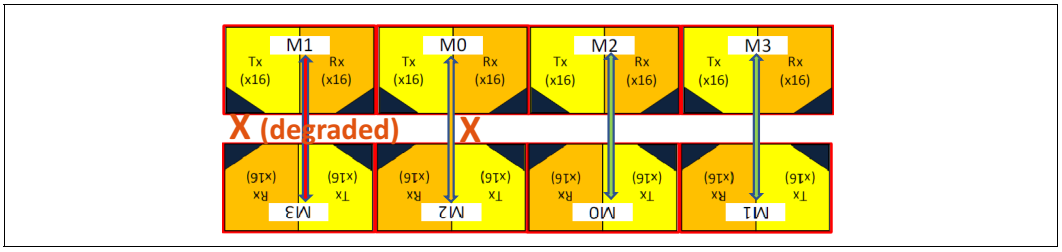


Table 5-23 summarizes the resulting degraded link if there are one, two, or three failed module-pairs for the x4 Unstacked to x4 Unstacked configuration.

Table 5-23. Summary of Degraded Links when Standard Package Module-pairs Fail

Module – Module Partner Pair	Number of Module-pairs Failed[a]													
	1-fail				2-fail						3-fail			
M0 – M2	x	x (d)	✓	✓	x	x	x	✓	✓	✓	x	x	x	✓
M1 – M3	x (d)	x	✓	✓	x	✓	✓	x	x	✓	x	x	✓	x
M3 – M1	✓	✓	x	x (d)	✓	x	✓	x	✓	x	x	✓	x	x
M2 – M0	✓	✓	x (d)	x	✓	✓	x	✓	x	x	✓	x	x	x

a. x = Failed Module – Module Partner Pair.
x (d) = Disabled Module – Module Partner Pair to comply with Degrade rules.
✓ = Functional Module – Module Partner Pair.

All other module configurations shall follow the same Module Degrade rules as defined above.

5.7.4 UCIe-S Sideband-only Port

A UCIe-S sideband-only port is also permitted for test/manageability purposes. The RDI signals to the sideband port for a sideband-only configuration are the same as for a sideband with mainband configuration (see Chapter 10.0 for details of the latter).

Figure 5-53 shows the bump map for a UCIe-S sideband-only port. Figure 5-54 shows the supported configurations for a UCIe-S sideband-only port.

Figure 5-53. UCIe-S Sideband-only Port Bump Map

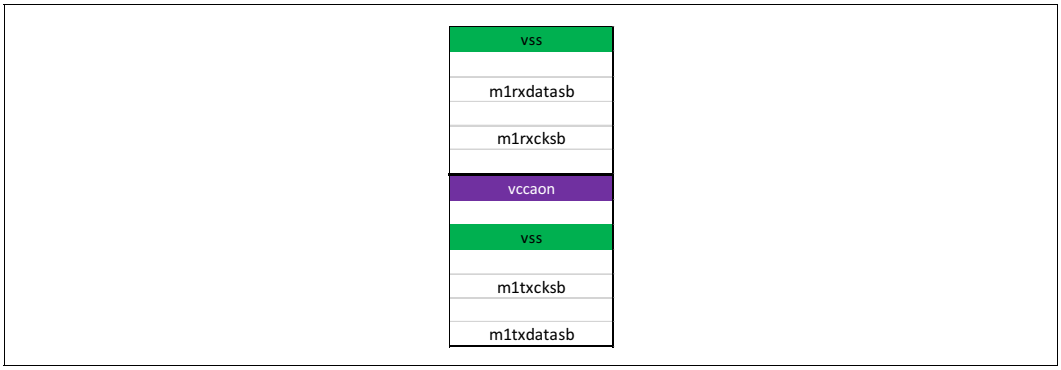
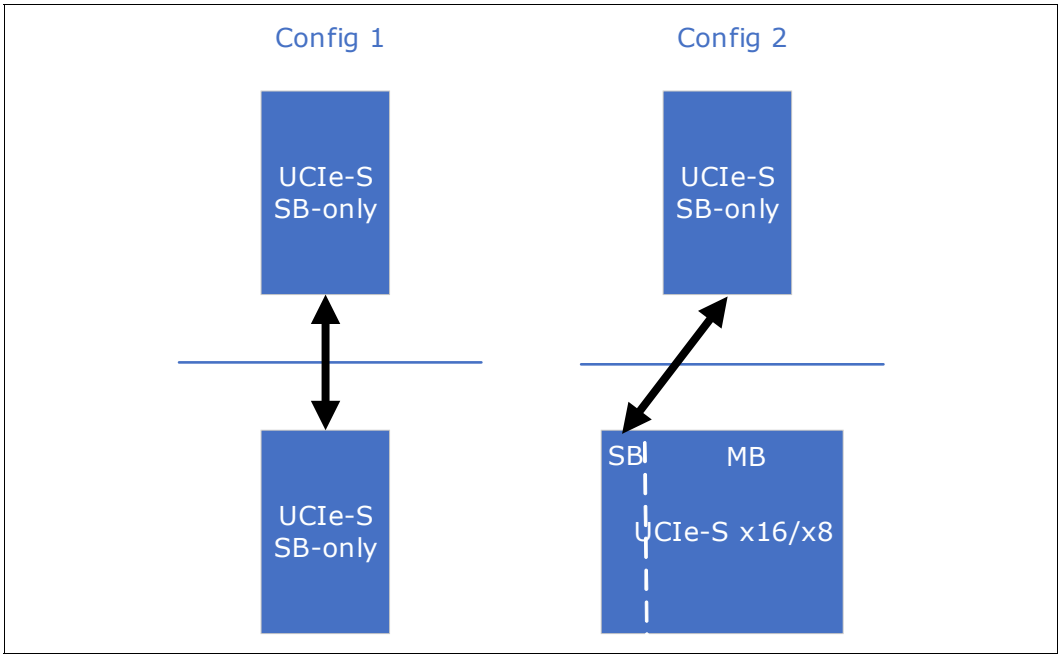


Figure 5-54. UCIe-S Sideband-only Port Supported Configurations



5.8 Tightly Coupled Mode

Tightly Coupled PHY mode is defined as when both of the following conditions are met:

- Shared Power Supply between Tx and Rx, or Forwarded Power Supply from Tx to Rx
- Channel supports larger eye mask defined in Table 5-24

In this mode, there is no Receiver termination and the Transmitter must provide full swing output. In this mode, further optimization of PHY circuit and power reduction is possible. For example, a tuned inverter can potentially be used instead of a front-end amplifier. Training complexity such as voltage reference can be simplified.

Table 5-24. Tightly Coupled Mode: Eye Mask

Data Rate	4-16 GT/s
Overall (Eye Closure due to Channel)[a]	
Eye Height[b]	250 mV
Eye Width (rectangular eye mask with specified eye height)	0.7 UI

a. With 750-mV Transmitter signal swing.
b. Centered around VCCFWDIO/2.

Loss and crosstalk requirement follow the same VTF method, adjusting to the eye mask defined in Table 5-24. Table 5-25 shows the specification at Nyquist frequency.

Table 5-25. Tightly Coupled Mode Channel for Advanced Package

Data Rate	4-12 GT/s	16 GT/s
VTF Loss[a] (dB)	$L(f_N) > -3$	-
VTF Crosstalk[a] (dB)	$XT(f_N) < 1.5 * L(f_N) - 21.5$ and $XT(f_N) < -23$	-

a. Based on Voltage Transfer Function (Tx: 25 ohm / 0.25 pF; Rx: 0.2 pF).

Loss and crosstalk specifications between DC and Nyquist f_N follow the same methodology defined in Section 5.7.2.1.

Although the use of this mode is primarily for Advanced Package, it may also be used for Standard Package when two Dies are near one another and Receiver must be unterminated.

5.9 Interconnect redundancy Remapping

5.9.1 Advanced Package Lane Remapping

Interconnect Lane remapping is supported in Advanced Package Module to improve assembly yield and recover functionality. Each module supports:

- Four redundant bumps for Data
- One redundant bump for Clock and Track
- One redundant bump for Valid

For x64 Advanced Package modules, the four redundant bumps for data repair are divided into two groups of two. Figure 5-55 shows an illustration of x64 Advanced package module redundant bump assignment for data signals. TRD_P0 and TRD_P1 are allocated to the lower 32 data Lanes and TRD_P2 and TRD_P3 are allocated to the upper 32 data Lanes. Each group is permitted to remap up

to two Lanes. For example, TD15 is a broken Lane in the lower half and TD_P32 and TD_P40 are broken Lanes in the upper 32 Lanes. Figure 5-56 illustrates Lane remapping for the broken Lanes.

For x32 Advanced Package modules, only the lower 32 data lanes and TRD_P0 and TRD_P1 apply in Figure 5-55 and Figure 5-56.

Details and implementation of Lane remapping for Data, Clock, Track, and Valid are provided in Section 4.3.

Figure 5-55. Data Lane repair resources

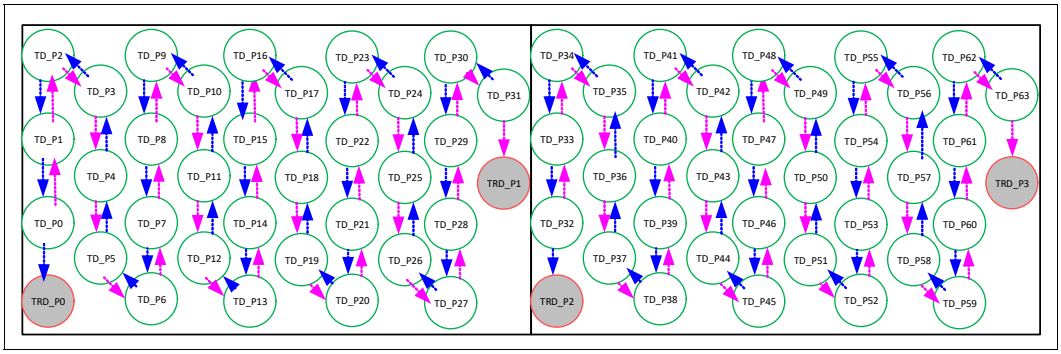
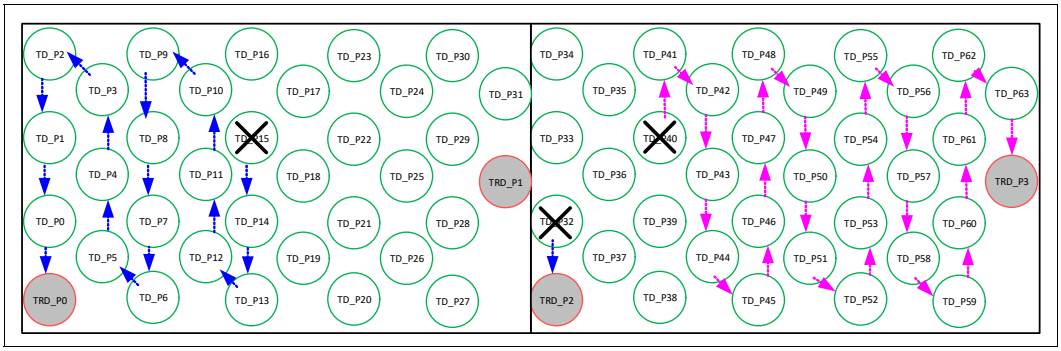


Figure 5-56. Data Lane repair



5.9.2 Standard Package Lane remapping

Lane repair is not supported in Standard Package modules.

5.10 BER requirements, CRC and retry

The BER requirement based on channel reach defined in Section 5.7 is shown in Table 5-26. Error detection and correction mechanisms such as CRC and retry are required for BER for 1E-15 to achieve the required Failure In Time (FIT) rate of significantly less than 1 (1 FIT = 1 device failure in 10^9 Hours). The UCIe spec defined CRC and retry is detailed in Chapter 3.0. For the BER of 1E-27, either parity or CRC can be used and the appropriate error reporting mechanism must be invoked to ensure a FIT that is significantly less than 1.

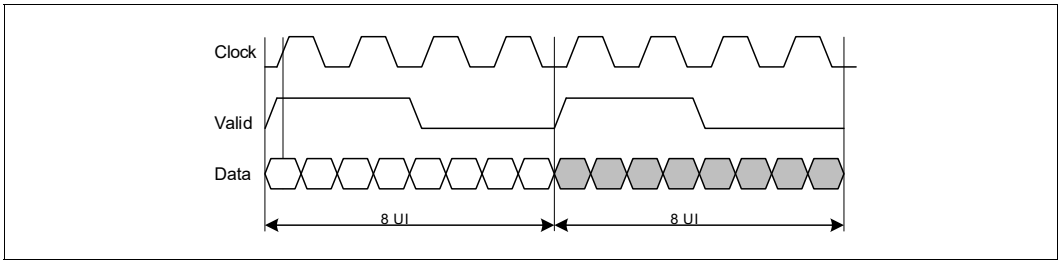
Table 5-26. Raw BER requirements

Package Type	Data Rate (GT/s)					
	4	8	12	16	24	32
Advanced Package	1E-27	1E-27	1E-27	1E-15	1E-15	1E-15
Standard Package	1E-27	1E-27	1E-15	1E-15	1E-15	1E-15

5.11 Valid and Clock Gating

Valid is used to frame transmit data. For a single transmission of 8 UI data packet, Valid is asserted for the first 4 UI and de-asserted for the second 4 UI. Figure 5-57 shows the transfer of two 8 UI data packets back to back.

Figure 5-57. Valid Framing



As described in Section 4.1.3, clock must be gated only after Valid signal remains low for 16 UI (8 cycles) of postamble clock for half-rate clocking and 32 UI (8 cycles) of postamble clock for quarter-rate clocking, unless free running clock mode is negotiated.

Idle state is when there is no data transmission on the mainband. During Idle state, Data, Clock, and Valid Lanes must hold values as follows:

- If the Link is unterminated (all Advanced Package and unterminated Standard Package Links), some Data Lane Transmitters are permitted to remain toggling up to the same transition density as the scrambled data without advancing the scrambler state. The remaining Data Lane Transmitters must hold the data of the last transmitted bit. Valid Lane must be held low until the next normal transmission.
  - In Strobe mode, the clock level in a clock-gated state for half-rate clocking (after meeting postamble requirement) must alternate between differential high and differential low during consecutive clock-gating events. For quarter-rate clocking, the clock level in a clock-gated state must alternate between high and low for both phases (Phase-1 and Phase-2) simultaneously. Clock must drive a differential (simultaneous) low for half- (quarter-) rate clocking for at least 1 UI or a maximum of 8 UI before normal operation. The total clock-gated period must be an integer multiple of 8 UI. Example shown in Figure 5-58 and Figure 5-59.
  - In Continuous mode, the clock remains free running (examples shown in Figure 5-60). Total idle period must be an integer multiple of 8 UI.

Figure 5-58. Data, Clock, Valid Levels for Half-rate Clocking: Clock-gated Unterminated Link

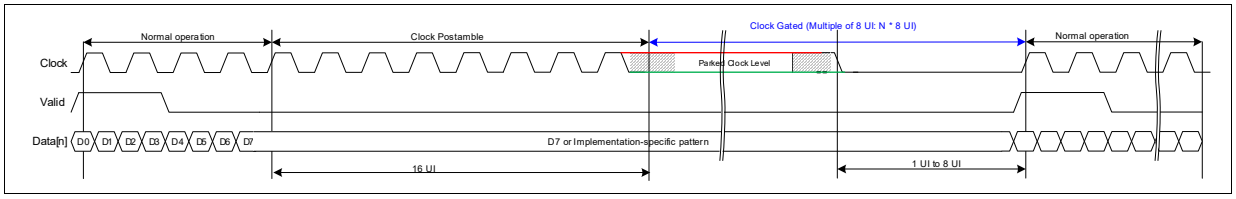


Figure 5-59. Data, Clock, Valid Levels for Quarter-rate Clocking: Clock-gated Unterminated Link

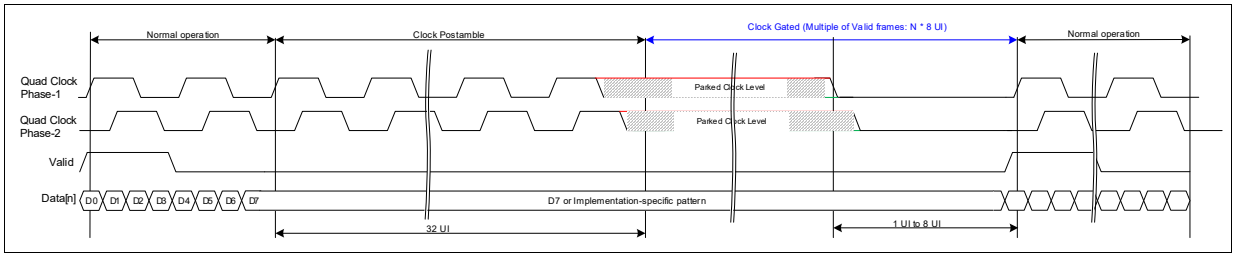
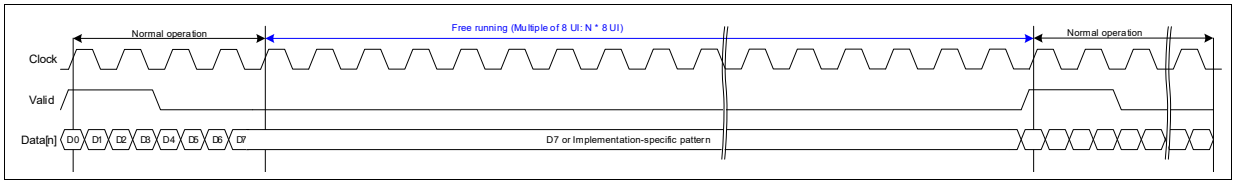


Figure 5-60. Data, Clock, Valid Levels for Half-rate Clocking: Continuous Clock Unterminated Link



- If the Link is terminated (Standard Package terminated Links), some Data Lane Transmitters are permitted to remain toggling up to the same transition density as the scrambled data without advancing the scrambler state. The remaining Data Lanes Transmitters hold the data of the last-transmitted bit. Valid Lane must be held low until the next normal transmission. Note that keeping the transmitter toggling will incur extra power penalty and should be applied with discretion.
  - In Strobe mode, the clock level in a clock-gated state for half-rate clocking (after meeting postamble requirement) must alternate between differential high and differential low during consecutive clock-gating events. For quarter-rate clocking, the clock level in a clock-gated state must alternate between high and low for both phases (Phase-1 and Phase-2) simultaneously. Transmitters must precondition the Data Lanes to a 0 or 1 (V) and clock must drive a differential low for at least 1 UI or up to a maximum of 8 UIs for half- (quarter-) rate clocking before the normal transmission. The total clock-gated period must be an integer multiple of 8 UI. Example shown in Figure 5-61 and Figure 5-63.
  - In Continuous mode, the clock remains free running (examples shown in Figure 5-64). Transmitters must precondition the Data Lanes to a 0 or 1 (V) for at least 1 UI or up to a maximum of 8 UI. Total idle period must be an integer multiple of 8 UI.

Note: Entry into and Exit from Hi-Z state are analog transitions. Hi-Z represents Transmitter state and the actual voltage during this period will be pulled Low due to termination to **ground** at the Receiver.

Figure 5-61. Data, Clock, Valid Gated Levels for Half-rate Clocking: Terminated Link

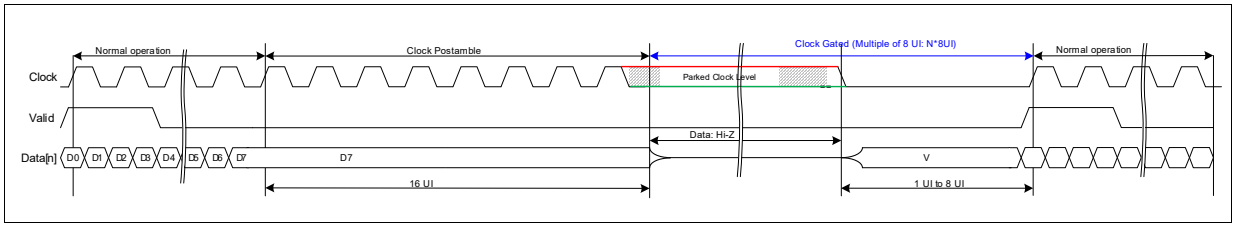


Figure 5-62. Data, Clock, Valid Gated Levels for Quarter-rate Clocking: Terminated Link

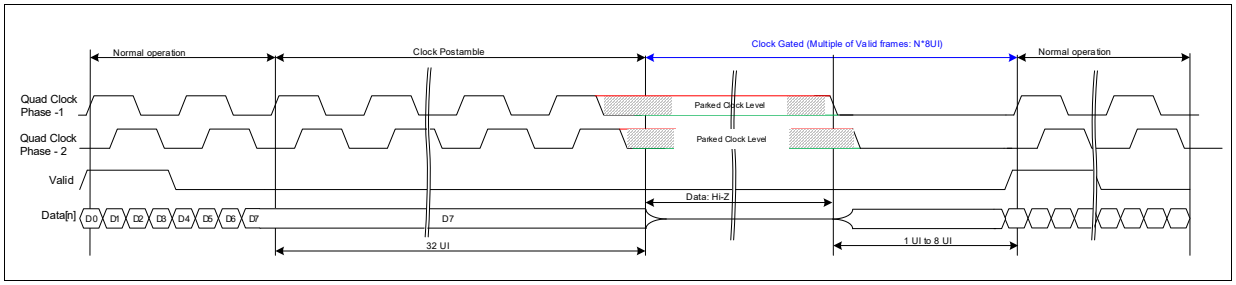
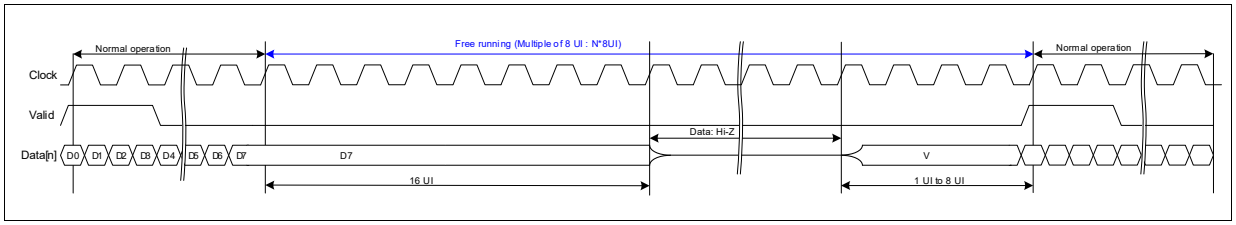


Figure 5-63. Data, Clock, Valid Gated Levels for Half-rate Clocking: Continuous Clock Terminated Link



5.12 Electrical Idle

Some training states need electrical idle when Transmitters and Receivers are waiting for generate and receive patterns.

- Electrical idle on the mainband in this Specification is described as when Transmitters and Receivers are enabled; Data, Valid and Track Lanes are held low and Clock is parked at high and low.

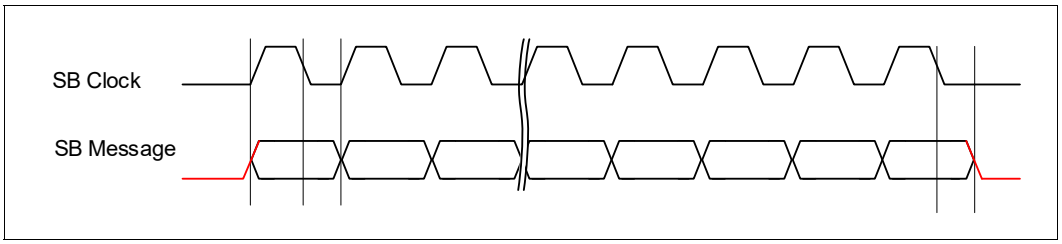
5.13 Sideband signaling

Each module supports a sideband interface. The sideband is a two-signal interface that is used for the transmit and receive directions. The sideband data is an 800 MT/s single data rate signal with an 800-MHz source. Sideband must run on power supply and clock derived from the auxiliary clock (AUXCLK) source which are always on (VCCAON). See Section 5.13.2 for AUXCLK details.

Sideband data is sent edge aligned with the positive edge of the strobe. The Receiver must sample the incoming data with the strobe. The negative edge of the strobe is used to sample the data as the data uses single data rate signaling as shown in Figure 5-64. Sideband transmission is described in Section 4.1.5.

For Advanced Package modules, redundancy is supported for the sideband interface. Sideband initialization and repair are described in Section 4.5.3.2. There is no redundancy and no Lane repair support on Standard Package modules.

Figure 5-64. Sideband signaling



5.13.1 Sideband Electrical Parameters

Table 5-27 shows the sideband electrical parameters.

It is strongly recommended that the two sides of the sideband I/O Link share the same power supply rail.

Table 5-27. Sideband Parameters summary

Parameter	Min	Typ	Max	Unit
Supply voltage (VCCAON)[a]	0.65			V
TX Swing	0.8*VCCAON	-	-	V
Input high voltage (V_{IH})	0.7*VCCAON			V
Input low voltage (V_{IL})			0.3*VCCAON	V
Output high voltage (V_{OH})	0.9*VCCCAON			V
Output low voltage (V_{OL})			0.1*VCCAON	V
Sideband Data Setup Time	200	-	-	ps
Sideband Data Hold Time	200	-	-	ps
Rise/Fall time for Advanced Package[b]	50	-	280	ps
Rise/Fall time for Standard Package[c]	80	-	175	ps

a. Always On power supply. The guidelines for maximum Voltage presented in Section 1.5 apply to sideband signaling.
b. 20 to 80% of VCCAON level with Advanced Package reference channel load.
c. 20 to 80% of VCCAON level with Standard Package reference channel load.

5.13.2 Auxiliary Clock (AUXCLK)

Auxiliary clock (AUXCLK) may be from any clock source. Although other clock frequencies are possible, it is recommended that every chiplet should also use a 100-MHz clock source. Table 5-28 lists the permitted auxiliary clock frequency range. The minimum and maximum frequencies listed in the table indicate the limits, and do not indicate a requirement to support the entire frequency range. Reference clock (REFCLK; see Section 5.1.2) can be used if it is always on. Spread-Spectrum Clocking (SSC) is permitted. AUXCLK has reduced tolerances compared to REFCLK.

Table 5-28. AUXCLK Frequency Parameters

Symbol	Description	Limits			Unit	Notes
		Min	Rec	Max		
F_{AUXCLK}	AUXCLK Frequency	25	100	800	MHz	

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