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2012.07.14 am.10:15 Lab 303

培训内容：

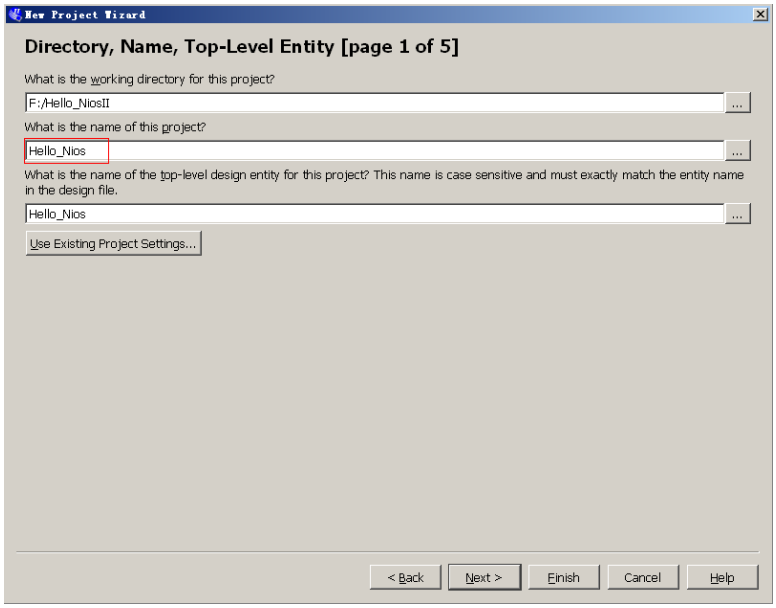
Qsys 和 Nios II Eclipse 的使用

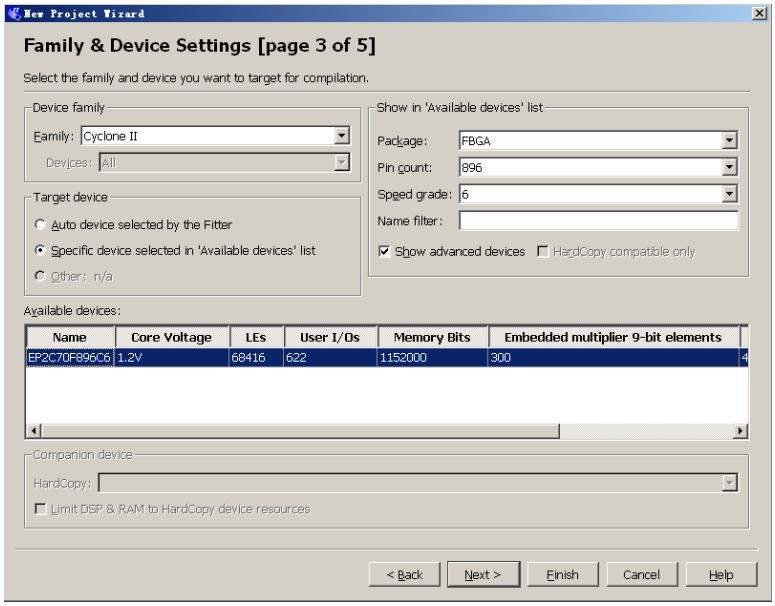
Debug

开发平台：

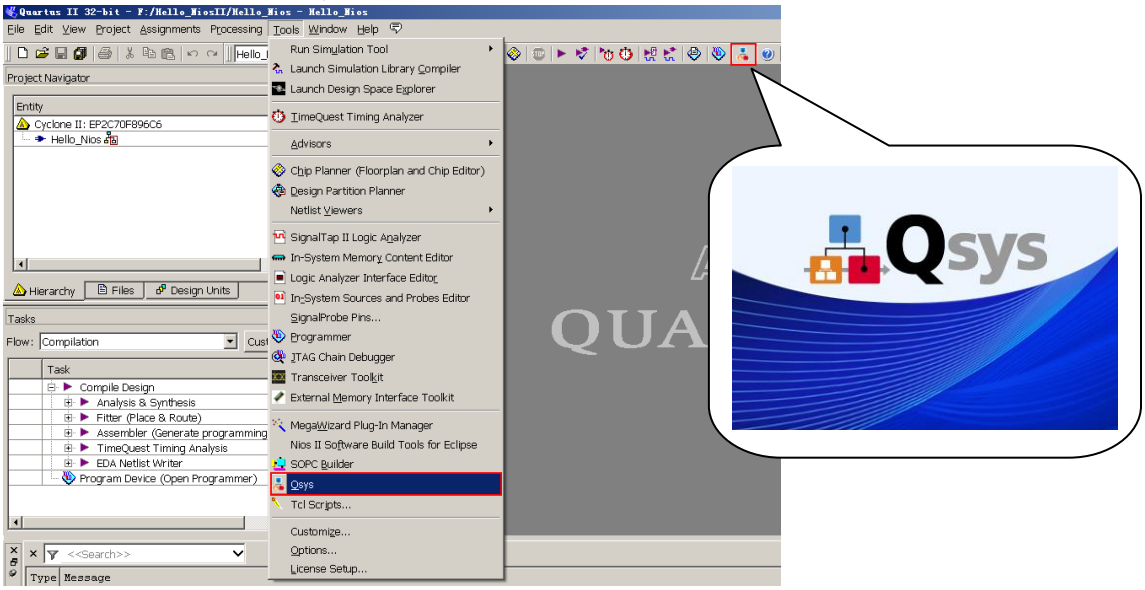
Quartus II 12.0 (Qsys)　　DE2_70

首先，新建工程

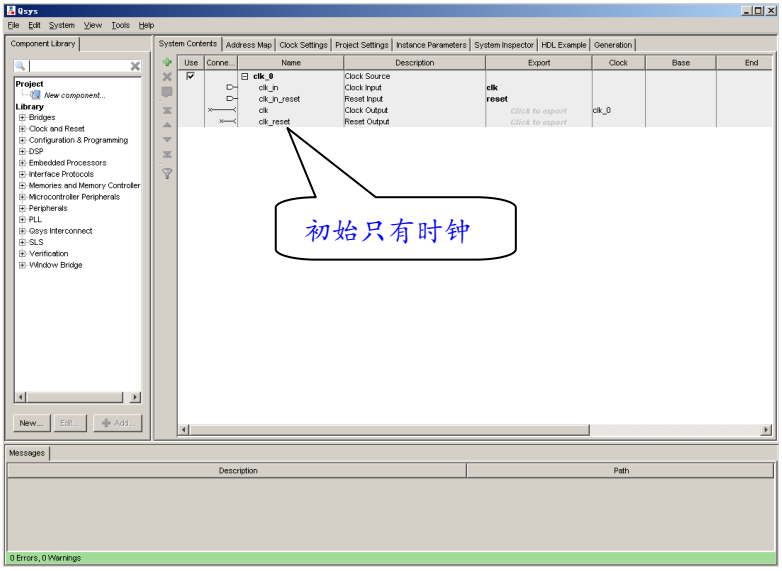


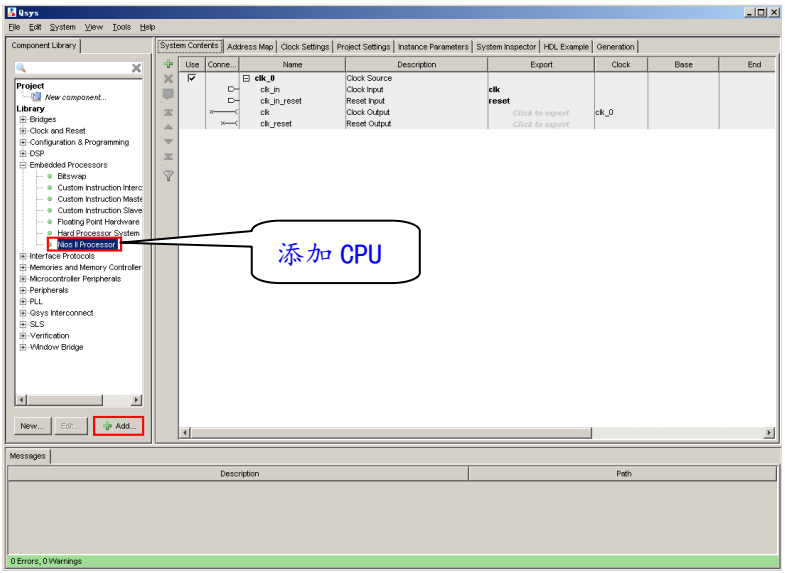


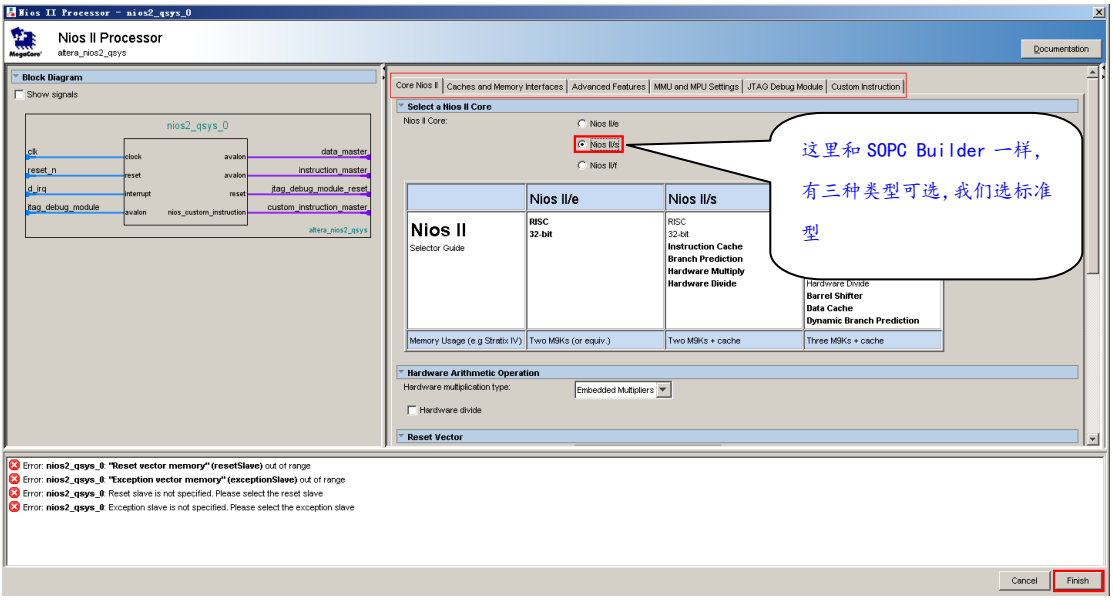
工程新建完成后，启动 Qsys

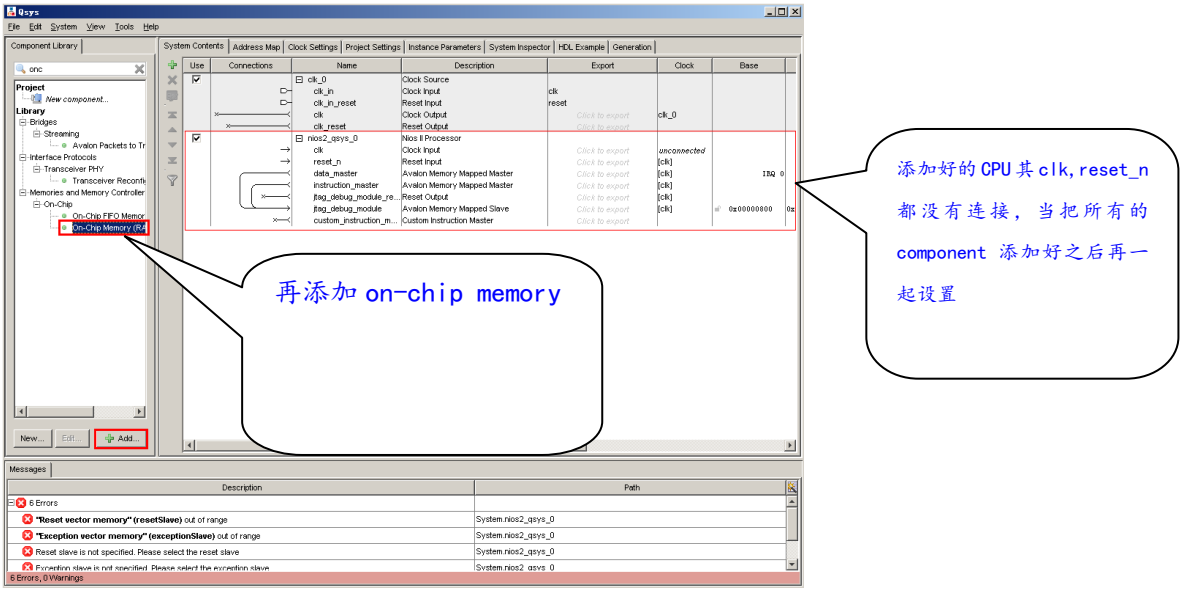


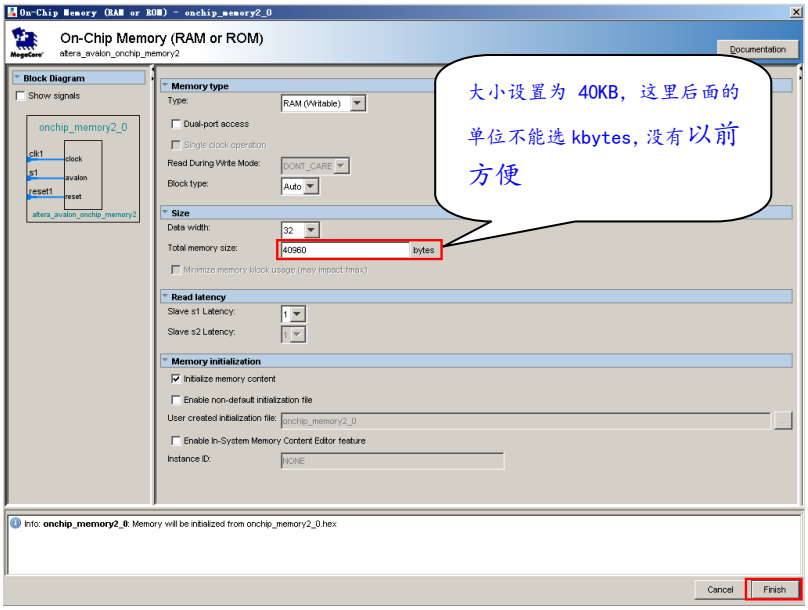
启动之后界面如下：

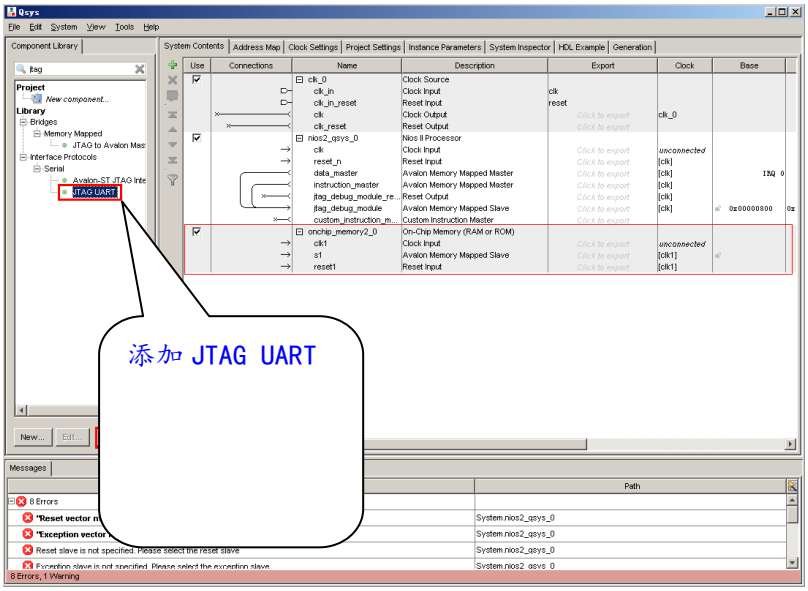


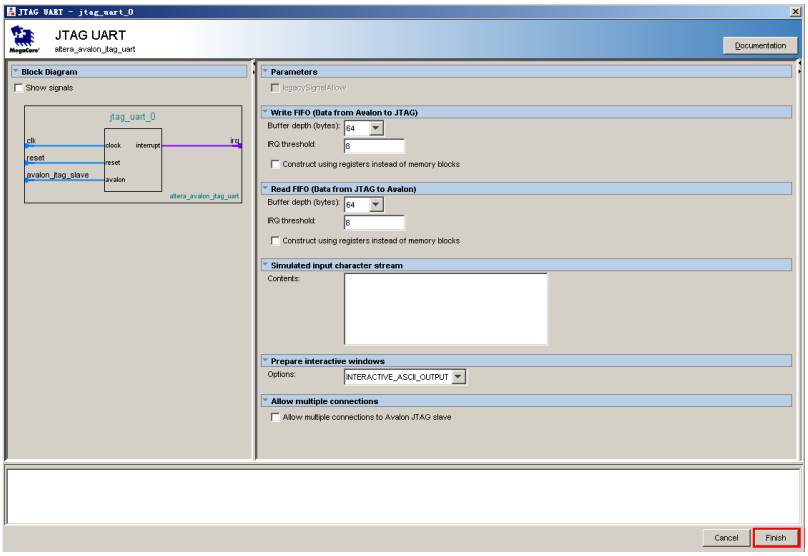


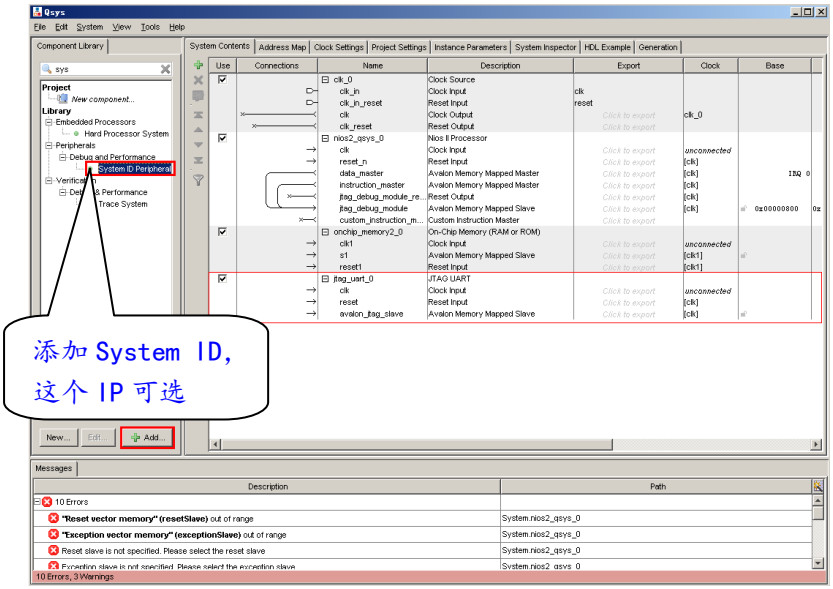

Nios II Processor - nios2_qsys_0
Nios II Processor
altera_nios2_qsys
Documentation
Block Diagram
Show signals
nios2_qsys_0
Core Nios II
Caches and Memory Interfaces
Advanced Features
MMU and MPU Settings
JTAG Debug Module
Custom Instruction
Select a Nios II Core
Nios II Core:
Nios II/e
Nios II/s
Nios II/f
这里和 SOPC Builder 一样，有三种类型可选，我们选标准型
Nios II
Selector Guide
RISC
32-bit
Instruction Cache
Branch Prediction
Hardware Multiply
Hardware Divide
Hardware Divide
Barrel Shifter
Data Cache
Dynamic Branch Prediction
Memory Usage (e.g Stratix IV)
Two M9Ks (or equiv.)
Two M9Ks + cache
Three M9Ks + cache
Hardware Arithmetic Operation
Hardware multiplication type:
Embedded Multipliers
Hardware divide
Reset Vector
Error: nios2_qsys_0: "Reset vector memory" (resetSlave) out of range
Error: nios2_qsys_0: "Exception vector memory" (exceptionSlave) out of range
Error: nios2_qsys_0: Reset slave is not specified. Please select the reset slave
Error: nios2_qsys_0: Exception slave is not specified. Please select the exception slave
Cancel
Finish

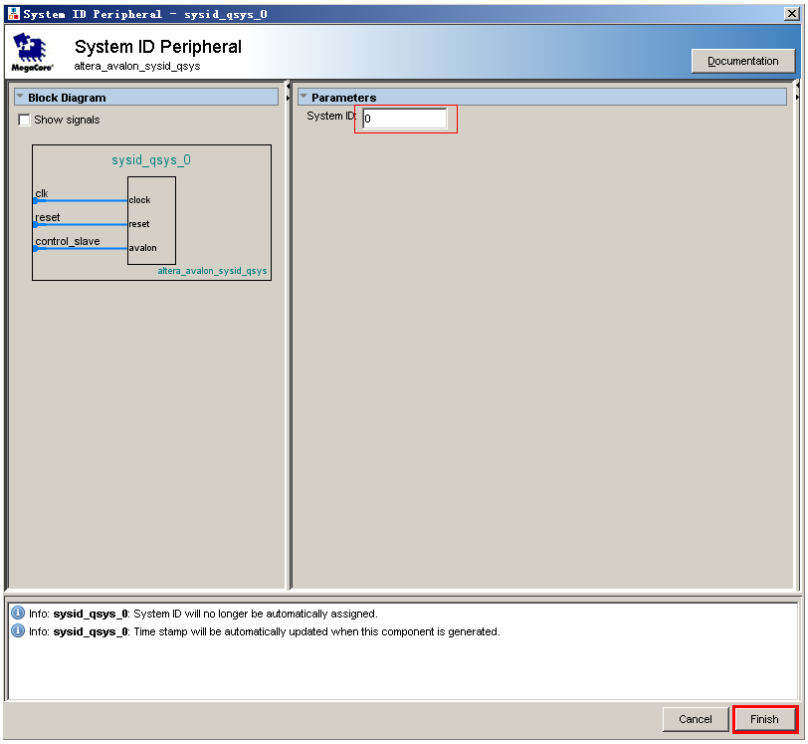

Qsys
File Edit System View Tools Help
Component Library
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
再添加 on-chip memory
添加好的 CPU 其 clk, reset_n 都没有连接，当把所有的 component 添加好之后再一起设置
Messages
6 Errors
"Reset vector memory" (resetSlave) out of range
"Exception vector memory" (exceptionSlave) out of range
Reset slave is not specified. Please select the reset slave
6 Errors, 0 Warnings

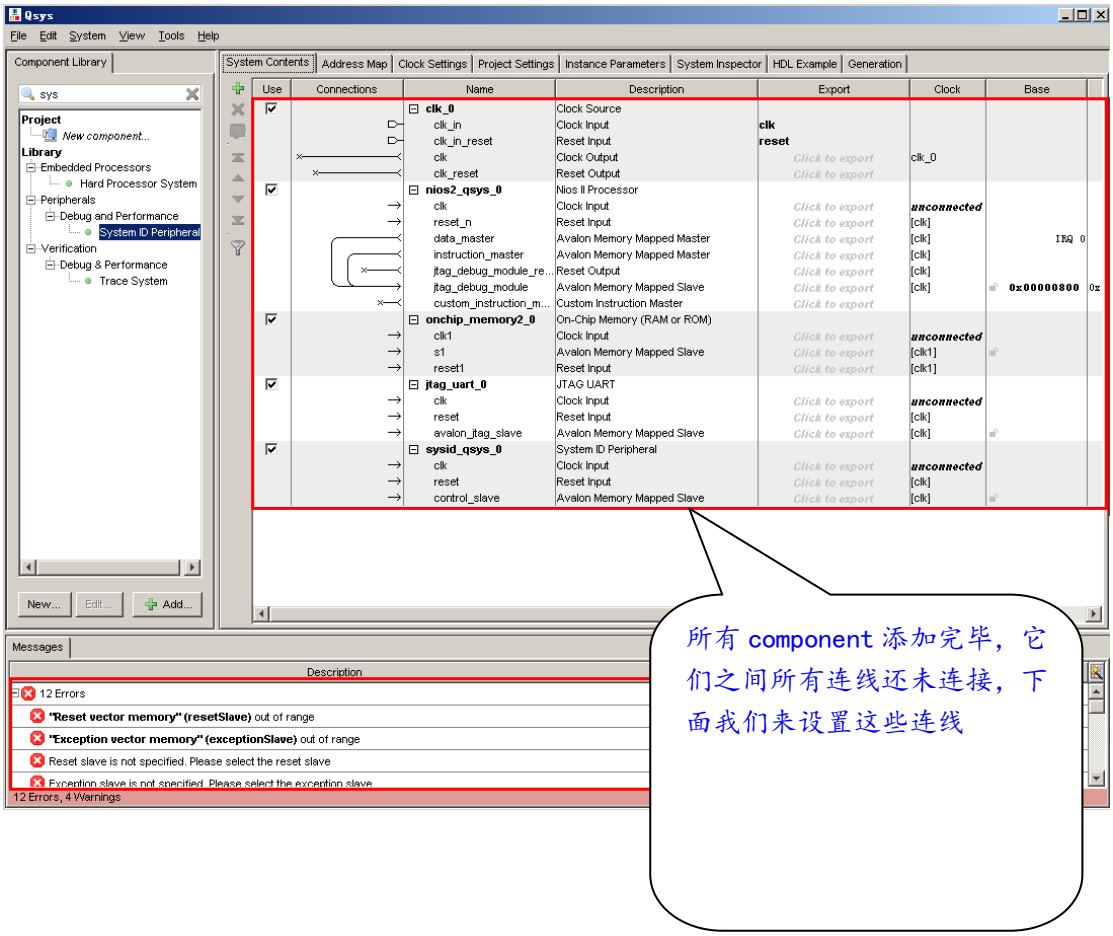

On-Chip Memory (RAM or ROM) - onchip_memory2_0
On-Chip Memory (RAM or ROM)
altera_avalon_onchip_memory2
Documentation
Block Diagram
Show signals
onchip_memory2_0
大小设置为 40KB，这里后面的单位不能选 kbytes，没有以前方便
Memory type
Type:
RAM (Writable)
Dual-port access
Single clock operation
Read During Write Mode:
DONT_CARE
Block type:
Auto
Size
Data width:
32
Total memory size:
40960
bytes
Minimize memory block usage (may impact fmax)
Read latency
Slave s1 Latency:
Slave s2 Latency:
Memory initialization
Initialize memory content
Enable non-default initialization file
User created initialization file:
onchip_memory2_0
Enable In-System Memory Content Editor feature
Instance ID:
NONE
Info: onchip_memory2_0: Memory will be initialized from onchip_memory2_0.hex
Cancel
Finish

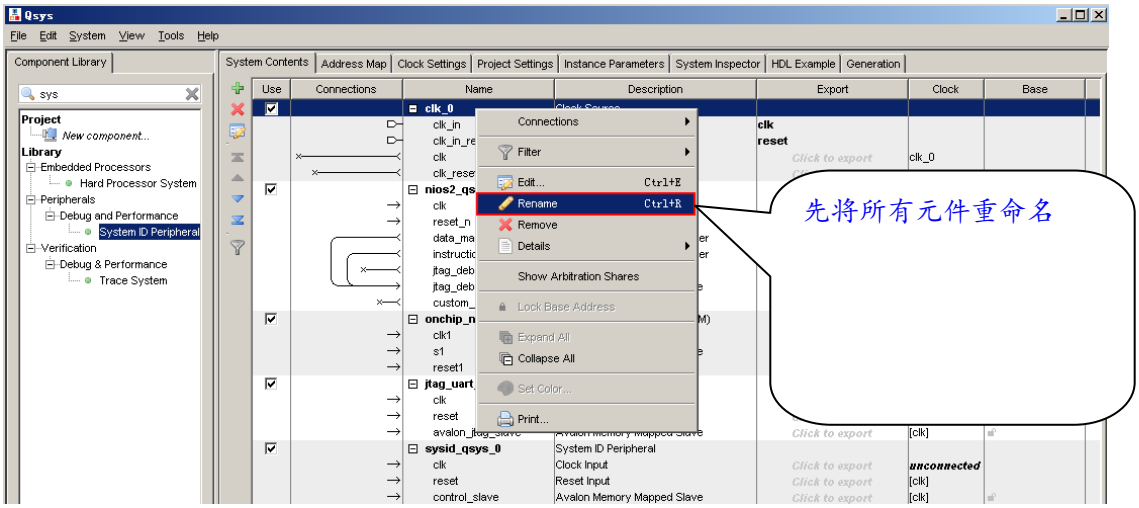

添加 JTAG UART

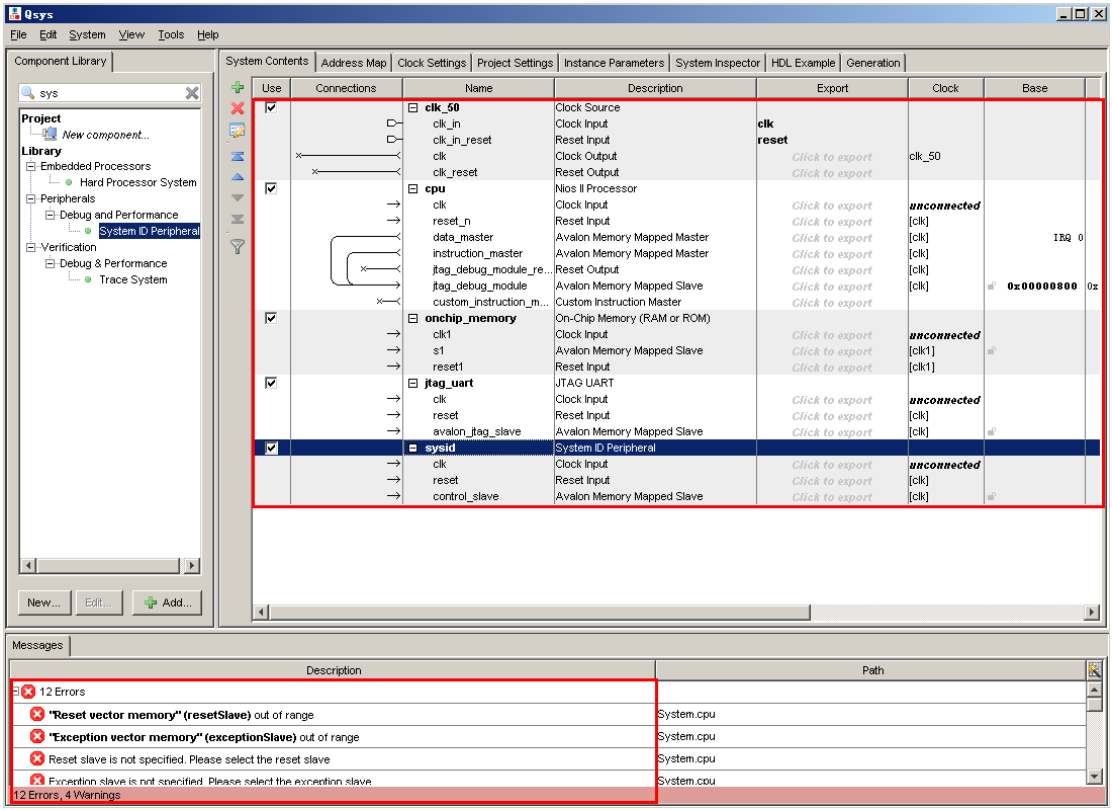

JTAG UART
Documentation
Cancel
Finish


添加 System ID,
这个 IP 可选

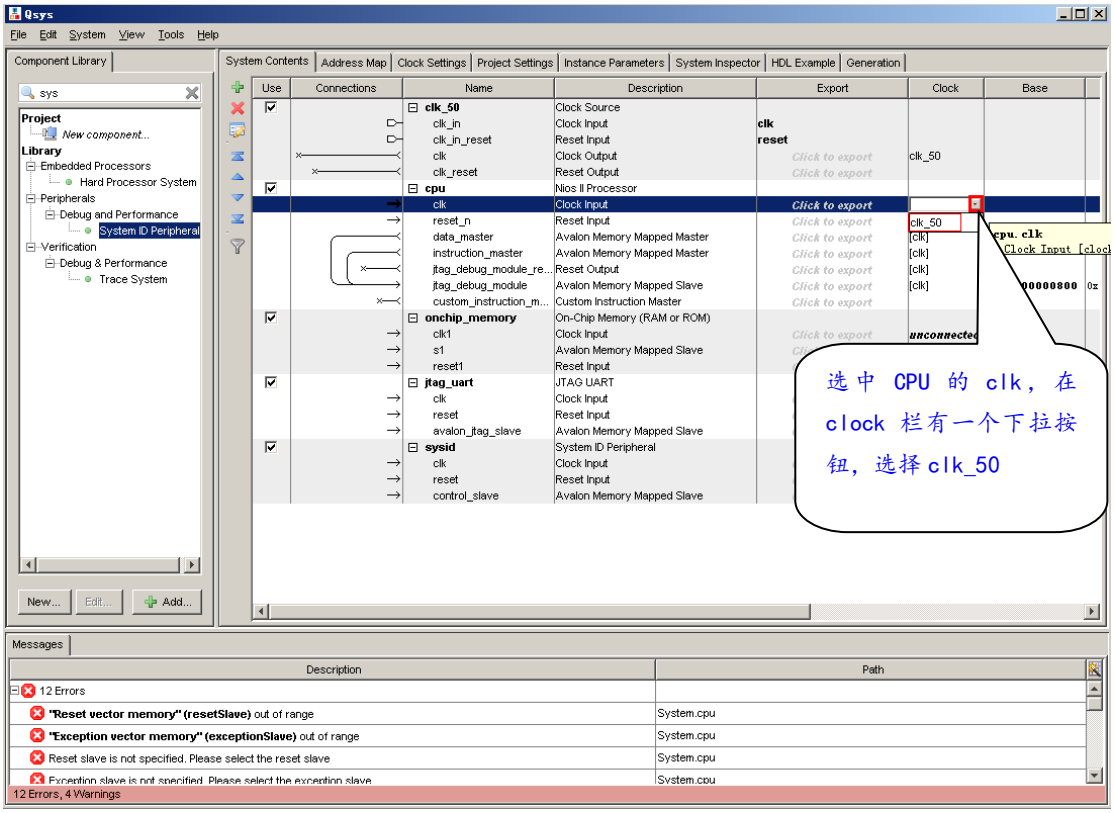

System ID Peripheral - sysid_qsys_0
System ID Peripheral
altera_avalon_sysid_qsys
Documentation
Block Diagram
Show signals
sysid_qsys_0
clk
reset
control_slave
clock
reset
avalon
altera_avalon_sysid_qsys
Parameters
System ID:
0
Info: sysid_qsys_0: System ID will no longer be automatically assigned.
Info: sysid_qsys_0: Time stamp will be automatically updated when this component is generated.
Cancel
Finish

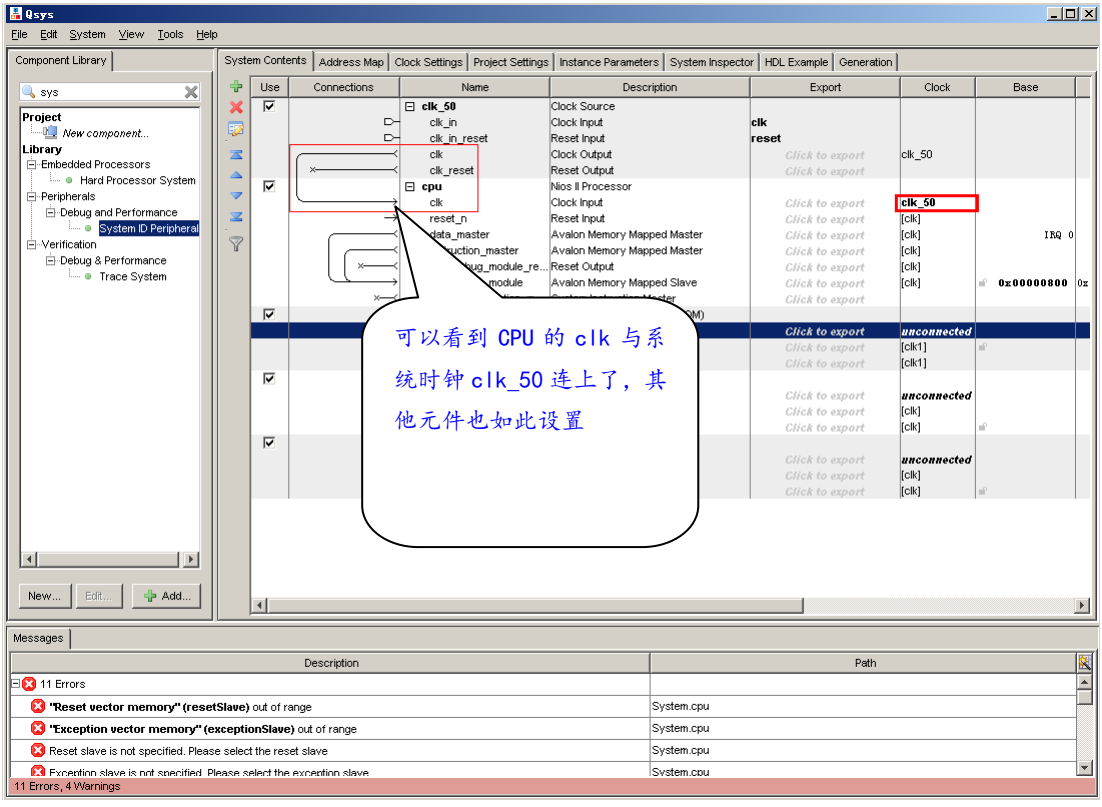

Qsys
File Edit System View Tools Help
Component Library
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
clk_0
nios2_qsys_0
onchip_memory2_0
jtag_uart_0
sysid_qsys_0
Messages
12 Errors
"Reset vector memory" (resetSlave) out of range
"Exception vector memory" (exceptionSlave) out of range
Reset slave is not specified. Please select the reset slave
12 Errors, 4 Warnings
所有 component 添加完毕，它们之间所有连线还未连接，下面我们来设置这些连线

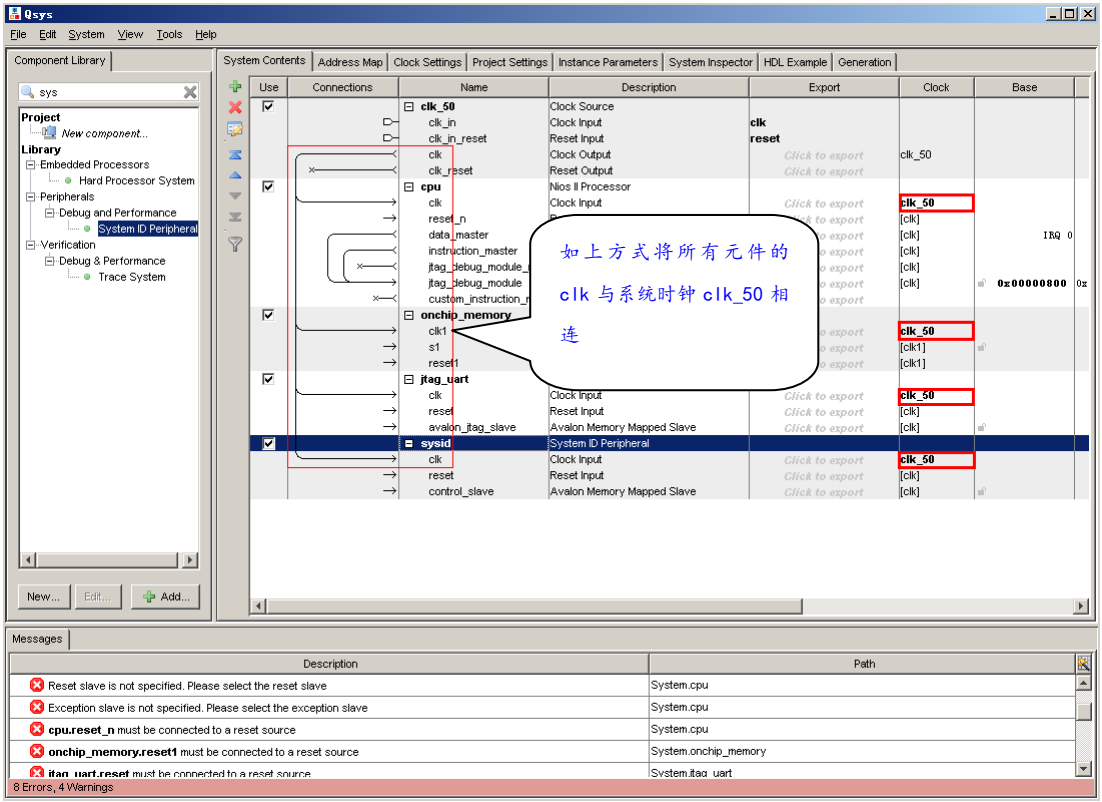


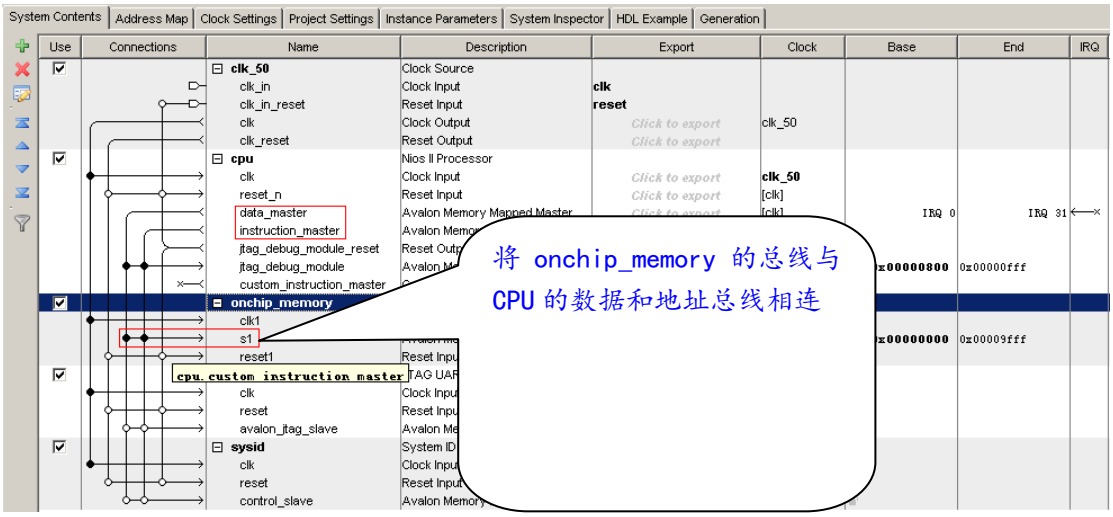


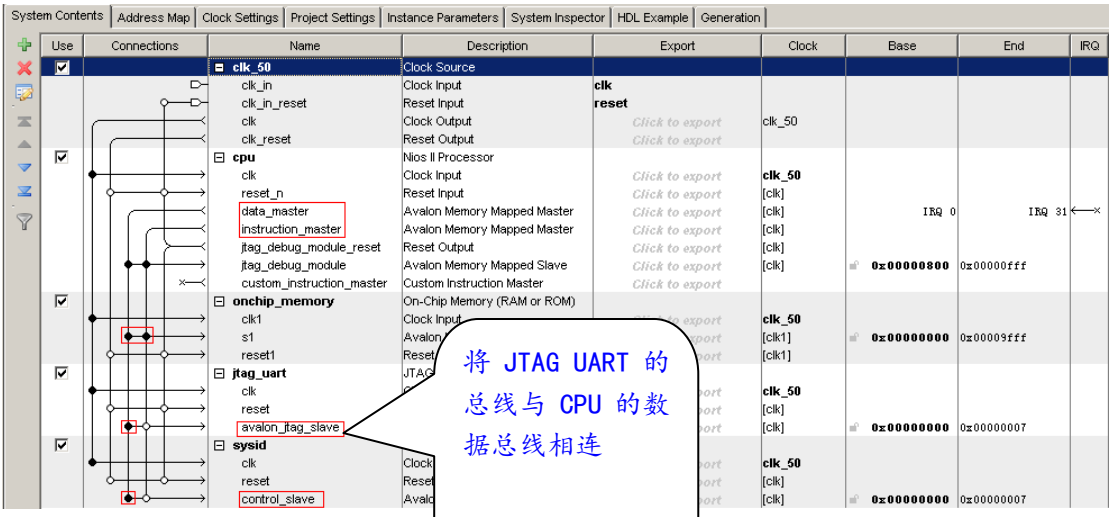
重命名完成之后，需要设置时钟（注意：复位的设置现在先不设置，之后会用全局的复位网络进行快速连接）


Qsys
File Edit System View Tools Help
Component Library
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
clk_50
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
clk_50
clk_reset
Reset Output
cpu
Nios II Processor
reset_n
data_master
instruction_master
jtag_debug_module_re...
jtag_debug_module
custom_instruction_m...
onchip_memory
On-Chip Memory (RAM or ROM)
clk1
s1
reset1
jtag_uart
JTAG UART
avalon_jtag_slave
sysid
control_slave
Click to export
unconnected
选中 CPU 的 clk，在 clock 栏有一个下拉按钮，选择 clk_50
Messages
Description
Path
12 Errors
"Reset vector memory" (resetSlave) out of range
"Exception vector memory" (exceptionSlave) out of range
Reset slave is not specified. Please select the reset slave
12 Errors, 4 Warnings

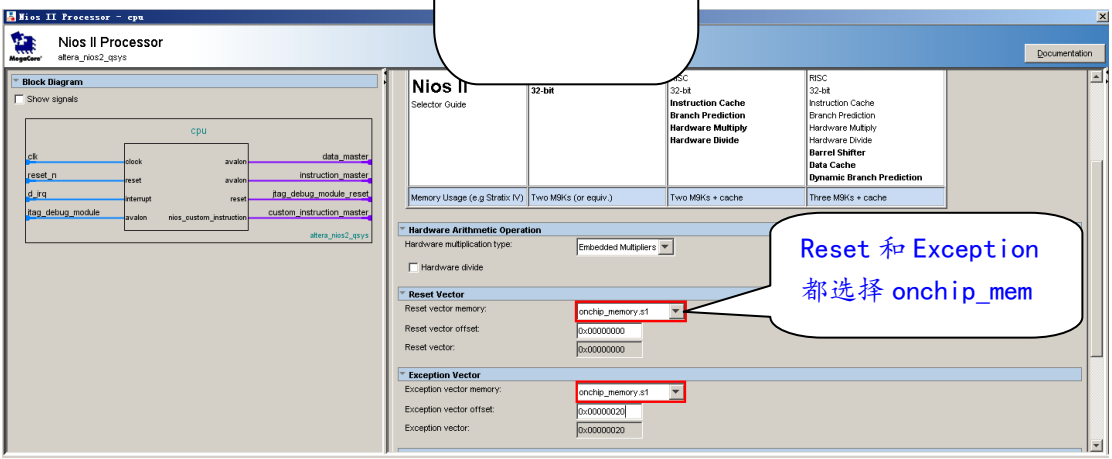

Qsys
File Edit System View Tools Help
Component Library
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
clk_50
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
clk_50
clk_reset
Reset Output
cpu
Nios II Processor
clk_50
reset_n
data_master
Avalon Memory Mapped Master
IRQ 0
Reset Output
Avalon Memory Mapped Slave
0x00000800
unconnected
可以看到 CPU 的 clk 与系统时钟 clk_50 连上了，其他元件也如此设置
Messages
Description
Path
11 Errors
"Reset vector memory" (resetSlave) out of range
"Exception vector memory" (exceptionSlave) out of range
Reset slave is not specified. Please select the reset slave
11 Errors, 4 Warnings

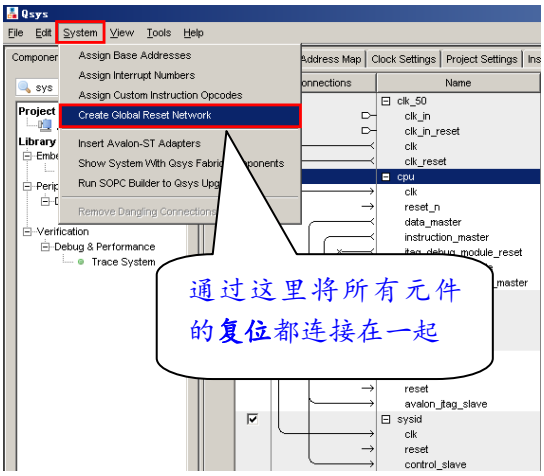

Qsys
File Edit System View Tools Help
Component Library
System Contents Address Map Clock Settings Project Settings Instance Parameters System Inspector HDL Example Generation
如上方式将所有元件的 clk 与系统时钟 clk_50 相连
Messages
Description Path
Reset slave is not specified. Please select the reset slave System.cpu
Exception slave is not specified. Please select the exception slave System.cpu
cpu.reset_n must be connected to a reset source System.cpu
onchip_memory.reset1 must be connected to a reset source System.onchip_memory
8 Errors, 4 Warnings

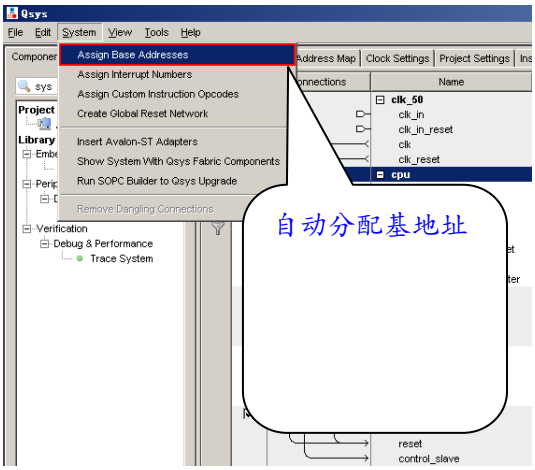

System Contents Address Map Clock Settings Project Settings Instance Parameters System Inspector HDL Example Generation
将 onchip_memory 的总线与 CPU 的数据和地址总线相连

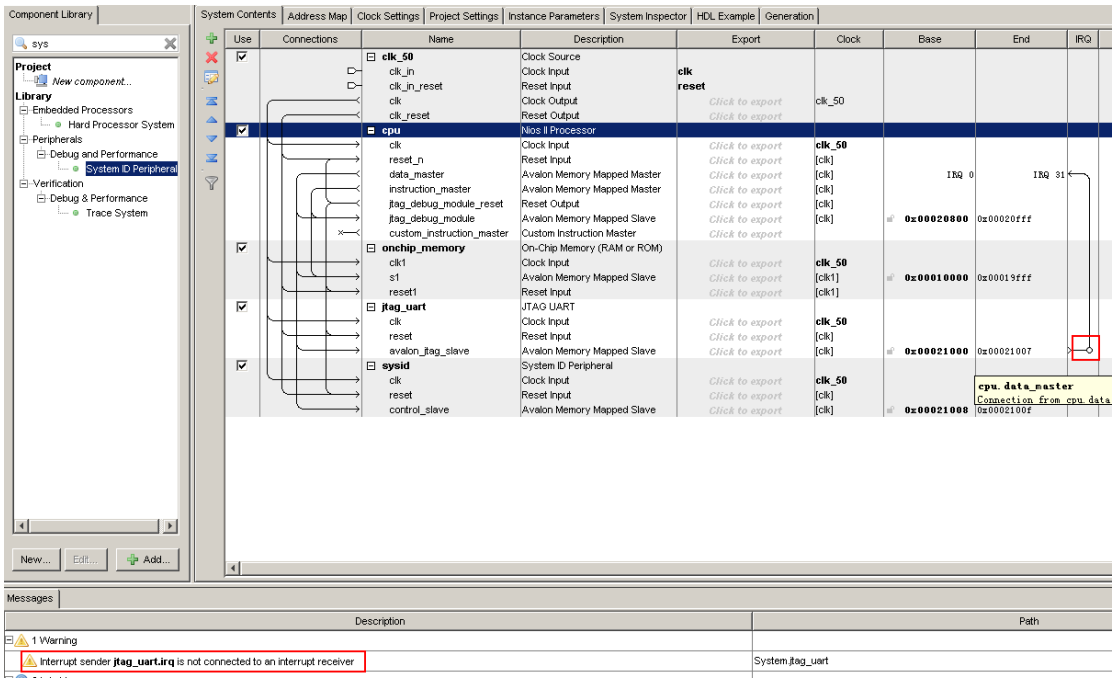

System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
End
IRQ
clk_50
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
clk_reset
Reset Output
cpu
Nios II Processor
reset_n
data_master
instruction_master
jtag_debug_module_reset
jtag_debug_module
Avalon Memory Mapped Slave
custom_instruction_master
Custom Instruction Master
onchip_memory
On-Chip Memory (RAM or ROM)
clk1
s1
reset1
jtag_uart
avalon_jtag_slave
sysid
control_slave
0x00000800
0x00000fff
0x00000000
0x00009fff
0x00000007
将 JTAG UART 的总线与 CPU 的数据总线相连

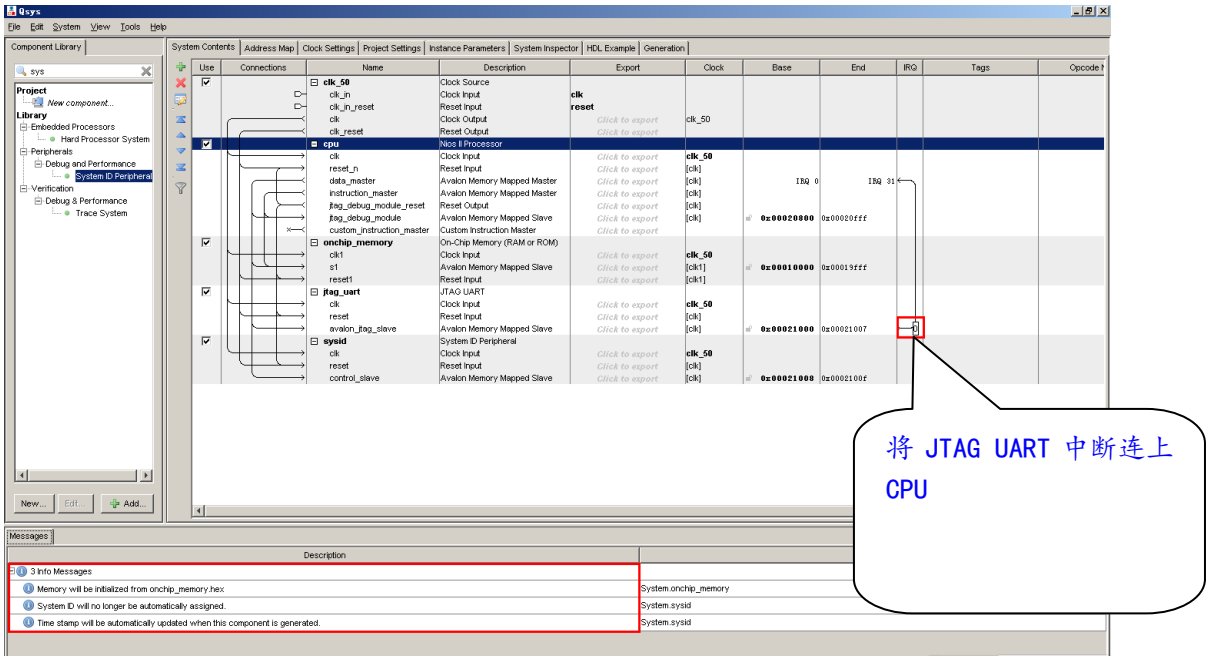
设置复位和异常的位置

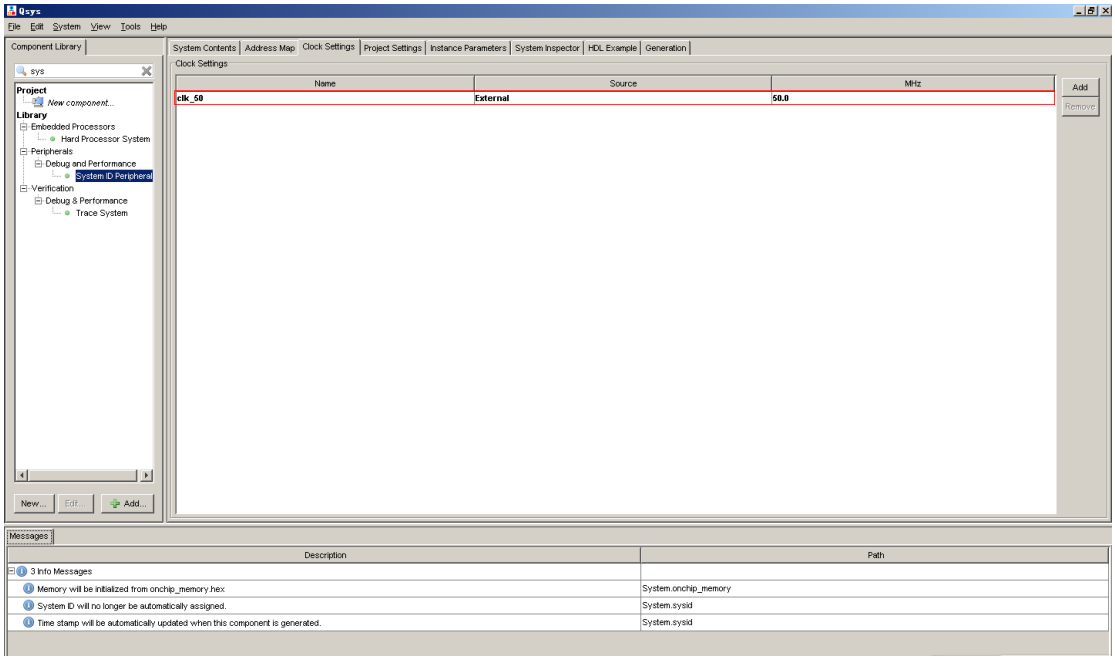

Nios II Processor - cpu
Nios II Processor
altera_nios2_qsys
Documentation
Block Diagram
Show signals
Nios II
Selector Guide
Hardware Arithmetic Operation
Hardware multiplication type:
Embedded Multipliers
Hardware divide
Reset Vector
Reset vector memory:
onchip_memory.s1
Reset vector offset:
Reset vector:
Exception Vector
Exception vector memory:
Exception vector offset:
Exception vector:
Reset 和 Exception 都选择 onchip_mem

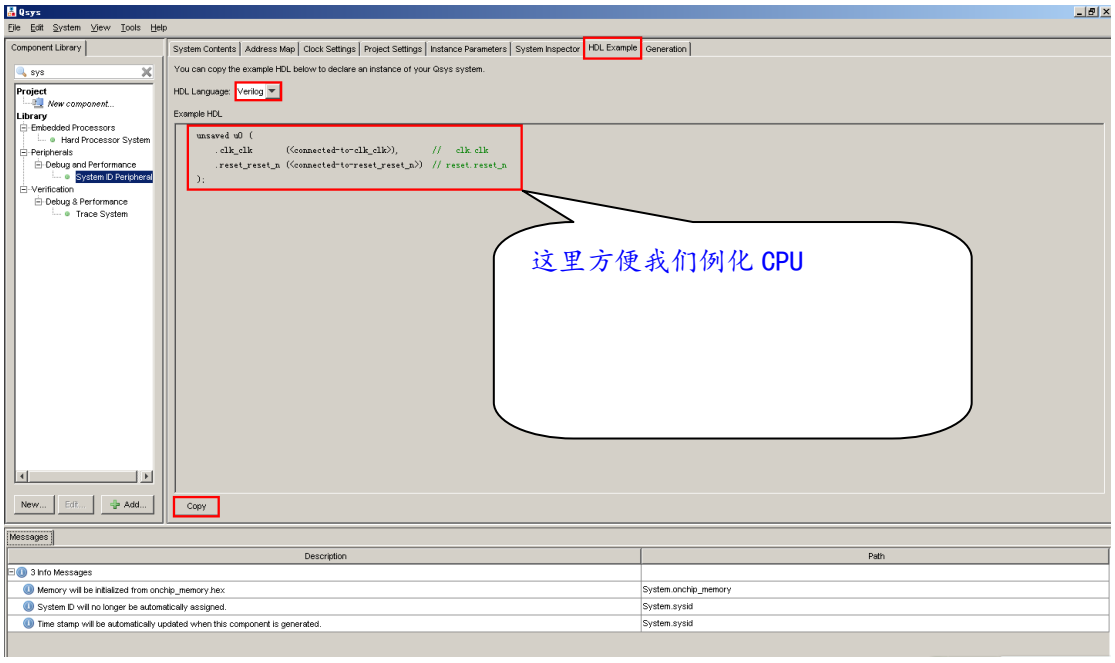

Qsys
File
Edit
System
View
Tools
Help
Assign Base Addresses
Assign Interrupt Numbers
Assign Custom Instruction Opcodes
Create Global Reset Network
Insert Avalon-ST Adapters
Show System With Qsys Fabric
Run SOPC Builder to Qsys Upg
Remove Dangling Connections
Project
Library
Verification
Debug & Performance
Trace System
Address Map
Clock Settings
Project Settings
Name
clk_50
clk_in
clk_in_reset
clk
clk_reset
cpu
reset_n
data_master
instruction_master
reset
avalon_jtag_slave
sysid
control_slave
通过这里将所有元件的复位都连接在一起

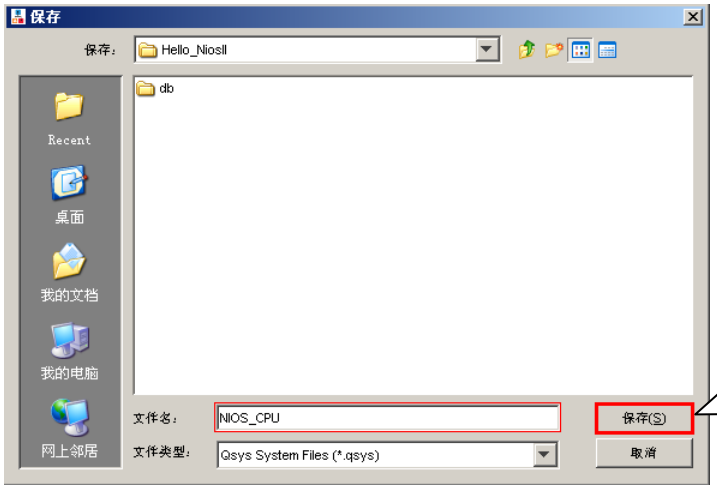

Qsys
File
Edit
System
View
Tools
Help
Assign Base Addresses
Assign Interrupt Numbers
Assign Custom Instruction Opcodes
Create Global Reset Network
Insert Avalon-ST Adapters
Show System With Qsys Fabric Components
Run SOPC Builder to Qsys Upgrade
Remove Dangling Connections
Project
Library
Verification
Debug & Performance
Trace System
Address Map
Clock Settings
Project Settings
Name
clk_50
clk_in
clk_in_reset
clk
clk_reset
cpu
reset
control_slave
自动分配基地址


Component Library
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
End
IRQ
clk_50
cpu
onchip_memory
jtag_uart
sysid
Messages
Description
Path
1 Warning
Interrupt sender jtag_uart.irq is not connected to an interrupt receiver
System.jtag_uart

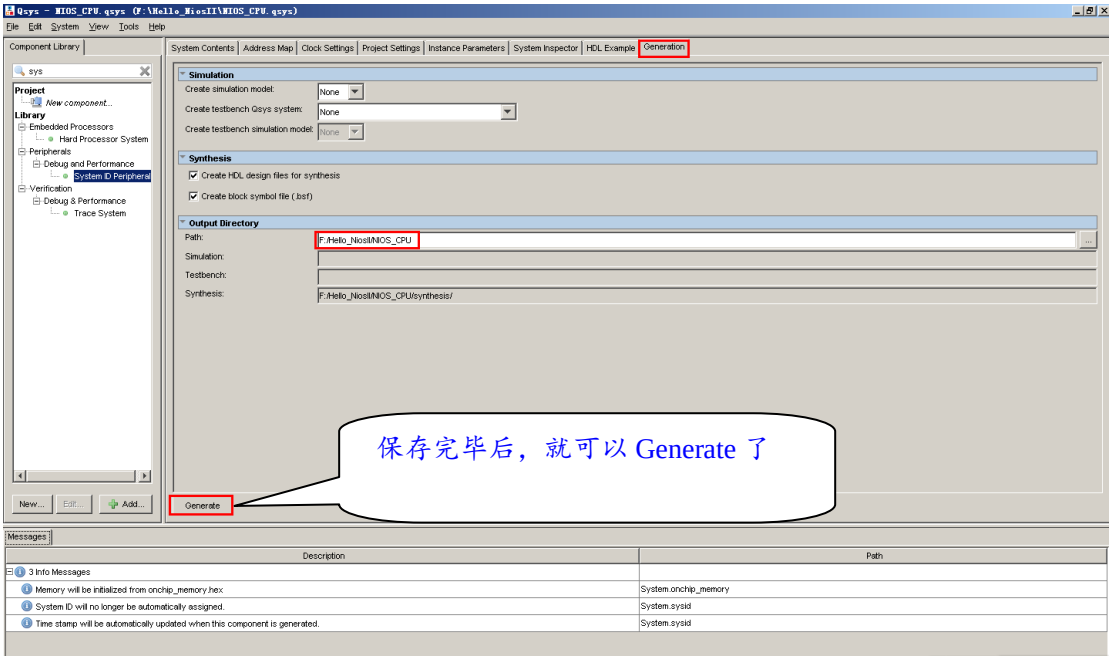

Qsys
File Edit System View Tools Help
Component Library
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Messages
3 Info Messages
Memory will be initialized from onchip_memory.hex
System ID will no longer be automatically assigned.
Time stamp will be automatically updated when this component is generated.
System.onchip_memory
System.sysid
System.sysid
将 JTAG UART 中断连上 CPU

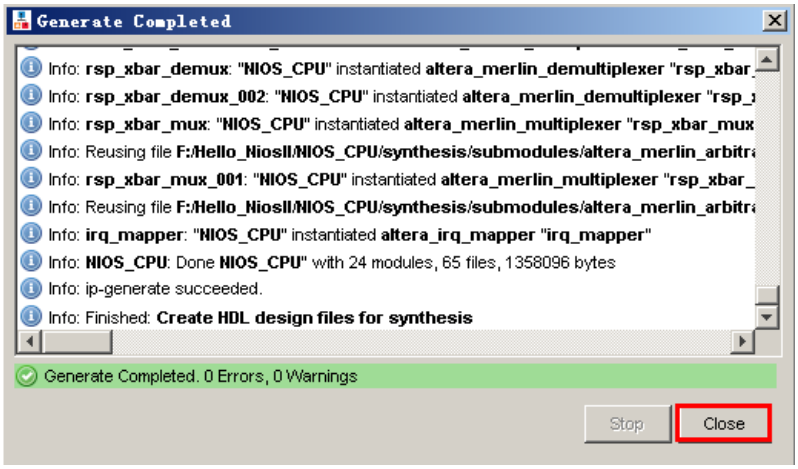




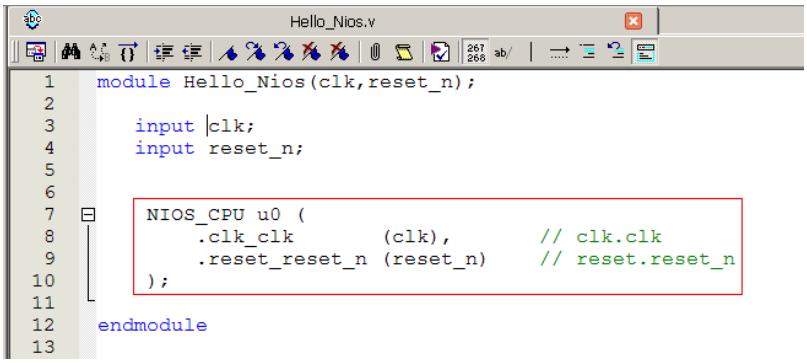


在设置和检查完成后，先保存我们的 CPU





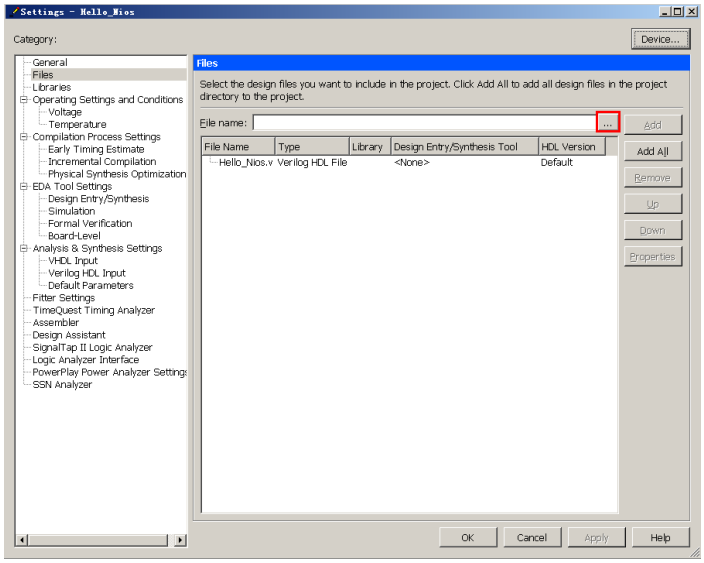
Nios CPU 定制完成后，需要在 Quartus II 的顶层模块中例化，首先回到 Quartus 中新建顶层 Verilog 文件，然后对 CPU 进行例化：

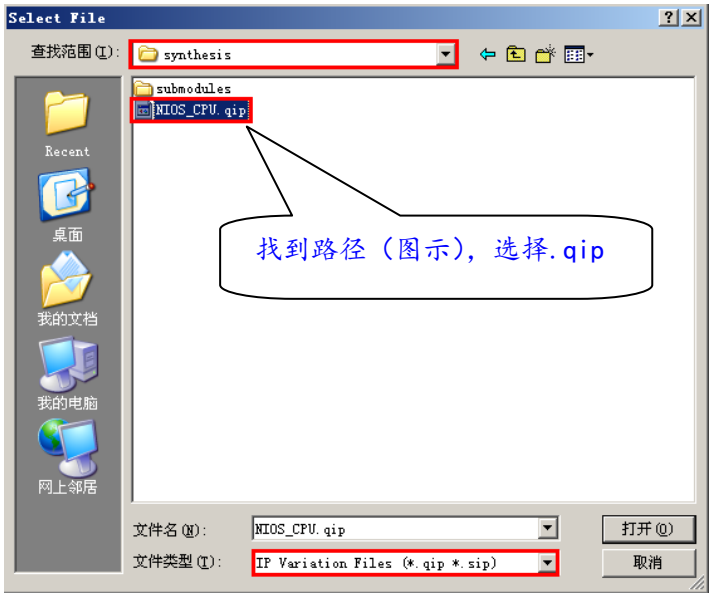


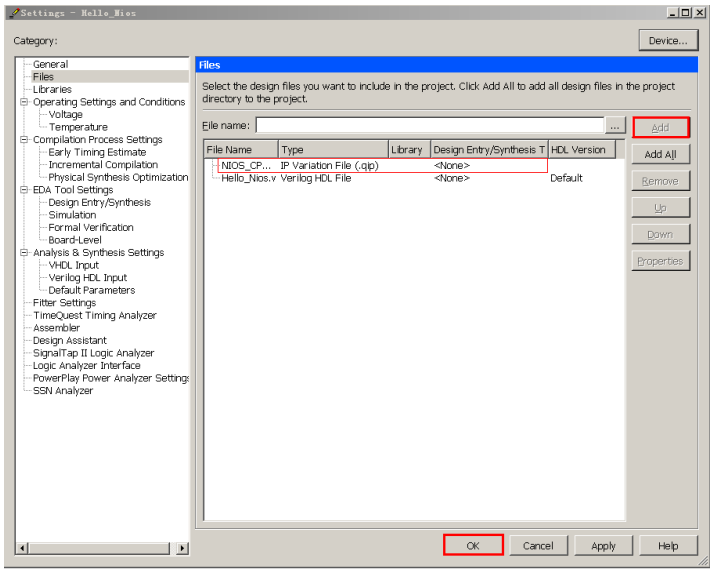
如果此时进行编译的话，会有错误：

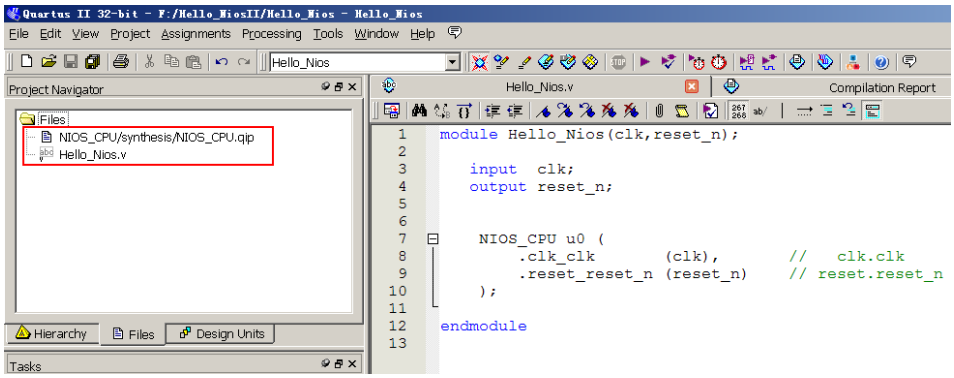
Error (12006): Node instance "u0" instantiates undefined entity "NIOS_CPU"

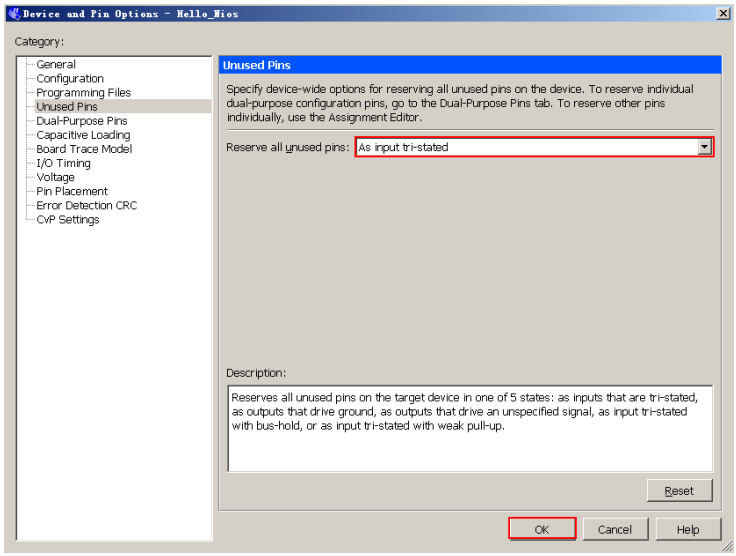
因为之前定制的 CPU 还没有被加入到 Quartus 的工程中，需要我们手动添加：


Settings - Hello_Nios
Category:
Device...
General
Files
Libraries
Operating Settings and Conditions
Voltage
Temperature
Compilation Process Settings
Early Timing Estimate
Incremental Compilation
Physical Synthesis Optimization
EDA Tool Settings
Design Entry/Synthesis
Simulation
Formal Verification
Board-Level
Analysis & Synthesis Settings
VHDL Input
Verilog HDL Input
Default Parameters
Fitter Settings
TimeQuest Timing Analyzer
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
PowerPlay Power Analyzer Settings
SSN Analyzer
Files
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
File name:
Add
Add All
Remove
Up
Down
Properties
File Name
Type
Library
Design Entry/Synthesis Tool
HDL Version
Hello_Nios.v
Verilog HDL File
<None>
Default
OK
Cancel
Apply
Help

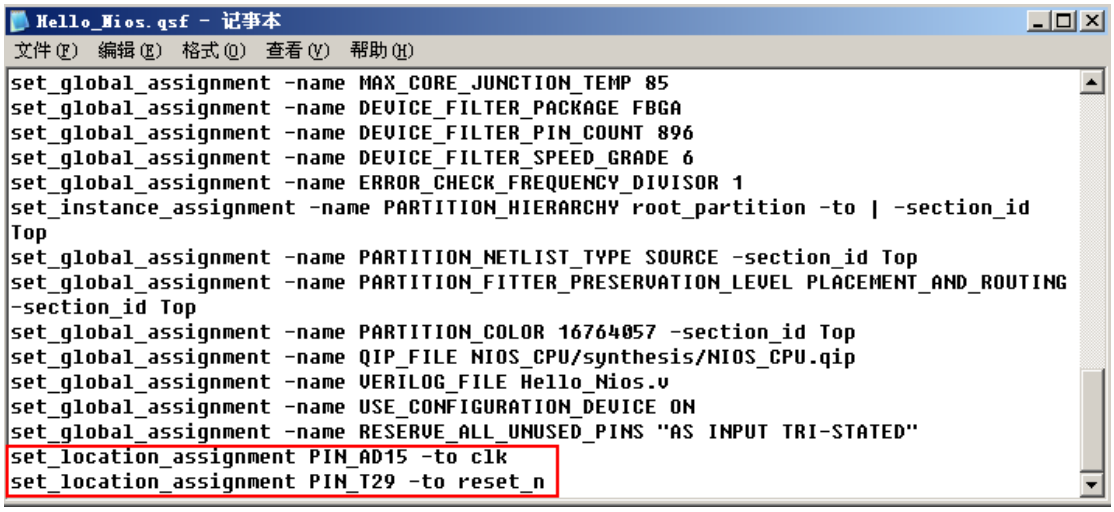

Select File
查找范围(I):
synthesis
submodules
NIOS_CPU.qip
找到路径（图示），选择.qip
Recent
桌面
我的文档
我的电脑
网上邻居
文件名(N):
NIOS_CPU.qip
打开(O)
文件类型(T):
IP Variation Files (*.qip *.sip)
取消


Settings - Hello_Nios
Category:
Device...
General
Files
Libraries
Operating Settings and Conditions
Voltage
Temperature
Compilation Process Settings
Early Timing Estimate
Incremental Compilation
Physical Synthesis Optimization
EDA Tool Settings
Design Entry/Synthesis
Simulation
Formal Verification
Board-Level
Analysis & Synthesis Settings
VHDL Input
Verilog HDL Input
Default Parameters
Fitter Settings
TimeQuest Timing Analyzer
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
PowerPlay Power Analyzer Settings
SSN Analyzer
Files
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
File name:
Add
Add All
Remove
Up
Down
Properties
File Name
Type
Library
Design Entry/Synthesis T
HDL Version
NIOS_CP...
IP Variation File (.qip)
<None>
Hello_Nios.v
Verilog HDL File
<None>
Default
OK
Cancel
Apply
Help

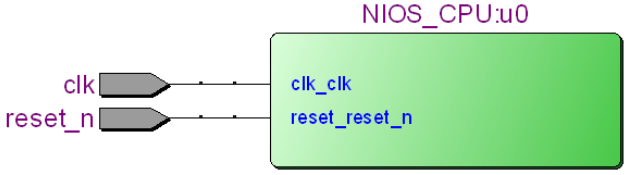




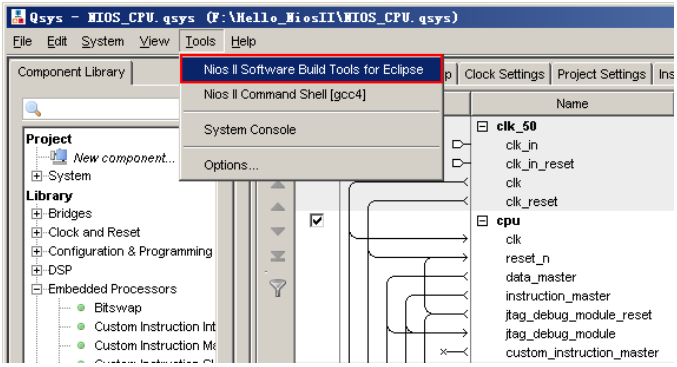
分配管脚

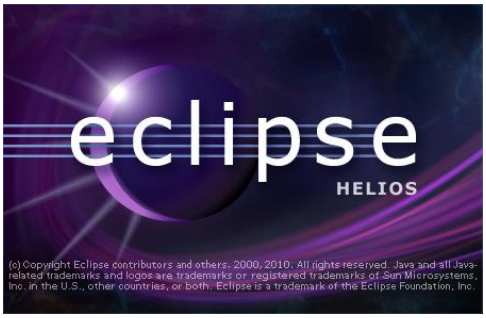


至此，我们就完成了硬件部分设置，先完全编译，查看 RTL：



接下来要在 Nios II Eclipse 进行软件设计了，打开 Nios II 开发环境


Qsys - NIOS_CPU.qsys (F:\Hello_NiosII\NIOS_CPU.qsys)
File Edit System View Tools Help
Nios II Software Build Tools for Eclipse
Nios II Command Shell [gcc4]
System Console
Options...
Component Library
Clock Settings
Project Settings
Name
Project
New component...
System
Library
Bridges
Clock and Reset
Configuration & Programming
DSP
Embedded Processors
Bitswap
clk_50
clk_in
clk_in_reset
clk
clk_reset
cpu
clk
reset_n
data_master
instruction_master
jtag_debug_module_reset
jtag_debug_module
custom_instruction_master


eclipse
HELIOS
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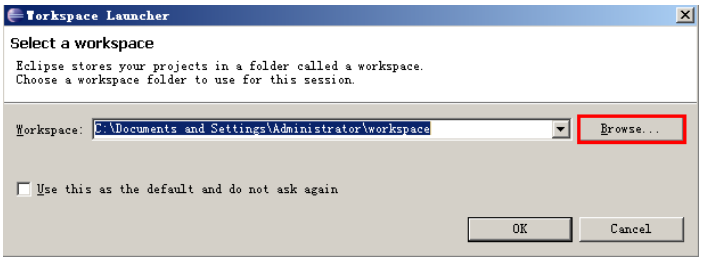
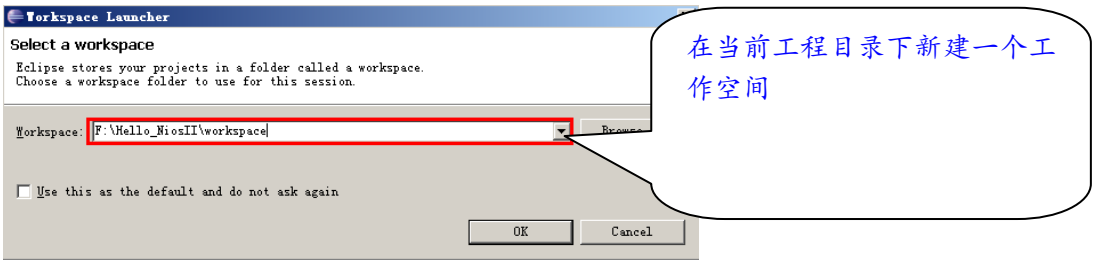
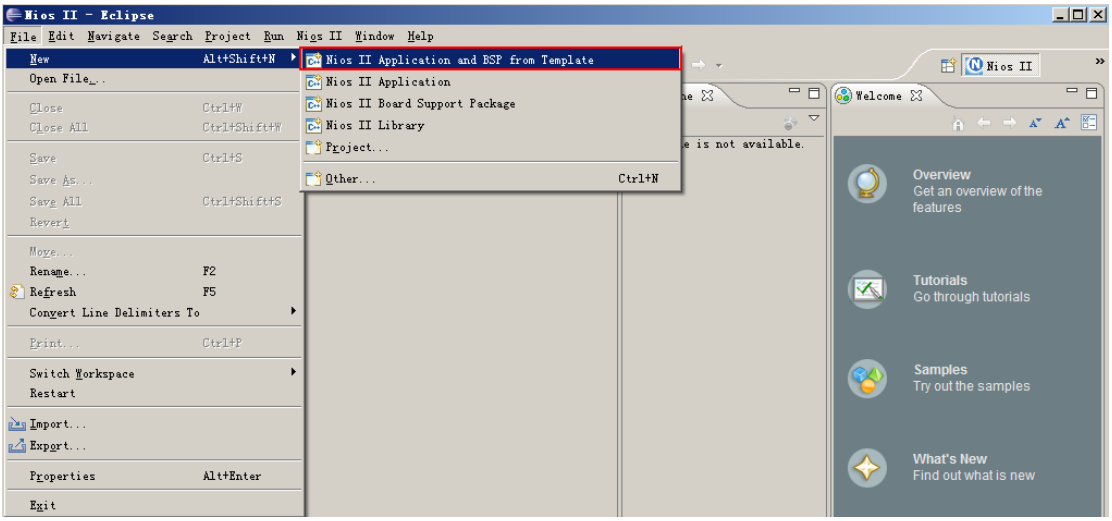
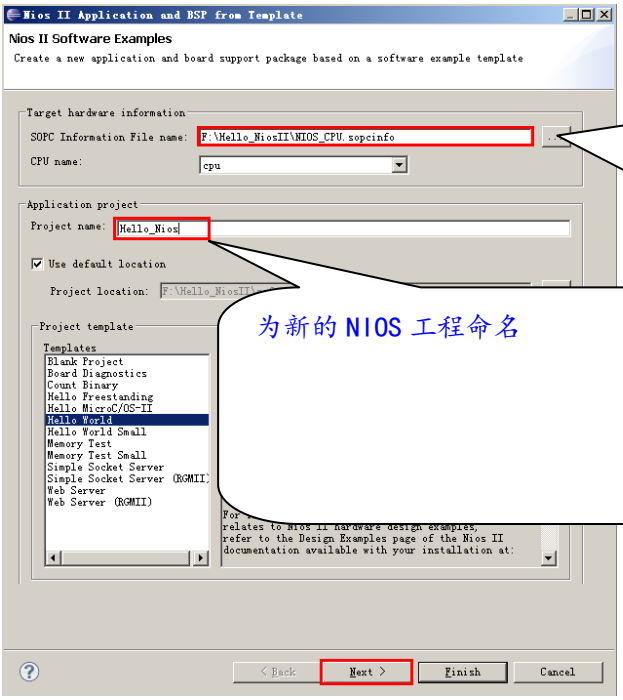

Workspace Launcher
Select a workspace
Eclipse stores your projects in a folder called a workspace.
Choose a workspace folder to use for this session.
Workspace:
C:\Documents and Settings\Administrator\workspace
Browse...
Use this as the default and do not ask again
OK
Cancel


Workspace Launcher
Select a workspace
Eclipse stores your projects in a folder called a workspace.
Choose a workspace folder to use for this session.
Workspace:
F:\Hello_NiosII\workspace
Use this as the default and do not ask again
OK
Cancel
在当前工程目录下新建一个工作空间

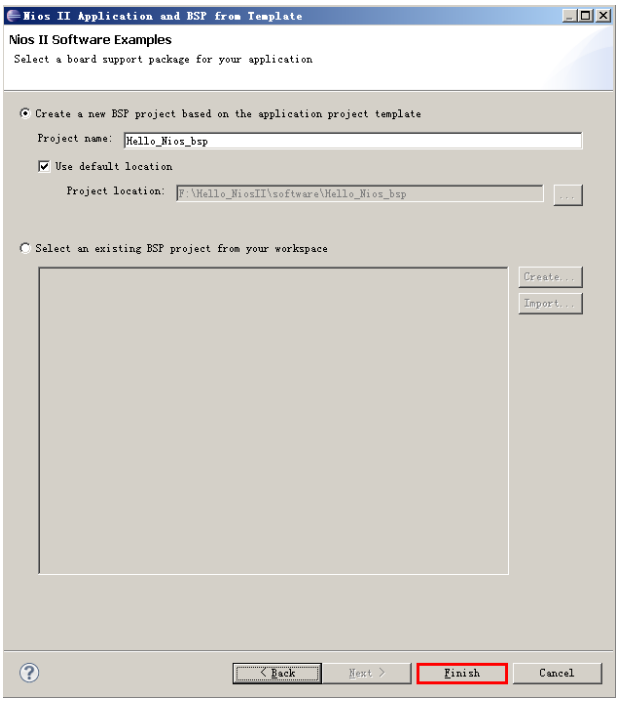
新建 NIOS 工程：

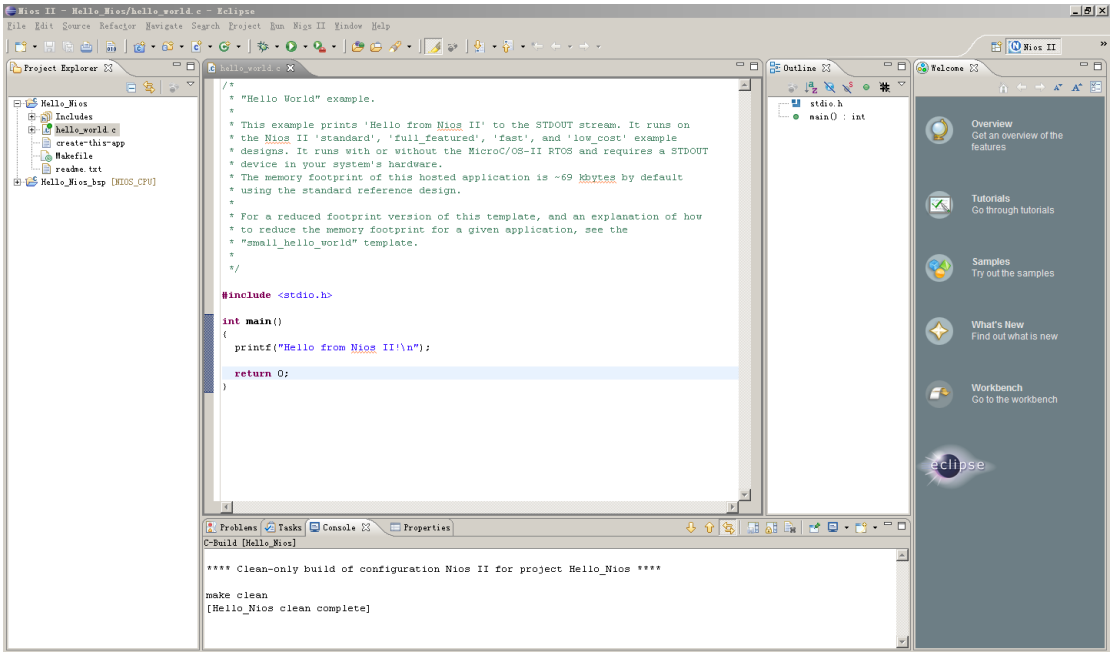

Nios II - Eclipse
File Edit Navigate Search Project Run Nios II Window Help
New Alt+Shift+N
Open File...
Close Ctrl+W
Close All Ctrl+Shift+W
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
Revert
Move...
Rename... F2
Refresh F5
Convert Line Delimiters To
Print... Ctrl+P
Switch Workspace
Restart
Import...
Export...
Properties Alt+Enter
Exit
Nios II Application and BSP from Template
Nios II Application
Nios II Board Support Package
Nios II Library
Project...
Other... Ctrl+N
Nios II
Welcome
Overview
Get an overview of the features
Tutorials
Go through tutorials
Samples
Try out the samples
What's New
Find out what is new

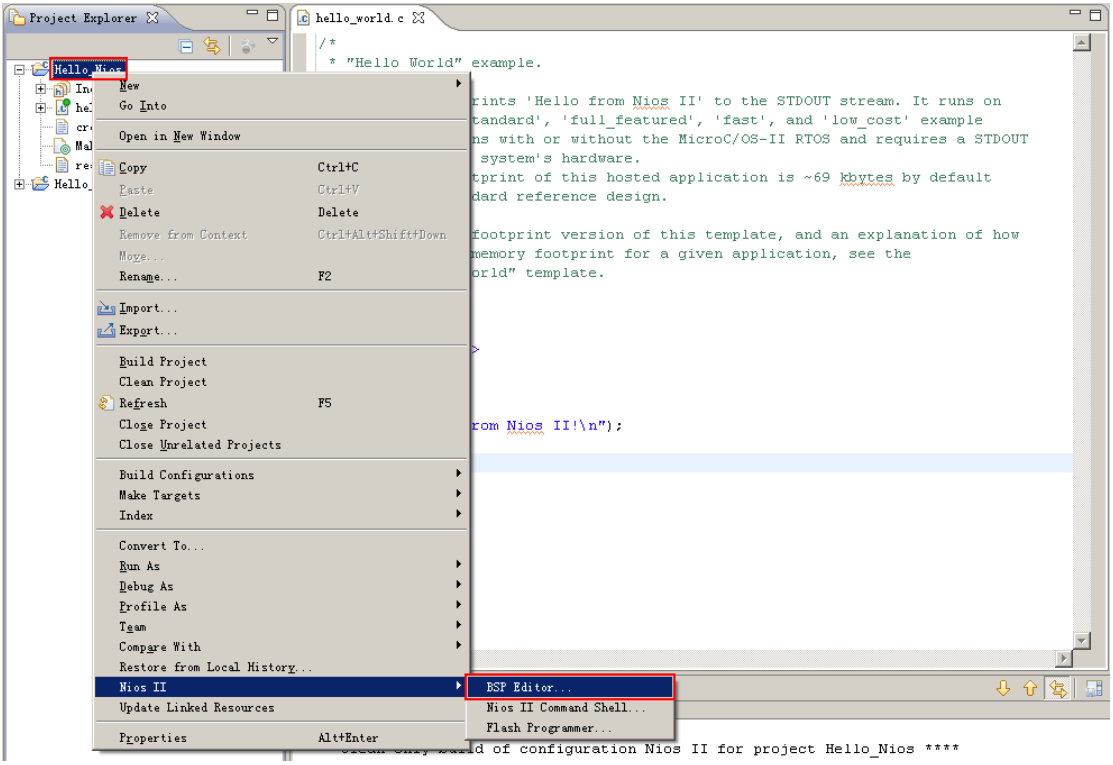


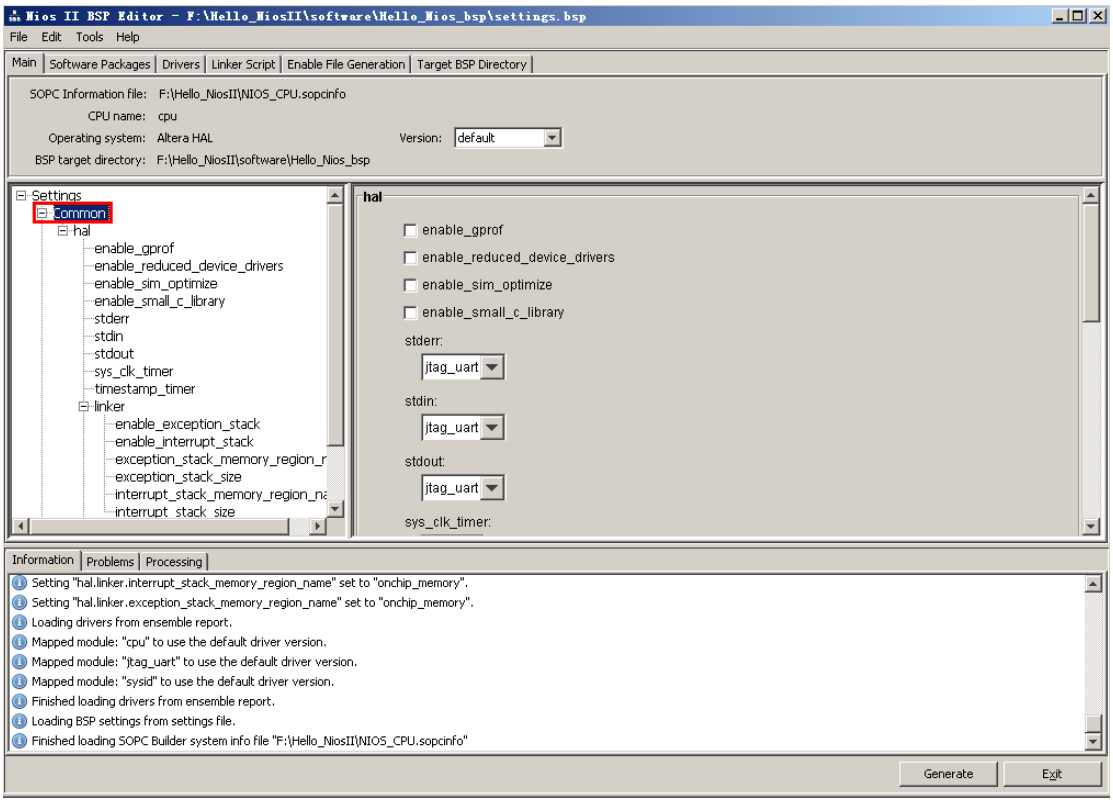
选择之前 Qsys 产生的.sopcinfo 文件

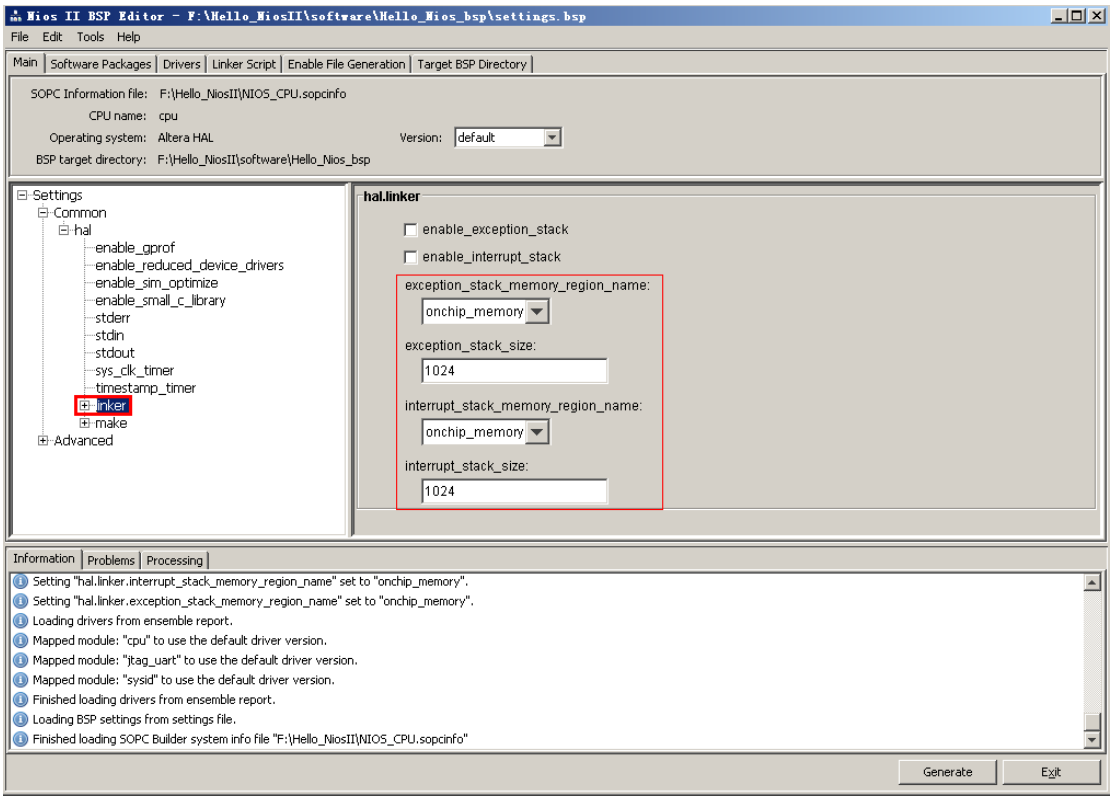
为新的 NIOS 工程命名



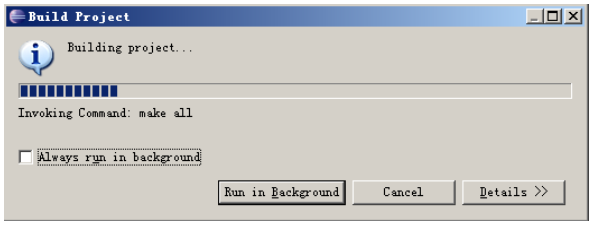

Nios II - Hello_Nios/hello_world.c - Eclipse
File Edit Source Refactor Navigate Search Project Run Nios II Window Help
Project Explorer
Hello_Nios
Includes
hello_world.c
create-this-app
Makefile
readme.txt
Hello_Nios_bsp [NIOS_CPU]
hello_world.c
/*
* "Hello World" example.
*
* This example prints 'Hello from Nios II' to the STDOUT stream. It runs on
* the Nios II 'standard', 'full_featured', 'fast', and 'low_cost' example
* designs. It runs with or without the MicroC/OS-II RTOS and requires a STDOUT
* device in your system's hardware.
* The memory footprint of this hosted application is ~69 kbytes by default
* using the standard reference design.
*
* For a reduced footprint version of this template, and an explanation of how
* to reduce the memory footprint for a given application, see the
* "small_hello_world" template.
*
*/
#include <stdio.h>
int main()
{
printf("Hello from Nios II!\n");
return 0;
}
Outline
stdio.h
main() : int
Welcome
Overview
Get an overview of the features
Tutorials
Go through tutorials
Samples
Try out the samples
What's New
Find out what is new
Workbench
Go to the workbench
eclipse
Problems Tasks Console Properties
C-Build [Hello_Nios]
**** Clean-only build of configuration Nios II for project Hello_Nios ****
make clean
[Hello_Nios clean complete]


Project Explorer
hello_world.c
Hello_Nios
New
Go Into
Open in New Window
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Move...
Rename... F2
Import...
Export...
Build Project
Clean Project
Refresh F5
Close Project
Close Unrelated Projects
Build Configurations
Make Targets
Index
Convert To...
Run As
Debug As
Profile As
Team
Compare With
Restore from Local History...
Nios II
Update Linked Resources
Properties Alt+Enter
BSP Editor...
Nios II Command Shell...
Flash Programmer...
rom Nios II!\n");
d of configuration Nios II for project Hello_Nios ****

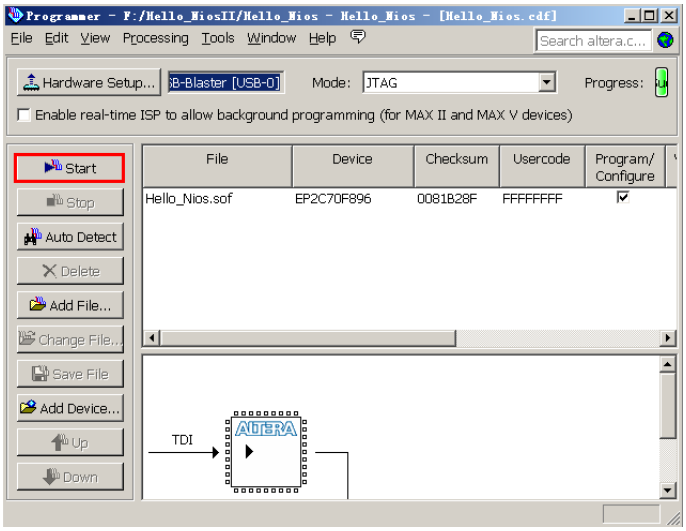

Nios II BSP Editor - F:\Hello_NiosII\software\Hello_Nios_bsp\settings.bsp
File Edit Tools Help
Main Software Packages Drivers Linker Script Enable File Generation Target BSP Directory
SOPC Information file: F:\Hello_NiosII\NIOS_CPU.sopcinfo
CPU name: cpu
Operating system: Altera HAL
Version: default
BSP target directory: F:\Hello_NiosII\software\Hello_Nios_bsp
Settings
Common
hal
enable_gprof
enable_reduced_device_drivers
enable_sim_optimize
enable_small_c_library
stderr
stdin
stdout
sys_clk_timer
timestamp_timer
linker
enable_exception_stack
enable_interrupt_stack
exception_stack_memory_region_r
exception_stack_size
interrupt_stack_memory_region_na
interrupt_stack_size
hal
enable_gprof
enable_reduced_device_drivers
enable_sim_optimize
enable_small_c_library
stderr:
jtag_uart
stdin:
jtag_uart
stdout:
jtag_uart
sys_clk_timer:
Information Problems Processing
Setting "hal.linker.interrupt_stack_memory_region_name" set to "onchip_memory".
Setting "hal.linker.exception_stack_memory_region_name" set to "onchip_memory".
Loading drivers from ensemble report.
Mapped module: "cpu" to use the default driver version.
Mapped module: "jtag_uart" to use the default driver version.
Mapped module: "sysid" to use the default driver version.
Finished loading drivers from ensemble report.
Loading BSP settings from settings file.
Finished loading SOPC Builder system info file "F:\Hello_NiosII\NIOS_CPU.sopcinfo"
Generate
Exit


Nios II BSP Editor - F:\Hello_NiosII\software\Hello_Nios_bsp\settings.bsp
File Edit Tools Help
Main Software Packages Drivers Linker Script Enable File Generation Target BSP Directory
SOPC Information file: F:\Hello_NiosII\NIOS_CPU.sopcinfo
CPU name: cpu
Operating system: Altera HAL
Version: default
BSP target directory: F:\Hello_NiosII\software\Hello_Nios_bsp
Settings
Common
hal
enable_gprof
enable_reduced_device_drivers
enable_sim_optimize
enable_small_c_library
stderr
stdin
stdout
sys_clk_timer
timestamp_timer
linker
make
Advanced
hal.linker
enable_exception_stack
enable_interrupt_stack
exception_stack_memory_region_name:
onchip_memory
exception_stack_size:
1024
interrupt_stack_memory_region_name:
onchip_memory
interrupt_stack_size:
1024
Information Problems Processing
Setting "hal.linker.interrupt_stack_memory_region_name" set to "onchip_memory".
Setting "hal.linker.exception_stack_memory_region_name" set to "onchip_memory".
Loading drivers from ensemble report.
Mapped module: "cpu" to use the default driver version.
Mapped module: "jtag_uart" to use the default driver version.
Mapped module: "sysid" to use the default driver version.
Finished loading drivers from ensemble report.
Loading BSP settings from settings file.
Finished loading SOPC Builder system info file "F:\Hello_NiosII\NIOS_CPU.sopcinfo"
Generate
Exit

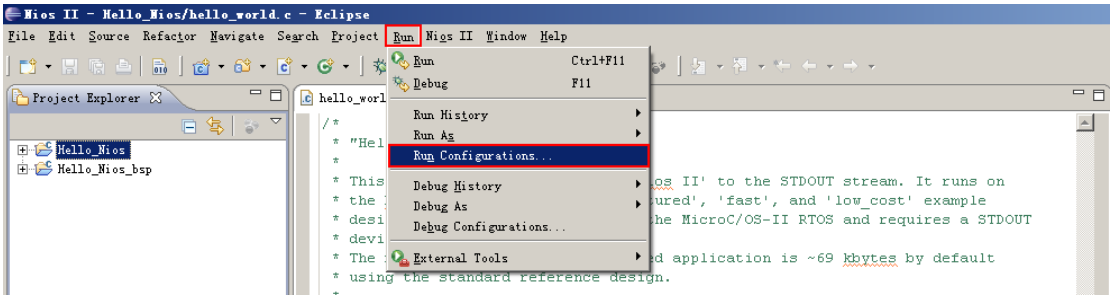
编译工程：

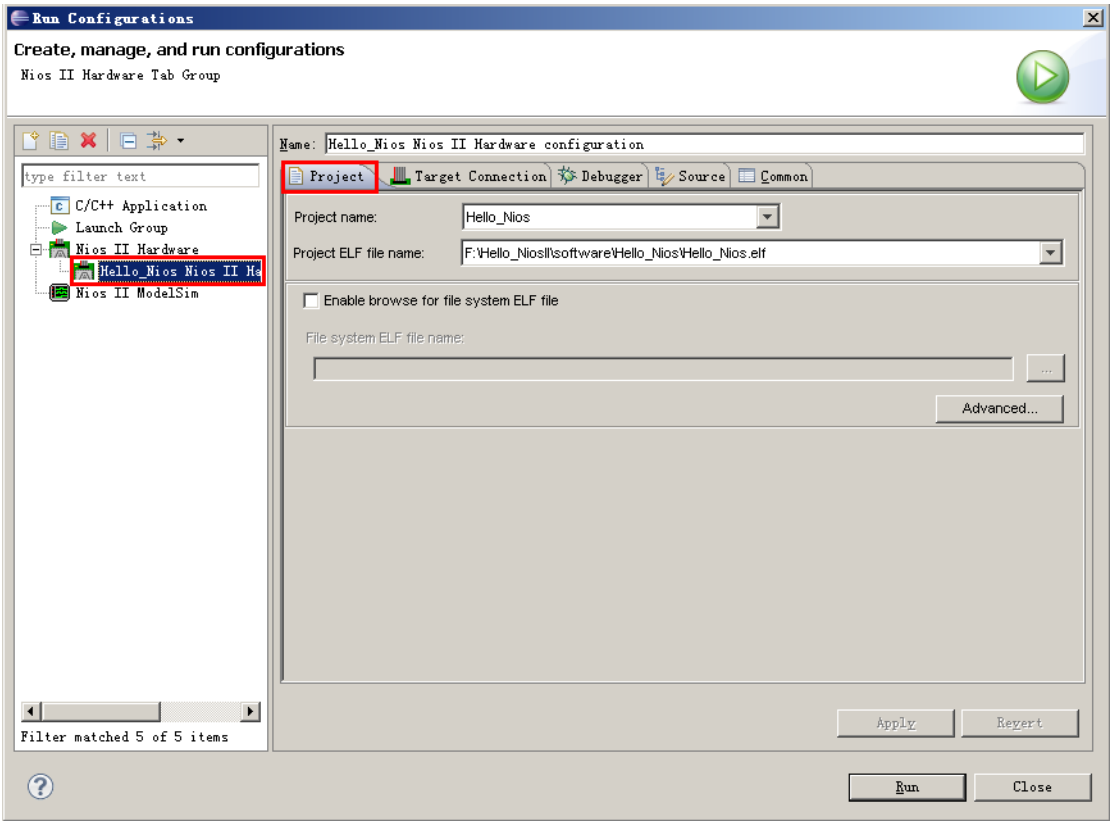


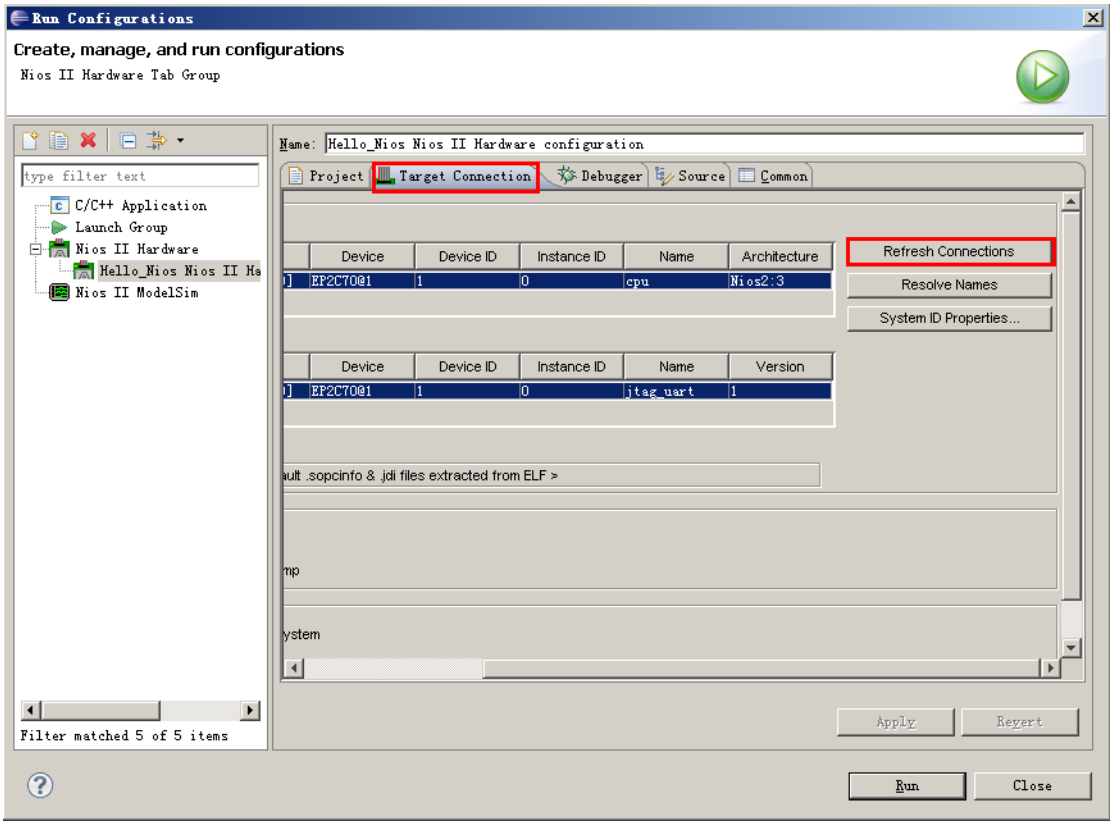
编译完成并无误后，先将硬件下载至 FPGA 中：

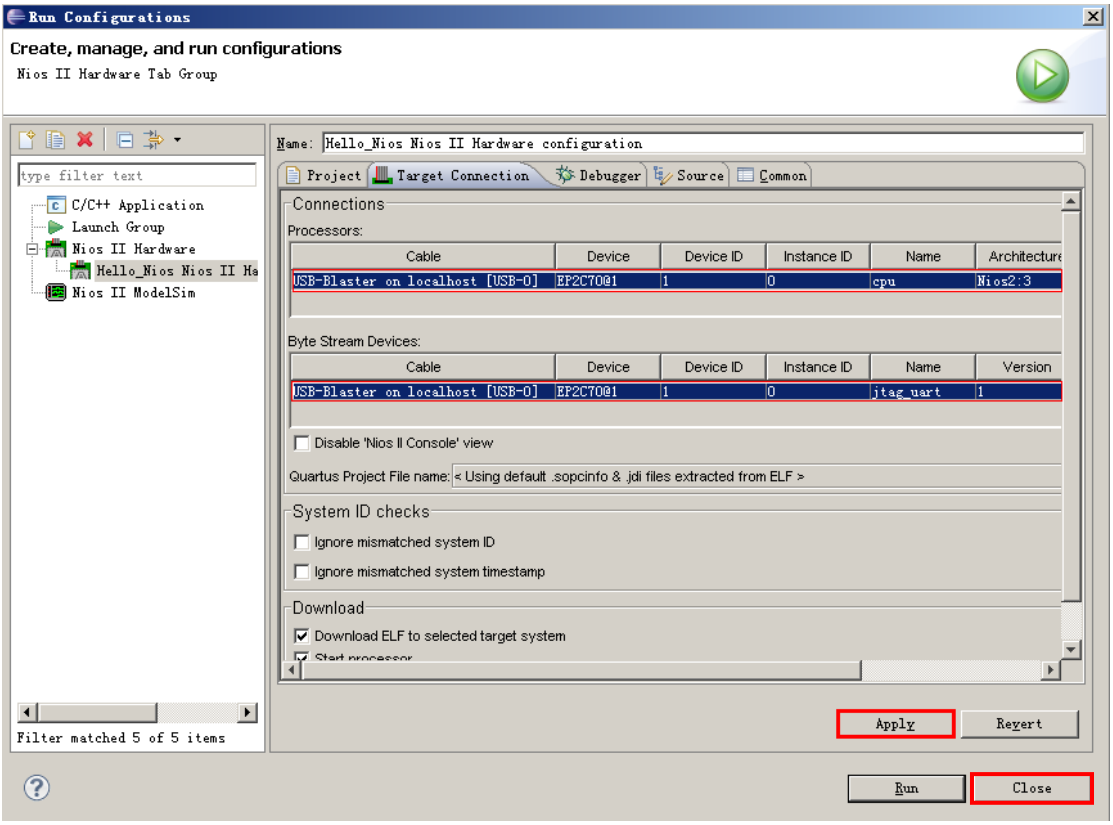


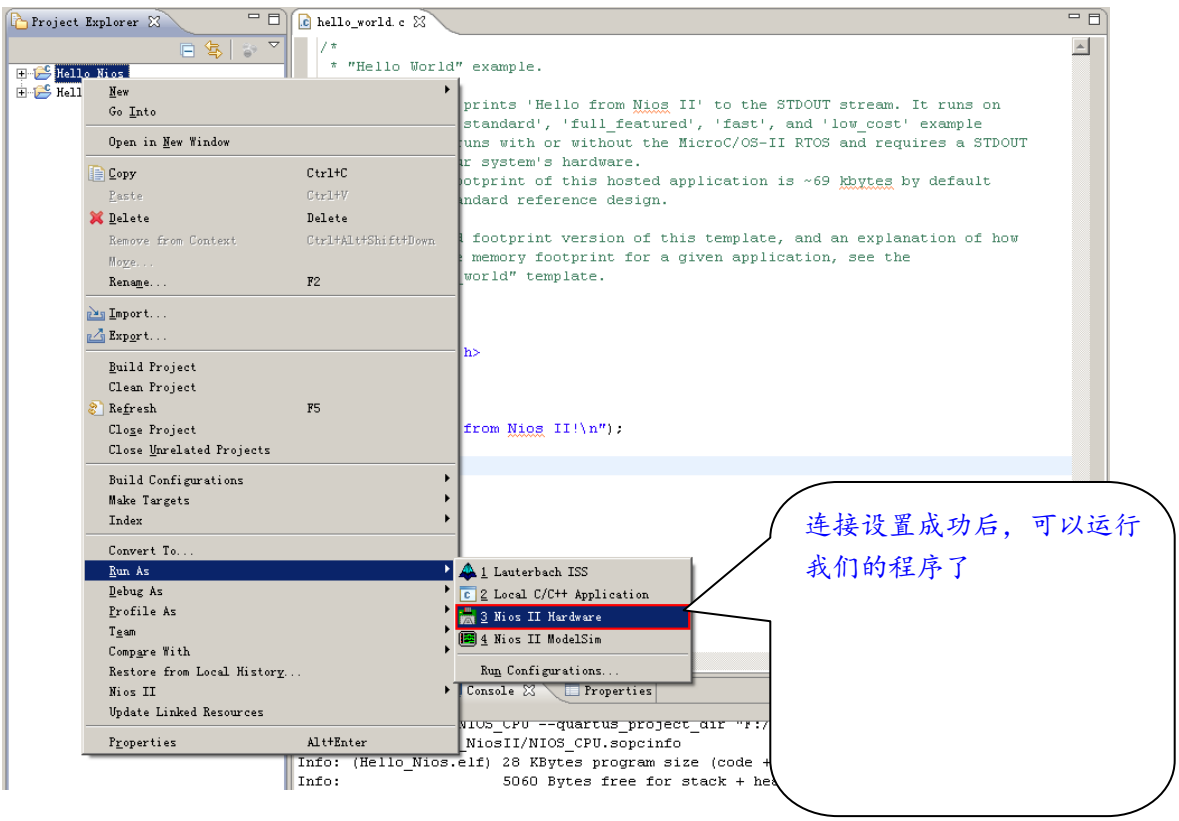
在 NIOS 中进行硬件连接的设置

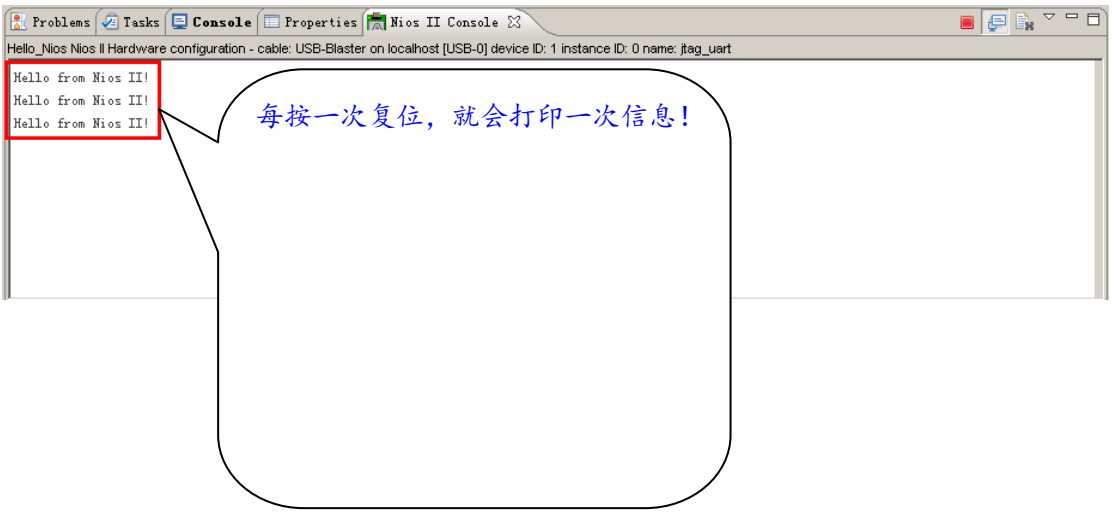



Run Configurations
Create, manage, and run configurations
Nios II Hardware Tab Group
type filter text
C/C++ Application
Launch Group
Nios II Hardware
Hello_Nios Nios II He
Nios II ModelSim
Filter matched 5 of 5 items
Name: Hello_Nios Nios II Hardware configuration
Project
Target Connection
Debugger
Source
Common
Project name:
Hello_Nios
Project ELF file name:
F:\Hello_NiosII\software\Hello_Nios\Hello_Nios.elf
Enable browse for file system ELF file
File system ELF file name:
Advanced...
Apply
Revert
Run
Close


Run Configurations
Create, manage, and run configurations
Nios II Hardware Tab Group
type filter text
C/C++ Application
Launch Group
Nios II Hardware
Hello_Nios Nios II Ha
Nios II ModelSim
Filter matched 5 of 5 items
Name: Hello_Nios Nios II Hardware configuration
Project
Target Connection
Debugger
Source
Common
Device
Device ID
Instance ID
Name
Architecture
EP2C70@1
1
0
cpu
Nios2:3
Refresh Connections
Resolve Names
System ID Properties...
Device
Device ID
Instance ID
Name
Version
EP2C70@1
1
0
jtag_uart
1
ault .sopcinfo & .jdi files extracted from ELF >
mp
ystem
Apply
Revert
Run
Close


Run Configurations
Create, manage, and run configurations
Nios II Hardware Tab Group
Name: Hello_Nios Nios II Hardware configuration
type filter text
C/C++ Application
Launch Group
Nios II Hardware
Hello_Nios Nios II Ha
Nios II ModelSim
Filter matched 5 of 5 items
Project
Target Connection
Debugger
Source
Common
Connections
Processors:
Cable
Device
Device ID
Instance ID
Name
Architecture
USB-Blaster on localhost [USB-0]
EP2C70@1
1
0
cpu
Nios2:3
Byte Stream Devices:
Cable
Device
Device ID
Instance ID
Name
Version
USB-Blaster on localhost [USB-0]
EP2C70@1
1
0
jtag_uart
1
Disable 'Nios II Console' view
Quartus Project File name: < Using default .sopcinfo & .jdi files extracted from ELF >
System ID checks
Ignore mismatched system ID
Ignore mismatched system timestamp
Download
Download ELF to selected target system
Apply
Revert
Run
Close


Project Explorer
hello_world.c
Hello_Nios
New
Go Into
Open in New Window
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Move...
Rename... F2
Import...
Export...
Build Project
Clean Project
Refresh F5
Close Project
Close Unrelated Projects
Build Configurations
Make Targets
Index
Convert To...
Run As
Debug As
Profile As
Team
Compare With
Restore from Local History...
Nios II
Update Linked Resources
Properties Alt+Enter
1 Lauterbach ISS
2 Local C/C++ Application
3 Nios II Hardware
4 Nios II ModelSim
Run Configurations...
Console
Properties
NiosII/NIOS_CPU.sopcinfo
Info: (Hello_Nios.elf) 28 KBytes program size (code +
Info: 5060 Bytes free for stack + he
连接设置成功后，可以运行我们的程序了


Problems
Tasks
Console
Properties
Nios II Console
Hello_Nios Nios II Hardware configuration - cable: USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: jtag_uart
Hello from Nios II!
Hello from Nios II!
Hello from Nios II!
每按一次复位，就会打印一次信息！