FPD-Link™ Overview



Ethernet & FPD-Link™ (EFL) Product Line Santa Clara, CA, USA



Agenda

- Introduction
- FPD-Link overview
- FPD-Link III for Infotainment
- FPD-Link IV for Infotainment

FPD-Link™ & Ethernet



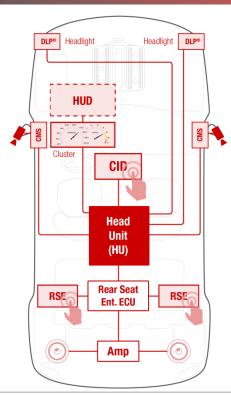
Infotainment FPD-Link™

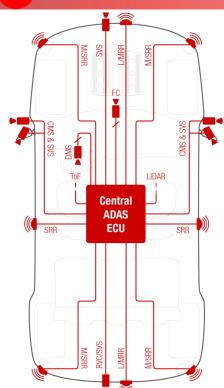


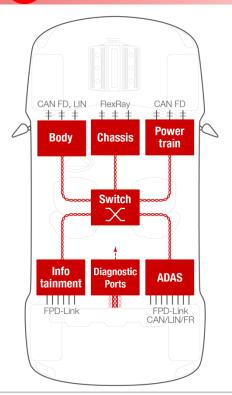
■ ADAS FPD-Link™



Ethernet Domain









TI Automotive Connectivity Solutions

FPD-Link™ Parallel Data Clock

Embedded Clock and Control

High-Speed & High-Resolution Real Time Connections

ADAS

- SVS, CVS, RVC, DMS, FVC
- Raw streaming object data from smart sensors

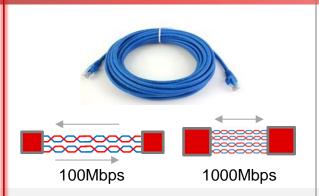
Infotainment

Control

- Cluster, RSE, CID, HUD
- CMS, Rear View Mirrors



Ethernet AEC-Q100



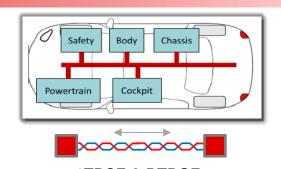
External Gateways

Firmware & OBD

- Diagnostics
- Firmware Upgrades
- Navigation



Auto PHYTER



1TPCE & RTPGE

Domain-Domain Connections

Backbone

Connects between domains

ADAS

- Pre-processed object data from smart sensors
- Raw data from low data-rate sensors

BCM

Connects Flexray, CAN, LIN





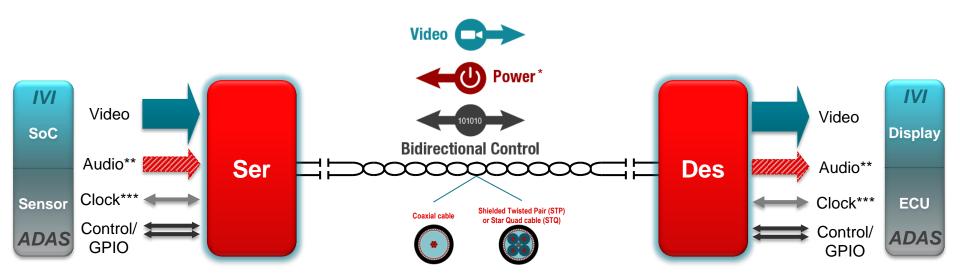


What is FPD-Link™

- What does FPD-Link™ stand for?
 - Short for Flat Panel Display Link
- What does it do?
 - Transports high-speed data such as video over a twisted pair or coax cable
 - Supports a variety of video interfaces (RGB, OpenLDI (LVDS), MIPI CSI-2 & DSI, HDMI)
 - Aggregates video, audio and clock as well as bi-directional data onto one stream
- What are the use-cases?
 - Automotive Infotainment & Cluster: data transfer between ECU and display
 - Automotive ADAS: data transfer between imagers, radar or other sensors to ECU

Common Automotive Video Links

with FPD-Link™



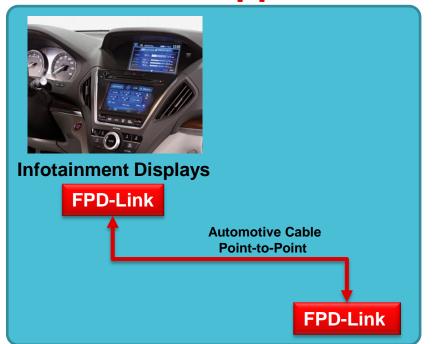


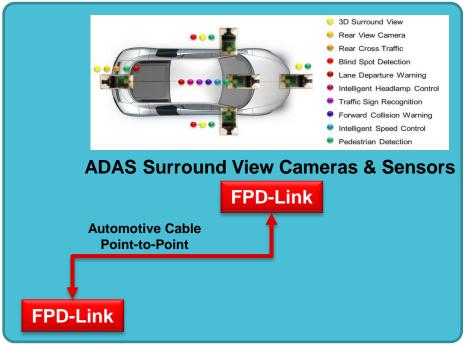
^{*:} optional for ADAS devices (Power over Coax [PoC])

^{**:} optional on certain IVI devices

^{***:} SER → DES for IVI devices | DES → SER for ADAS devices

FPD-Link™ Applications





Head-Unit With ECU



Aggregation of video, audio, GPIO, control (I²C, I²S) over one link and backward control

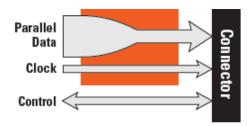


FPD-Link™ Legacy

FPD-Link I

FPD-Link II

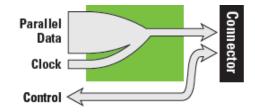
FPD-Link III



Parallel Clock

Many to Less

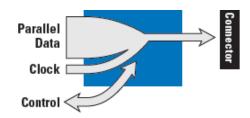
- 3/4 Data + 1 Clock = 8 wires
- Cable length ~ 3 meter
- Lower EMI



Embedded Clock

Many to One

- 2 wires (plus control)
- Up to 1.8 Gbps
- Cable length > 10 meter
- Reduced weight
- No ground currents on cable
- AEC-Q100, ISO 10605



Embedded Clock and Control

Do More (on One)

- · 2 wires only
- Up to 3 Gbps
- HDCP content protection (optional)
- Embedded control channel
- Adaptive equalization
- Built-in Diagnostics
- AEC-Q100, ISO 10605
- Great variety of video interfaces: RGB, OpenLDI (LVDS), MIPI CSI-2 & DSI. HDMI

...plus power transfer (PoC)!



9

FPD-Link Highlights

General

- Video, Bidirectional Control (I2C, SPI), GPIO and Power
 - Over single twisted pair or coaxial cable assemblies
- Adaptive equalization compensates for cable type, length, age and condition
- Multiple interface options: RGB, YUV, OpenLDI (LVDS), MIPI CSI-2 & DSI, HDMI

Infotainment



- Support for 720p, 1080p & 2K/3K
- Easy-to-use HDCP content protection
- Dithering, White Balance, and Test Patterns
- I²S audio plus I²S clock cleaning

ADAS

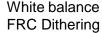


- Support for 1 and 2 Megapixel image sensors
- Very low latency
- Synchronized sensors with system clock → no oscillator on sensor side
- Easy frame synchronization using GPIO
- Deserializers with 2:1 input mux











High-bandwidth **Digital Content Protection**



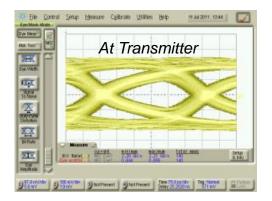


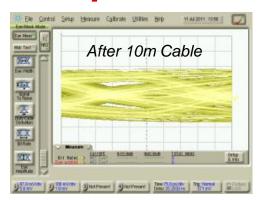


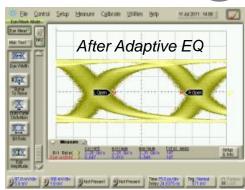


Advanced Adaptive Equalization





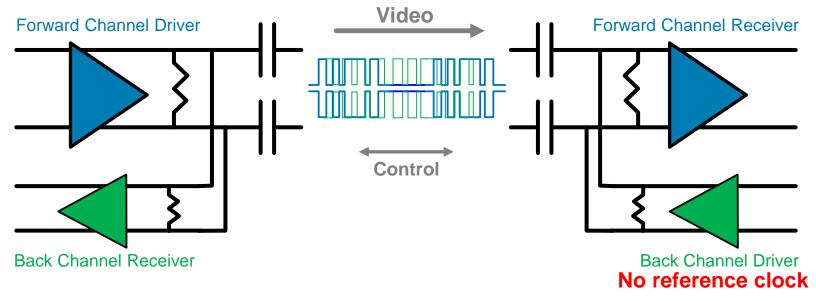




- Automatic algorithm
 - No adjustment compensates for cable type, length, connectors, etc
 - Adapts during power up
- Compensates for cable ageing effects
- No EMI impact
- Diagnostic function
 - Read out EQ level to monitor cable health
- Supports future data rates over low cost cables

Continuous, Low-Latency Backchannel





- Ultra-low (<15µs) latency
 - Ideal for remote ISP & camera sync control
- EMI friendly
 - No common mode modulation
 - No pre-emphasis or tuning

- No waiting for video blanking
 - Backchannel sent continuously
- Single pair
 - Works over coax & STP

Link Diagnostics: Layered Protection



12	Pattern Generation	Generates video patterns for test	test mode
11	BIST	Bit error rate test	test mode
10	Prog. Interrupt	Programmable open drain interrupt pin flags errors to processor	always active
9	Prog. Alarm Bit *	Programmable alarm signal provides module health monitoring	always active
8	Voltage/Temp Meas *	Monitors up to 2 voltages as well as internal temperature	always active
7	Frame Count	Verifies no frozen frames (note: frame count is sent by imager)	always active
6	I2C Write Protect *	Protects sensor module misconfiguration if I2C has bit errors	always active
6	CSI-2 CRC *	Verifies end-to-end link integrity and bit error rate	always active
5	SerDes CRC	Verifies SerDes link integrity and bit error rate	always active
4	CSI-2 Input Check *	Checks for data integrity from sensor data at input to 953	always active
3	Lock Detect	Verifies link established	always active
4	Internal Oscillator	Internal serializer oscillator establishes link even without clock	always active
2	Adaptive EQ Level	Read relative cable quality via I2C (7 levels)	set at power up
1	Link Fault Detect	Cable open, + to - short, short to ground, short to battery, incorrect link	always active

*: 953/954 for ADAS only

test mode

norm

normal operation

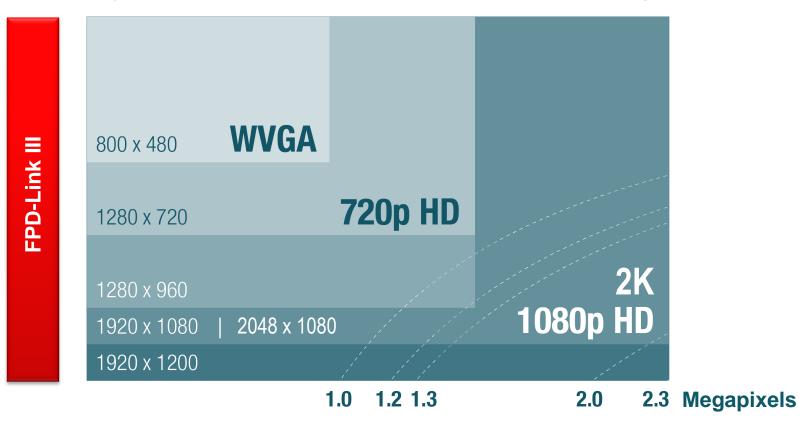


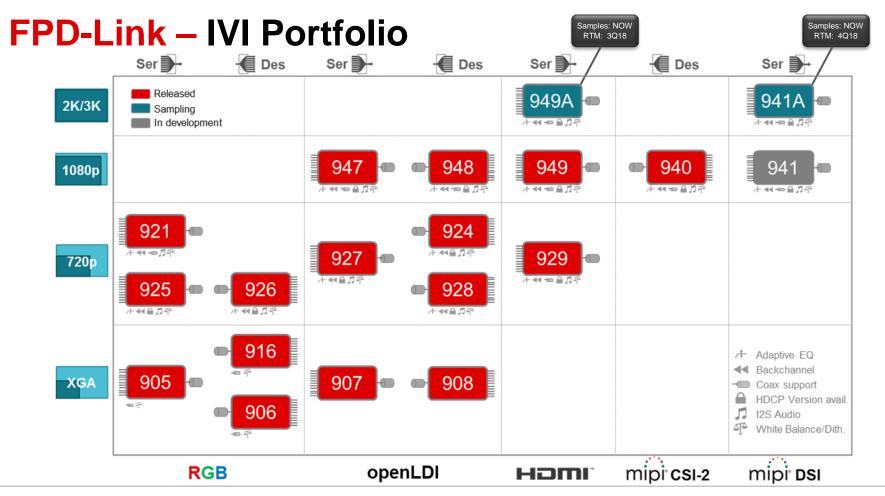
FPD-Link III

Infotainment



Display & Camera Resolutions – today





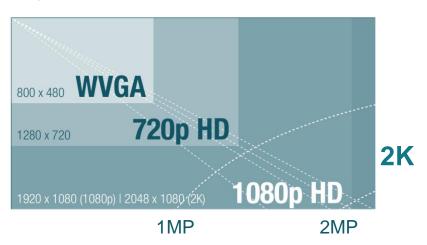
FPD-Link IV

Infotainment



Display & Camera Resolutions – next generation





Next generation display & camera requirements

	Horizontal	Vertical	Mega		Data Rate (Mbps)						
	Hres	Vres	pixels	Blanking	30 fps			60 fps Bits per pixel			
					Bits per pixel						
Format	(pixels)	(pixels)	(MP)	Factor	12	24	28	12	24	28	30
QVGA	320	240	0.08	1.10	30.4	60.8	71.0	60.8	121.7	141.9	152.1
VGA/NTSC	640	480	0.31	1.10	121.7	243.3	283.9	243.3	486.6	567.7	608.3
PAL	768	576	0.44	1.10	175.2	350.4	408.7	350.4	700.7	817.5	875.9
WVGA	800	480	0.38	1.10	152.1	304.1	354.8	304.1	608.3	709.6	760.3
SVGA	800	600	0.48	1.10	190.1	380.2	443.5	380.2	760.3	887.0	950.4
WSVGA	1024	600	0.61	1.10	243.3	486.6	567.7	486.6	973.2	1135.4	1216.5
XGA	1024	768	0.79	1.10	311.4	622.9	726.7	622.9	1245.7	1453.3	1557.1
720p HD	1280	720	0.92	1.10	365.0	729.9	851.6	729.9	1459.8	1703.1	1824.8
WXGA	1280	768	0.98	1.10	389.3	778.6	908.3	778.6	1557.1	1816.7	1946.4
	1280	960	1.23	1.10	486.6	973.2	1135.4	973.2	1946.4	2270.8	2433.0
SXGA	1280	1024	1.31	1.10	519.0	1038.1	1211.1	1038.1	2076.2	2422.2	2595.2
SAGA	1280	1080	1.38	1.10	547.4	1094.9	1277.3	1094.9	2189.7	2554.7	2737.2
	1920	720	1.38	1.10	547.4	1094.9	1277.3	1094.9	2189.7	2554.7	2737.2
1080p Full HD	1920	1080	2.07	1.10	821.1	1642.3	1916.0	1642.3	3284.6	3832.0	4105.7
WUXGA	1920	1200	2.30	1.10	912.4	1824.8	2128.9	1824.8	3649.5	4257.8	4561.9
2K	2048	1080	2.21	1.10	875.9	1751.8	2043.7	1751.8	3503.6	4087.5	4379.4
2K (WQHD)	2560	1440	3.69	1.10	1459.8	2919.6	3406.2	2919.6	5839.3	6812.5	7299.1
4K (UHD-1/UHDTV)	3840	2180	8.37	1.10	3315.0	6630.0	7735.0	6630.0	13260.0	15470.0	16575.0
4K (DCI)	4096	2160	8.85	1.10	3503.6	7007.1	8175.0	7007.1	14014.2	16349.9	17517.8
		Multiply data rate by 2x for YUV forma									

Next generation
display
technology
requires >12Gbps
video data rate

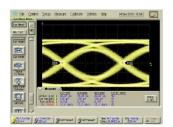


FPD-Link IV technology enables

- 4K video (and beyond), audio and control transport
- New features such as
 - Daisy-chaining

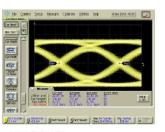
- New interfaces (e.g. DP/eDP)
- Image aggregation
- Higher data rate backchannel (100Mbps Ethernet)

- Image splitting
- Higher data rate using existing automotive connector/cable infrastructure



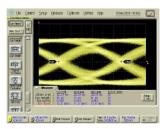
10m Dacar 302 (RTK031)

-15.05 dB @ 6GHz EQ Step = 0x03 (9.1dB @ 6GHz) Jitter (p-p) = 22.87 ps Eye Height = 130 mV Eye Width = 0.749 UI



10m RG-174

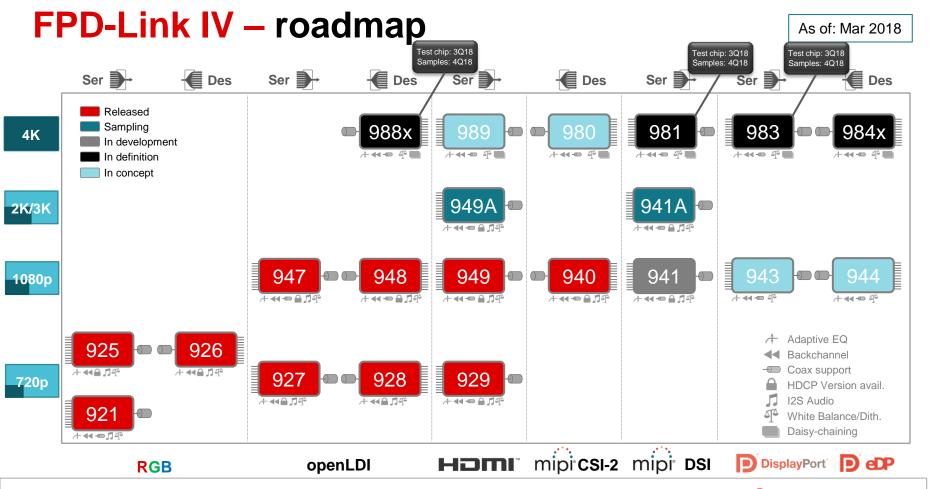
-20.62 dB @ 6GHz EQ Step = 0x07 (13.7dB @ 6GHz) Jitter (p-p) = 22.87 ps Eye Height = 139 mV Eve Width = 0.723 UI



15m RG-174

-31.26 dB @ 6GHz EQ Step = 0x1F (21.8dB @ 6GHz) Jitter (p-p) = 32.41ps Eye Height = 80 mV Eve Width = 0.588 UI 12Gbps EQ performance over **existing** coax cables





DS90UH983





FPD-Link IV DisplayPort (DP) Serializer for Ultra-High resolution



- Support of Multi-Stream Transport (MST) (via SoC) for
 - Multiple displays (image aggregation) with different resolutions
 - Daisy-chaining of up to 4 displays
- Splitting of FPD-Link 4 ports to enable Y-splitting architecture
- Supports DisplayPort HBR3 (1/2/4 lanes) up to 8.1Gbps/lane
- Link speed of 25Gbps with 12.5Gbps per pair or coax

- High Speed backchannel
 - I2C / SPI
 - GPIOs
 - 100Mbps Ethernet

DS90UH983





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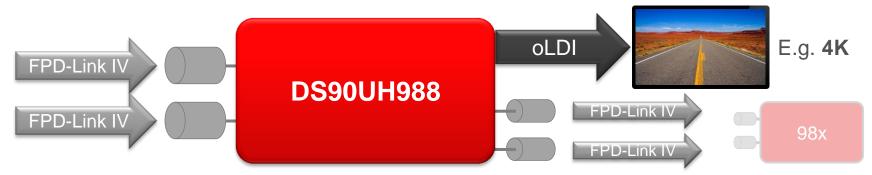
- High Speed backchannel
 - I2C / SPI
 - GPIOs
 - 100Mbps Ethernet

DS90UH988



openLDI

FPD-Link IV openLDI Deserializer for Ultra-High resolution

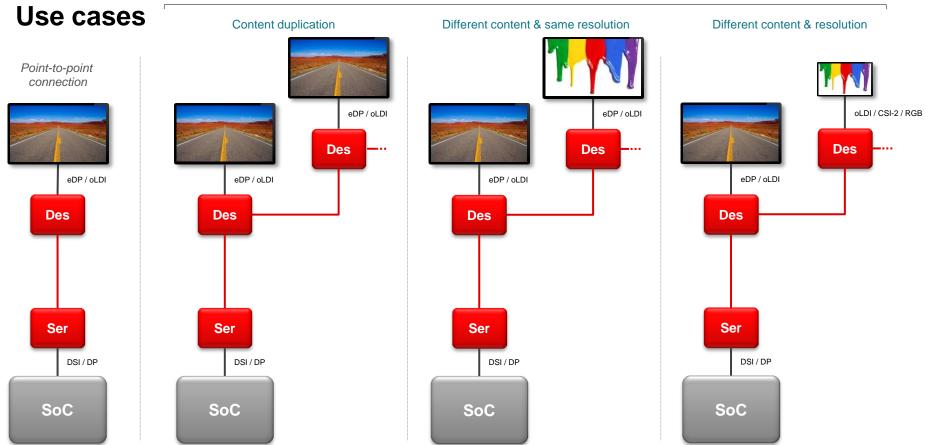


- openLDI Deserializer + FPD-Link repeater/splitter
- Deserializer can be configured as:
 - Point-to-point connection for single display
 - Daisy chaining configurations:
 - Display via oLDI + partial FPD-Link data pass-through to FPD-Link OUT
 - Repeater: Display via oLDI + full FPD-Link data passthrough to FPD-Link OUT
- Backward compatible to 94x Des for daisy-chaining (last node)

- High Speed backchannel
 - I2C / SPI
 - GPIOs
 - 100Mbps Ethernet

...next display (e.g. HUD) Deserializer





Thank you



DS90Ux983-Q1

FPD-Link IV DisplayPort (DP) Serializer for 4k+ resolution

Features

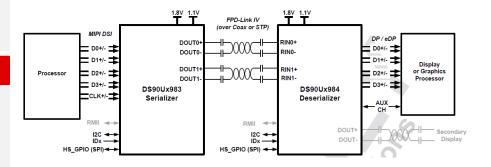
- FPD-Link 4 Video Link
- DisplayPort (DP HBR3 v1.4) support (8.1Gbps per lane)
- 25Gbps link speed via:
 - Single STQ
 - 2 x STP/SPP or Coax (12.5Gbps each)
- Multi-Stream Transport (MST) support via SoC
- I2C & SPI Compatible Serial Control Bus
- Internal Pattern Generation for Testing
- High Speed GPIO Ports
- 100Mbps Ethernet RMII
- AEC-Q100 Grade 1 (-40 to 115°C) Qualified

Applications

- Central Information Display (CID)
- Rear Seat Entertainment (RSE)
- Cluster
- Head Up Display (HUD)
- Rear View & Side Mirror Displays

Benefits

- Industry's first chipset to enable uncompressed 4K video
- Image aggregation to support multiple daisy-chained displays via DP MST
- Advanced Link robustness and EMC performance
- Enhanced Security and diagnostics features
- Higher data rate back channel with Ethernet support





DS90Ux981-Q1

FPD-Link IV MIPI DSI Serializer for 4k+ resolution

Features

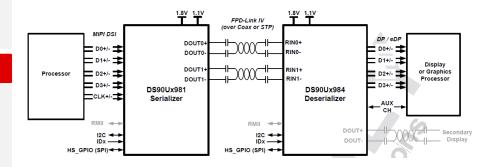
- FPD-Link 4 Video Link
- 2 MIPI DSI (D-PHY 1.2) ports (2.5Gbps per lane)
- 25Gbps link speed via:
 - Single STQ
 - 2 x STP/SPP or Coax (12.5Gbps each)
- Virtual Channel (VC) support for DSI via SoC
- I2C & SPI Compatible Serial Control Bus
- Internal Pattern Generation for Testing
- High Speed GPIO Ports
- 100Mbps Ethernet RMII
- AEC-Q100 Grade 1 (-40 to 115°C) Qualified

Applications

- Central Information Display (CID)
- Rear Seat Entertainment (RSE)
- Cluster
- Head Up Display (HUD)
- Rear View & Side Mirror Displays

Benefits

- Industry's first chipset to enable uncompressed 4K video
- Image aggregation to support multiple daisy-chained displays via MIPI DSI Virtual Channels
- Advanced Link robustness and EMC performance
- Enhanced Security and diagnostics features
- Higher data rate back channel with Ethernet support





DS90Ux988-Q1

FPD-Link IV openLDI (oLDI) Deserializer for 4k+ resolution

Features

- FPD-Link 4 Video Link
- 4 port OpenLDI interface (up to 200MHz per lane)
- 25Gbps link speed via:
 - Single STQ
 - 2 x STP/SPP or Coax (12.5Gbps each)
- Adaptive Equalization
- I2C & SPI Compatible Serial Control Bus
- Internal Pattern Generation for Testing
- High Speed GPIO Ports
- 100Mbps Ethernet RMII
- AEC-Q100 Grade 1 (-40 to 115°C) Qualified

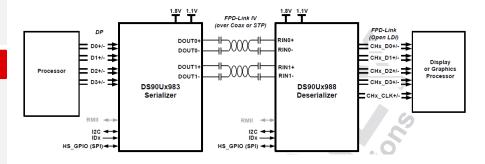
Applications

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- Cluster
- Head Up Display (HUD)
- Rear View & Side Mirror Displays

Benefits

- Industry's first chipset to enable uncompressed 4K video
- Image aggregation to support multiple daisy-chained displays via DP MST and MIPI DSI Virtual Channels
- Advanced Link robustness and EMC performance
- Enhanced Security and diagnostics features
- Higher data rate back channel with Ethernet support

9880: no daisy-chaining **9881**: daisy-chaining





DS90Ux984-Q1

FPD-Link IV DisplayPort (DP) Deserializer for 4k+ resolution

Features

- FPD-Link 4 Video Link
- DisplayPort (DP HBR3 v1.4) support (8.1Gbps per lane)
- 25Gbps link speed via:
 - Single STQ
 - 2 x STP/SPP or Coax (12.5Gbps each)
- Adaptive Equalization
- I2C & SPI Compatible Serial Control Bus
- Internal Pattern Generation for Testing
- High Speed GPIO Ports
- 100Mbps Ethernet RMII
- AEC-Q100 Grade 1 (-40 to 115°C) Qualified

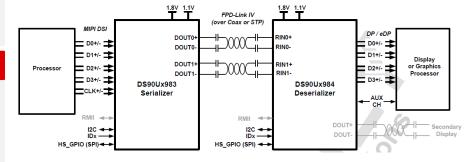
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Benefits

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- Advanced Link robustness and EMC performance
- Enhanced Security and diagnostics features
- Higher data rate back channel with Ethernet support

9840: no daisy-chaining **9841**: daisy-chaining





FPD-Link III — Driving multiple displays

