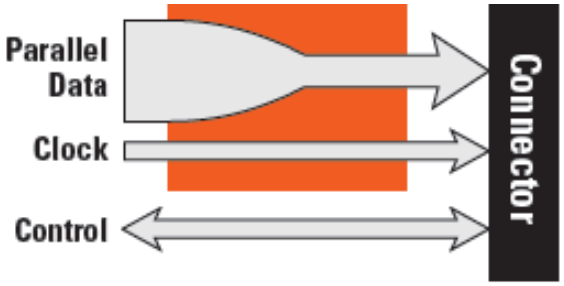
DS90UB925/926 调试

FPD-Link Evolution and Revolution

FPD-Link I

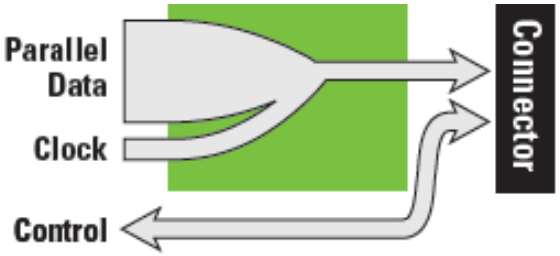


Parallel Clock

Many to Less

- 3/4 Data + 1 Clock = 8 wires
- Cable length ~ 3 meter
- Lower EMI

FPD-Link II



Embedded Clock

Many to One

- 2 wires (plus control)
- Up to 1.8 Gbps
- Cable length ≥ 10 meter
- Reduced weight
- No ground currents on cable
- AEC-Q100, ISO 10605

FPD-Link III

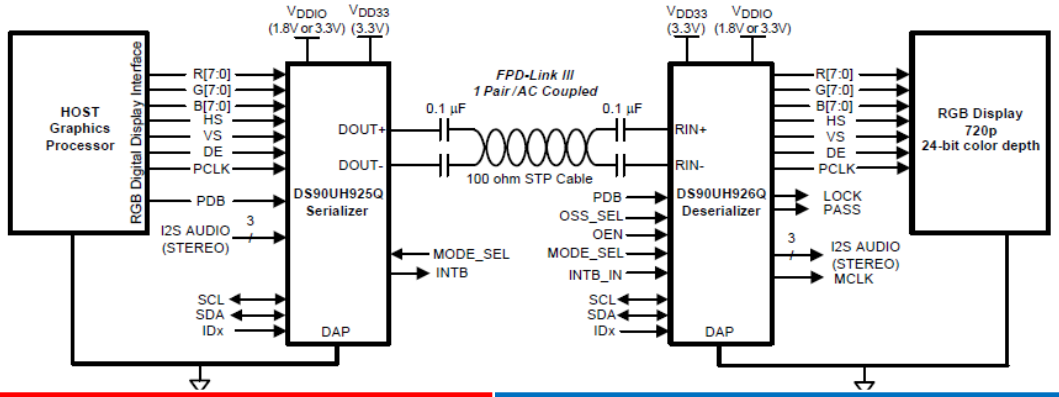
Embedded Clock and Control

Do More (on One)

- Only 2 wires
- Up to 3 Gbps
- Embedded control channel
- HDCP content protection (option)
- Adaptive equalization
- AEC-Q100, ISO 10605

…*and power transfer too!*

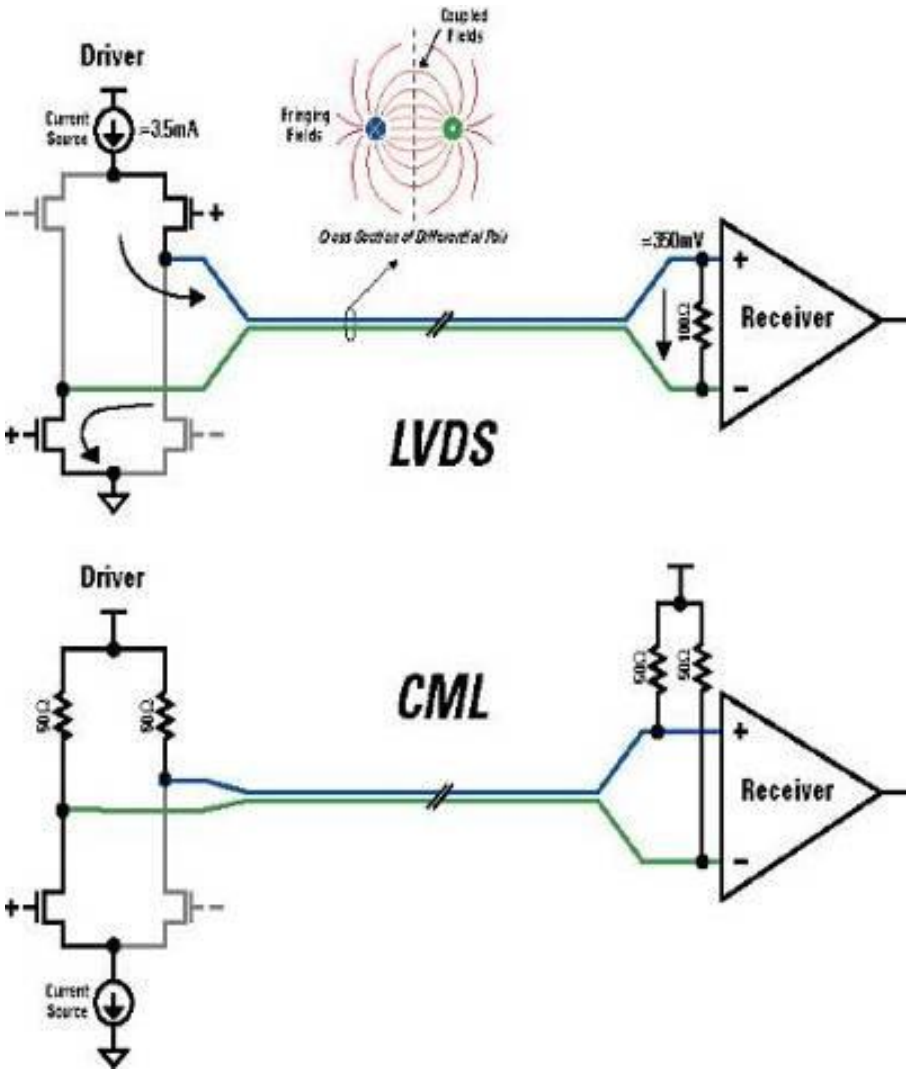
Function introduce



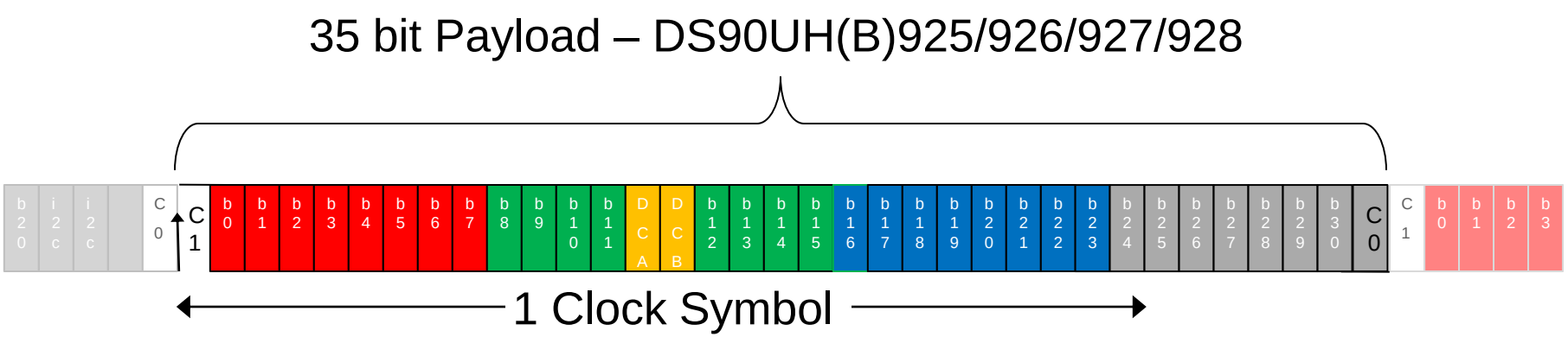
Feature	Benefit
5 – 85 MHz Pixel Clock	High def 1280 X 720p
400 kbps I2C Backchannel	Replaces CAN, LIN, MOST
2 I2S audio channels	Audio to HU or headphones
SSCG in deserializer	Reduces display EMI
Adaptive Equalization	Up to 10m at 85 MHz
FPD-Link III serialization	All on one pair of wires!
2.975Gbps bandwidth	24 bit color support
FRC dithering	Improved display on 18 bit
White balancing	Matched displays / panels

Differential Signaling I/O Structures

- Small differential swing
- Equal and opposite currents
- Wide common mode range
- High noise rejection
- Low EMI
- Technologies:
  - Low Voltage Differential Signaling (LVDS)
  - Current Mode Logic (CML)



FPD-Link III : 35 Bit Payload



C1 = Clock bit HIGH

C0 = Clock bit LOW

DCA & DCB = Link Overhead

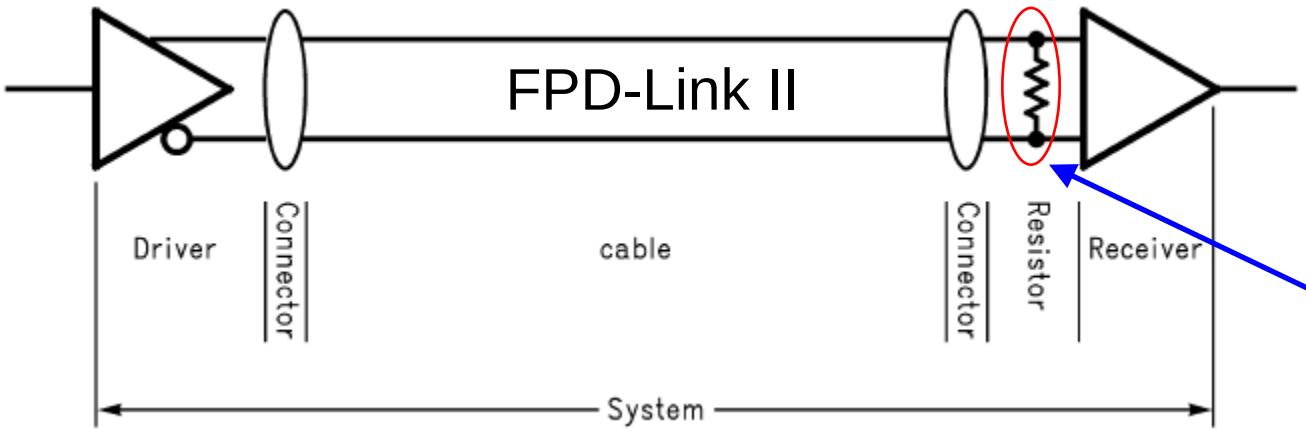
24-bit RGB + I2S audio + I2C + HDCP

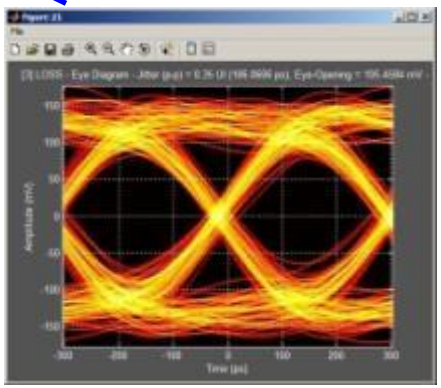
(encoded Sync)

Note: Payload bits are *Randomized, Balanced & Scrambled*
*Serial line rate = pixel clock * payload size (bits per pclk)*
For example @ pclk = 75MHz:
*serial line rate = 75MHz * 35 bits/pclk = 2625Mbps*

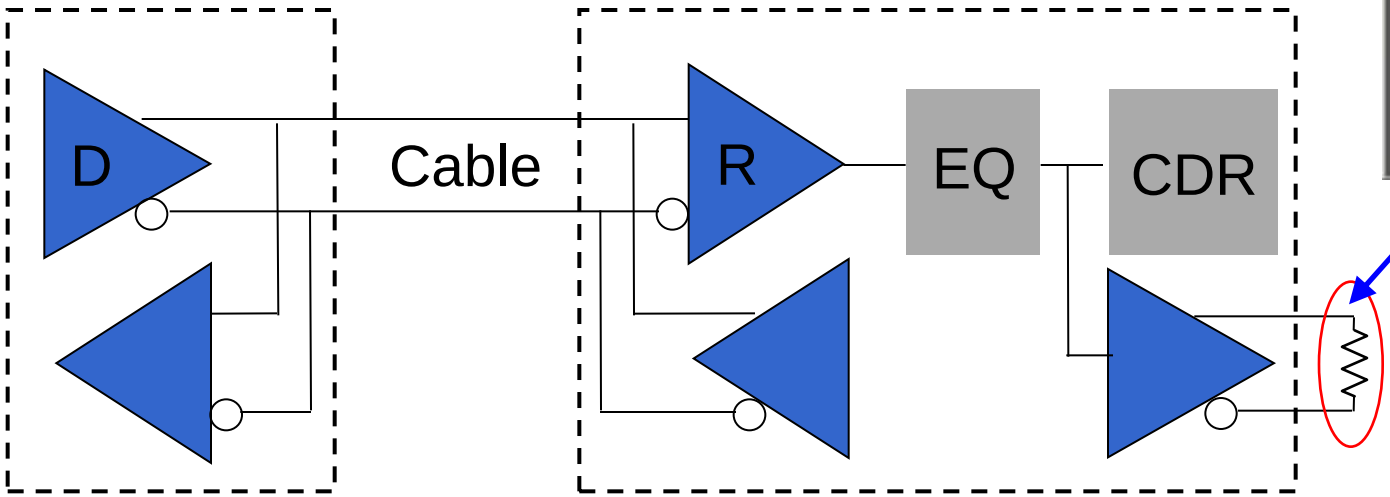
Differential signal probing

DS90UB926
1. 0x56 register bit 3, CML output enable.
2. External 100ohm resistor

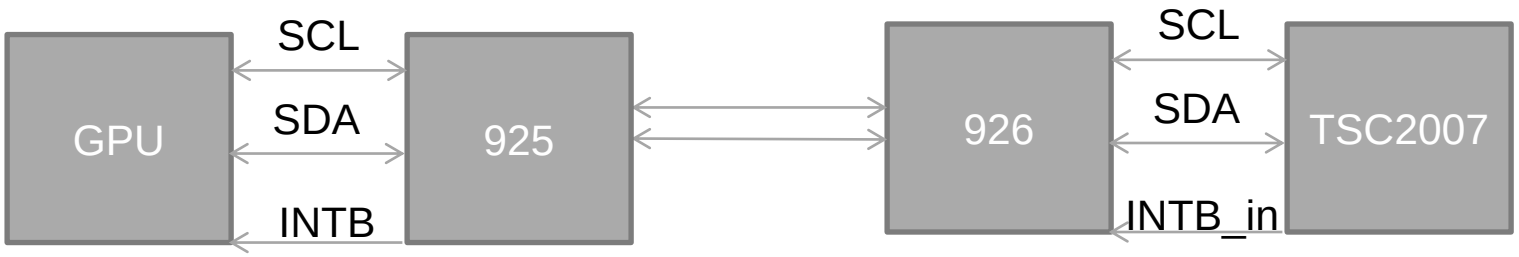




FPD-Link III



Interrupt



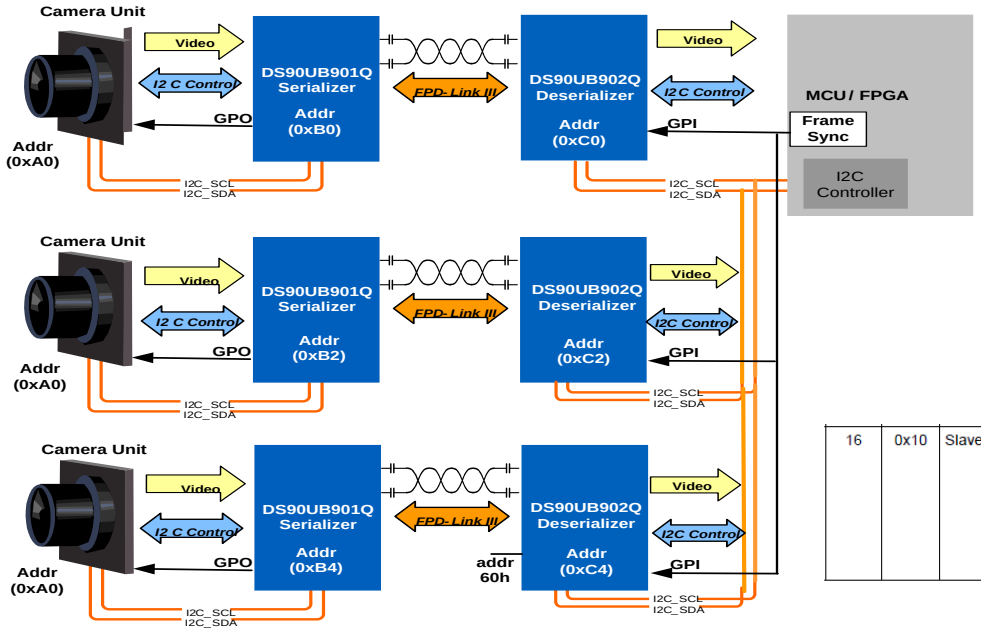
- 1. On DS90UH925, set register 0xC6[5] = 1 and 0xC6[0] = 1
- 2. DS90UH926Q deserializer INTB_IN (pin 16) is set LOW by some downstream device.
- 3. DS90UH925Q serializer pulls INTB (pin 31) LOW. The signal is active low, so a LOW indicates an interrupt
- condition.
- 4. External controller detects INTB = LOW; to determine interrupt source, read HDCP_ISR register .
- 5. A read to HDCP_ISR will clear the interrupt at the DS90UH925, releasing INTB.
- 6. The external controller typically must then access the remote device to determine downstream interrupt
- source and clear the interrupt driving INTB_IN. This would be when the downstream device releases the
- INTB_IN (pin 16) on the DS90UH926Q. The system is now ready to return to step (1) at next falling edge of
- INTB_IN.

I2C speed

38	0x26	SCL High Time	7:0	RW	0x83	SCL High Time	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Deserializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
39	0x27	SCL Low Time	7:0	RW	0x84	SCL Low Time	I2C SCL Low Time This field configures the low pulse width of the SCL output when the De-Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.

- Default value: period 13.1us, 76k.
- If want 400k, period 2.5us, 2500/2/50=25
- 0x26,0x27 set to 0x19

Remote Device Address

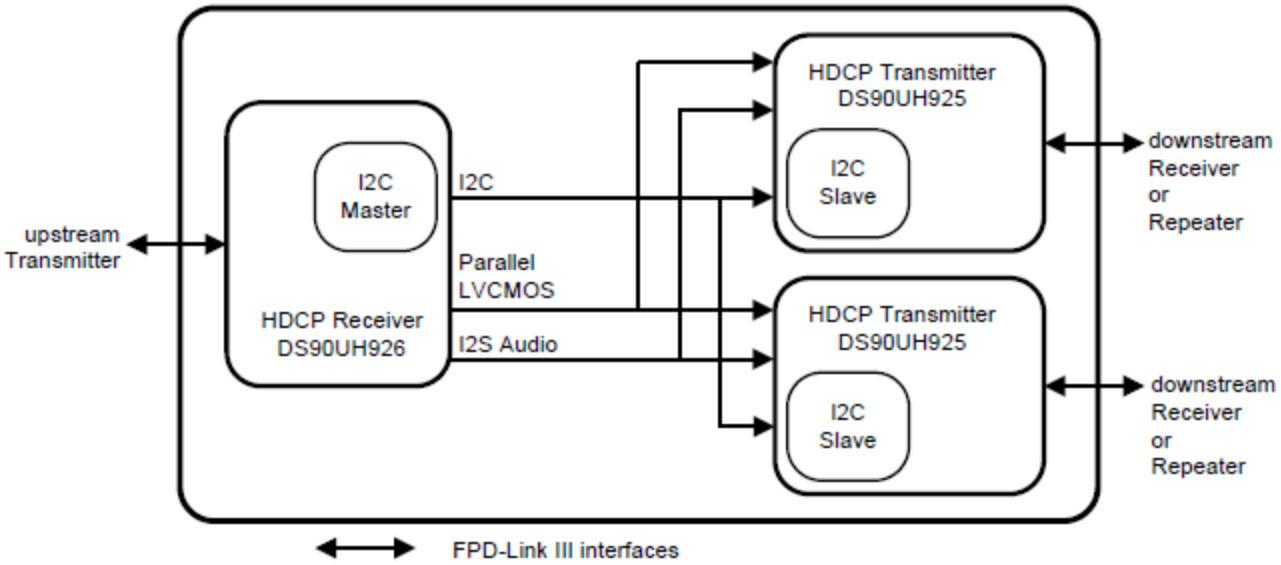


- synchronize multiple cameras/panel
- simplify camera/panel module development & repair

16	0x10	SlaveAlias[0]	7:1	RW	0x00	ID[0] Match	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***

7	0x07	Remote Device ID	7:1	RW	0x18	Remote ID	Remote ID Configures the I2C Slave ID of the remote Serializer. A value of 0 in this field disables I2C access to remote Serializer. This field is automatically configured via the Serializer Forward Channel. Software may overwrite this value, but should also set the FREEZE DEVICE ID bit to prevent overwriting by the Forward Channel.
			0	RW		Freeze Device ID	Freeze Serializer Device ID 1: Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written. 0: Update
8	0x08	SlaveID[0]	7:1	RW	0x00	Target Slave Device ID0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				***Reserved***

Repeater function



1. Video Data – Connect PCLK, RGB and control signals (DE, VS, HS).
2. I2C – Connect SCL and SDA signals. Both signals should be pulled up to VDD33 with 4.7 kΩ resistors
3. Audio – Connect I2S_CLK, I2S_WC, and I2S_DA signals.
4. IDx pin – Each HDCP Transmitter and Receiver must have an unique I2C address.
5. MODE_SEL pin – All HDCP Transmitter and Receiver must be set into the Repeater Mode.
6. Interrupt pin– Connect DS90UH926Q INTB_IN pin to DS90UH925Q INTB pin. The signal must be pulled up to VDDIO.

ESD

ESD Rating (IEC, powered-up only), R_D = 330Ω, C_S = 150pF	Air Discharge (R_{IN+}, R_{IN-})	≥±15 kV
	Contact Discharge (R_{IN+}, R_{IN-})	≥±8 kV
ESD Rating (ISO10605), R_D = 330Ω, C_S = 150pF	Air Discharge (R_{IN+}, R_{IN-})	≥±15 kV
	Contact Discharge(R_{IN+}, R_{IN-})	≥±8 kV
ESD Rating (ISO10605), R_D = 2kΩ, C_S = 150 & 330pF	Air Discharge (R_{IN+}, R_{IN-})	≥±15 kV
	Contact Discharge (R_{IN+}, R_{IN-})	≥±8 kV
ESD Rating (HBM)		≥±8 kV
ESD Rating (CDM)		≥±1.25 kV
ESD Rating (MM)		≥±250 V

- The ESD protection circuitry operates by shunting the energy during an ESD event to ground. This is done to protect the device circuit from damage. The signal line (device pin) that is “protected” will be shorted to ground during the ESD event. This will corrupt the data being transmitted at the time of the ESD event. We incorporate ESD protection circuits internally at the pins of our devices to guarantee that the parts will not suffer any permanent damage during an ESD event. Automotive requirements are quite stringent, and thus very robust circuits are developed to support this need. The ability to protect from damage and recover without any intervention (i.e. applying reset) is a critical feature.
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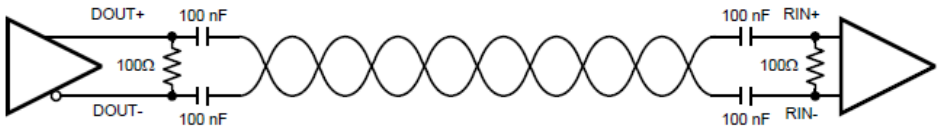
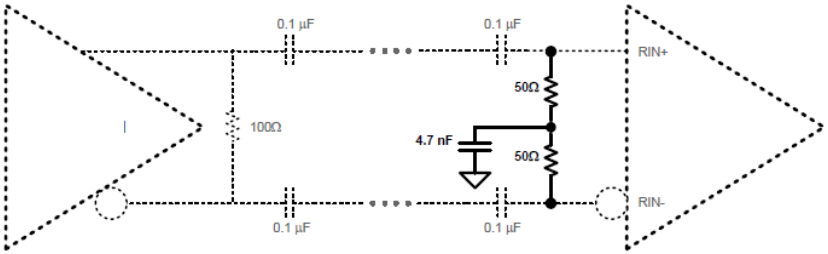
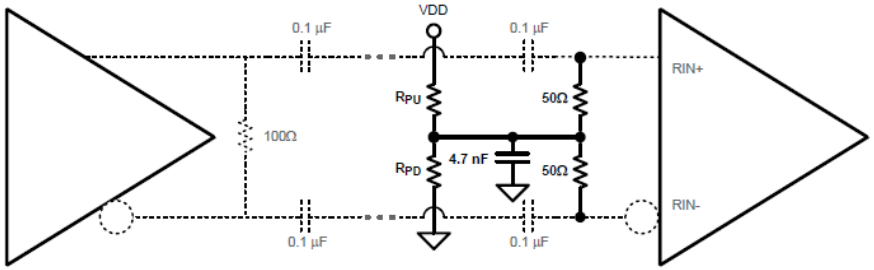
- We cannot guarantee that there will be no corruption of data (loss in transmission). From a system perspective the user impact could be minimized. One option would be to use the LOCK pin as an indicator to control the display. If the ESD event leads to a loss of LOCK (likely), this status pin of the DES could be used to initiate a fail-safe condition to the display (turn-off backlight, drive alternate image) until LOCK is stable.

Receiver Termination





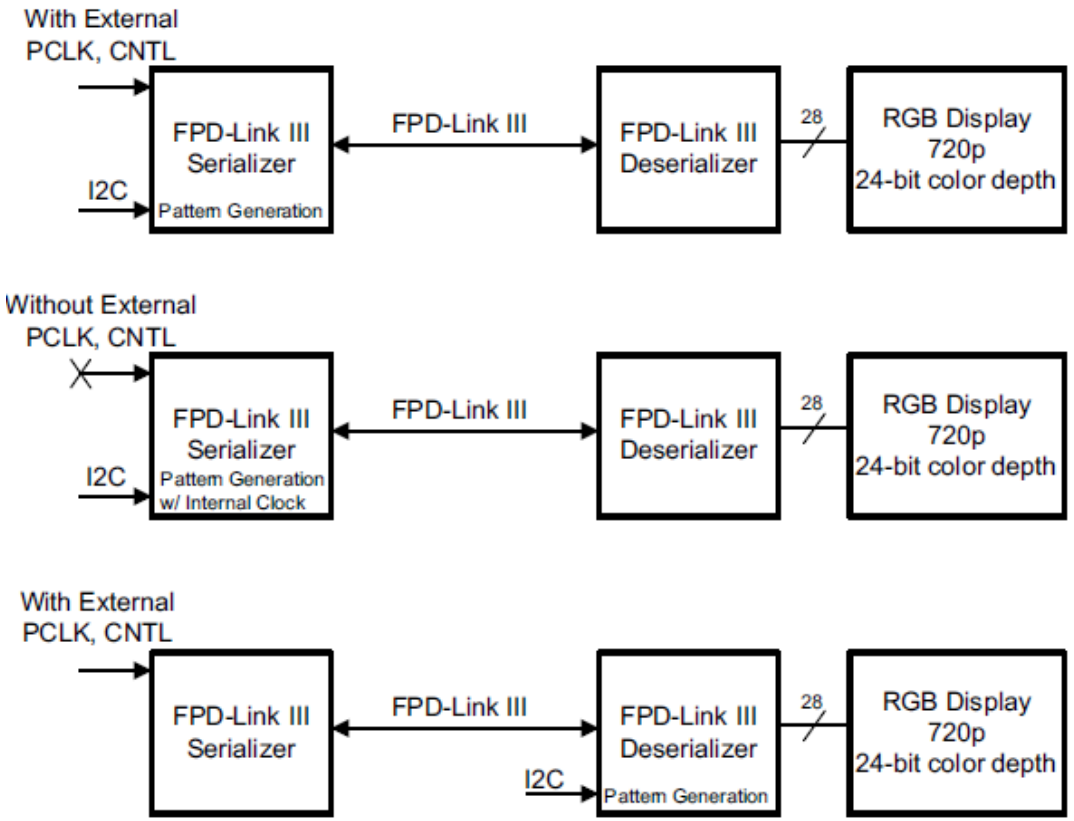


- For high noise environments an addtional voltage divider network may be connected to the center point .
- this provide has the advantage of a providing a DC low impedance path for noise suppression.
- Resistor 75ohm to 2kohm fo rthe pullup and pull down. Center point 1.2V, Vdd=3.3V, Rpulldown=750ohm, Rpullup=1.3kohm.
- The smaller values will consume more bias current, but will provide enhanced noise suppression.

BISTEN

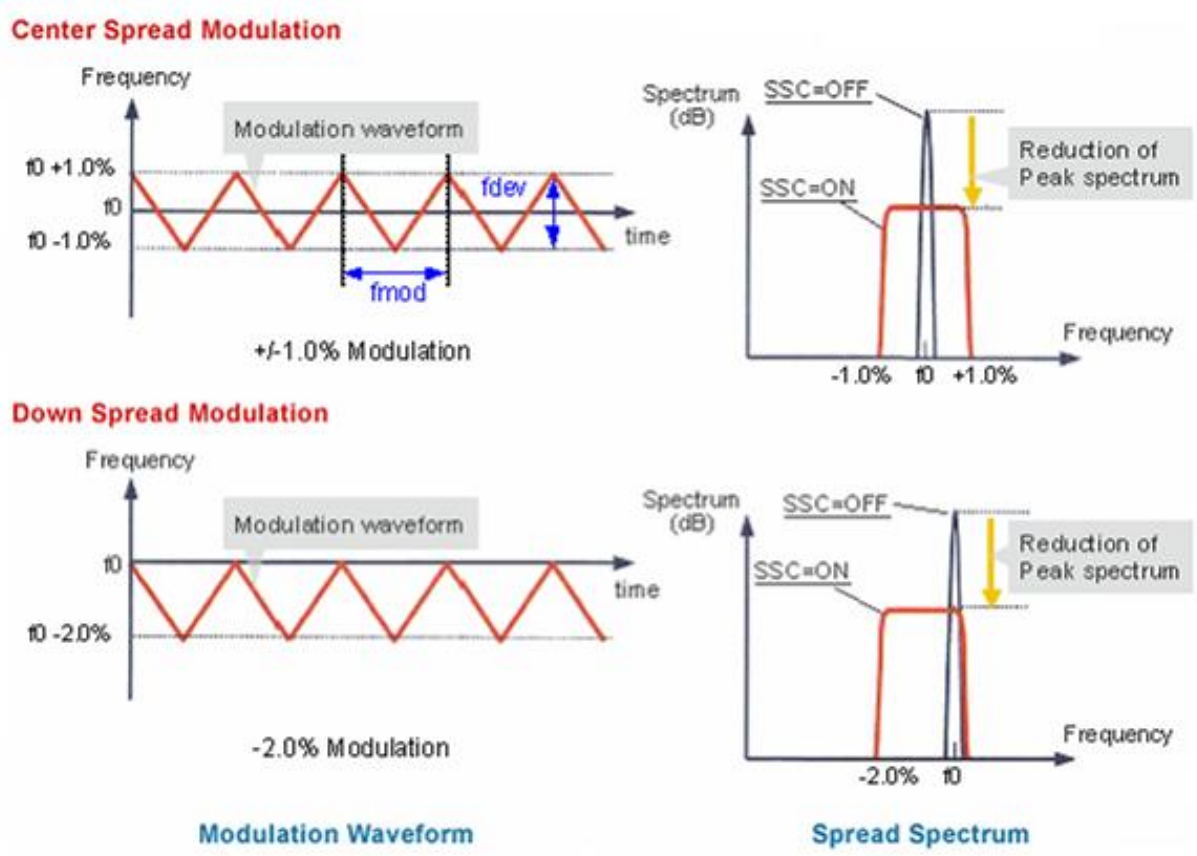
- Test interconnect between 925,926.
- 926: BISTEN=h.
- BISTC select external pclk or 33M internal oscillator clock frequency.
- Register 0x25 can select 33M or 25M or external
- LFMODE=1 select exteranl clk or 12.5Mhz.
- BISTEN=h, the BIST mode sent to the serializer through the back channel. The serializer output a test pattern and drives the link at speed.
- Monitor Pass pin and Lock pin.

Pattern Generation



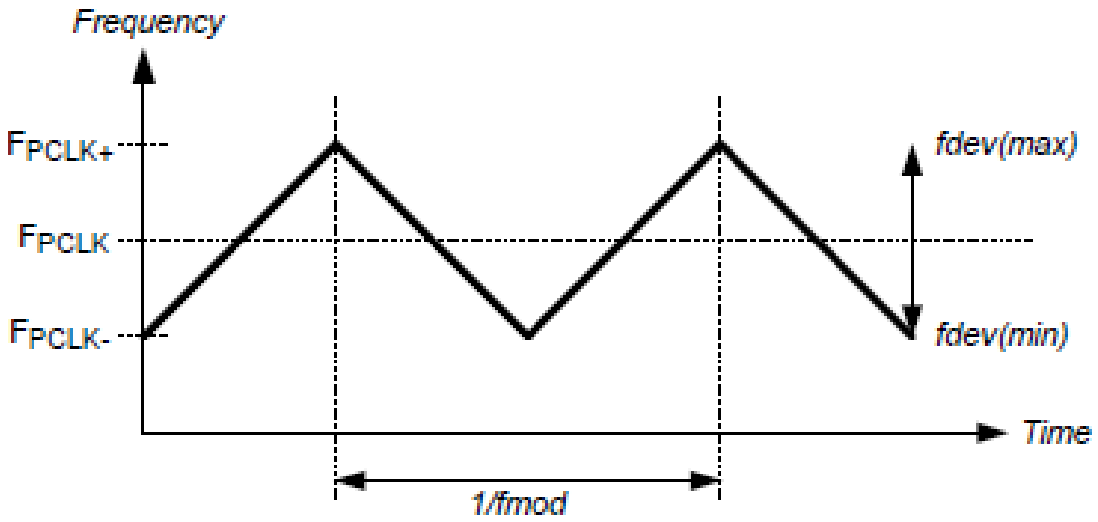
- Debug and test displays.
- Through the device control registers. 0x64,0x65
- AN-2198

Spread spectrum clocking(SSC)



- 925 capable of tracking a triangular input SSC profile up to +/-2.5% amplitude deviations(center spread), up to 35khz modulation at 5-85mhz form a host source

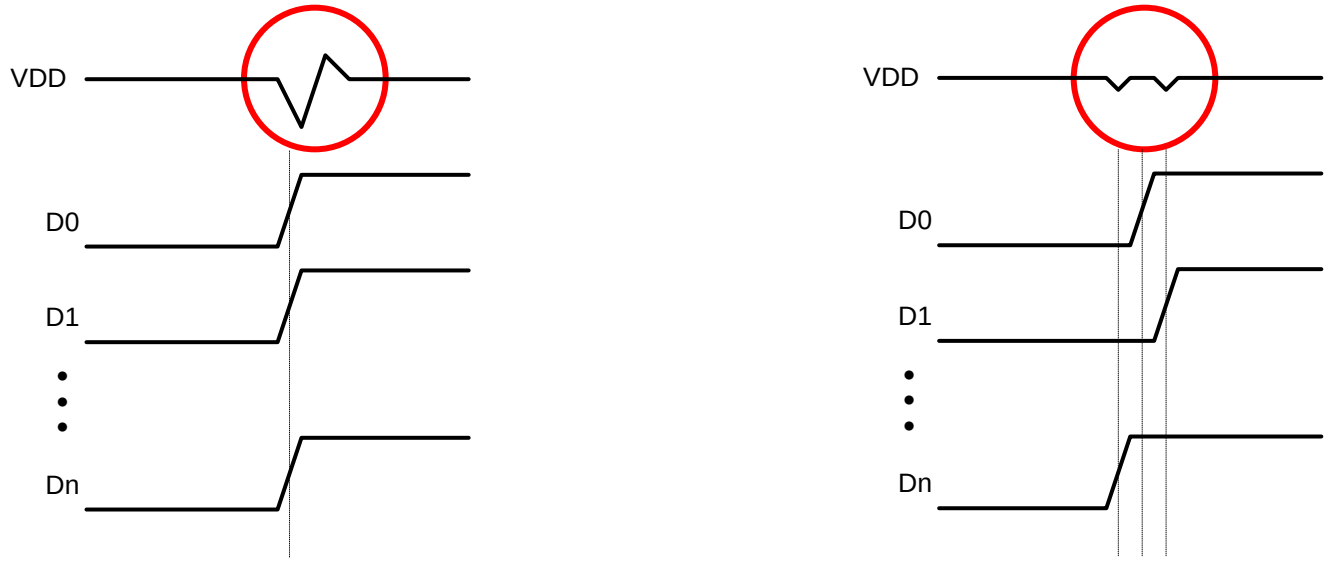
SSCG(spread spectrum clock generation)



SSCG Waveform

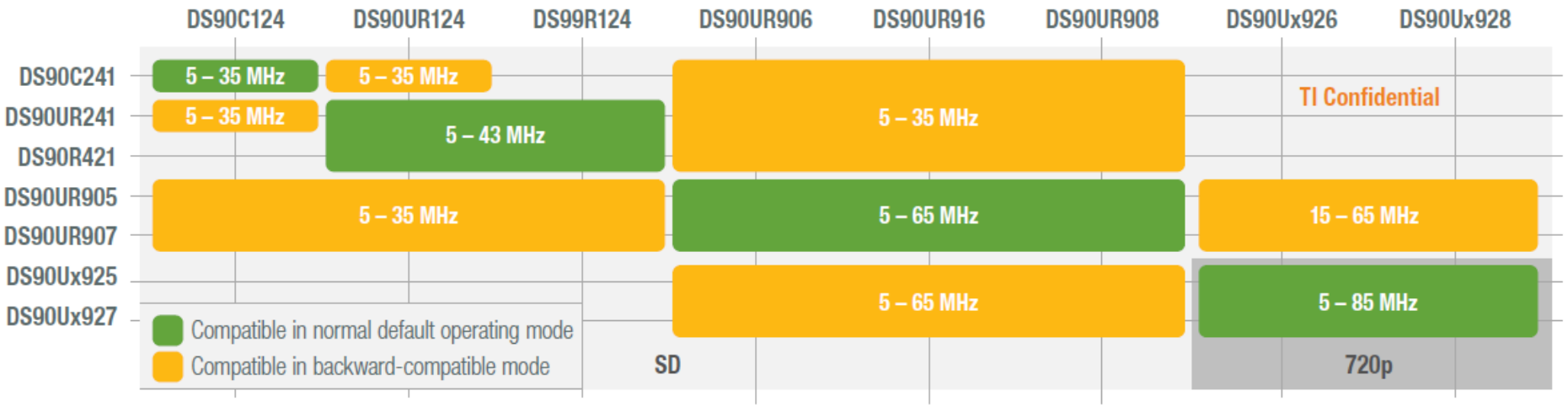
- 926 provides an internally generated SSCG to modulate its outputs(clock and data). Lower system EMI. Deviations to +-2.5% up to 100khz modulations .

EPTO(Enhanced Progressive Turn-ON)



- 926 LVCMOS parallel output timing are delayed groups of 8bits R,G,B outputs switch in a different time.
- Minimize the number of outputs switching simultaneously and helps to reduce supply noise. Spreads the noise spectrum out reducing overall EMI.

FPD-Link Interoperability



- 906 register 0x02

2	RW

Backward Compatible Mode Select	Backward Compatible Mode Select to DS90UR905Q and DS90UR907Q. If Reg_02[3] = 1 1: Backward Compatible is on 0: Backward Compatible is off

PCB layout

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
- – S = space between the pair
- – 2S = space between pairs
- – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair