FPD-Link III Troubleshooting Techniques

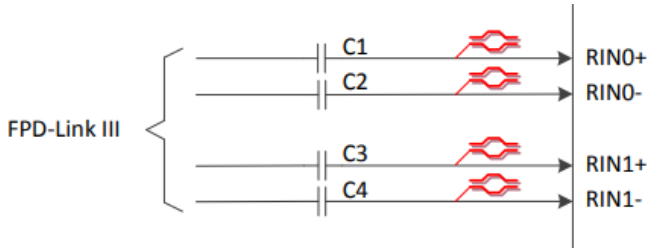
Ethernet & FPD-Link™ (EFL) Product Line

Step 1: Hardware verification

- Measure Voltage Levels / Sequencing
  - It is important to be supplying the correct voltage to the system. If the voltage levels are not properly regulated then the system is not receiving enough or is receiving too much current to properly function.
  - Measure the voltage rails at power-up and compare with recommended sequence in datasheet. The PDB pin should always come up after the supplies are stable.
- Verify cable connection between SER and DES
  - Is cable length and type supported?
  - It is important to verify that there is a true connection between the cable and each board to ensure proper communication. This can be done using the BIST function which can be run to identify some issues with link integrity margin.
  - This can also be verified using an oscilloscope to trace signal from SER, connector, cable, connector, DES

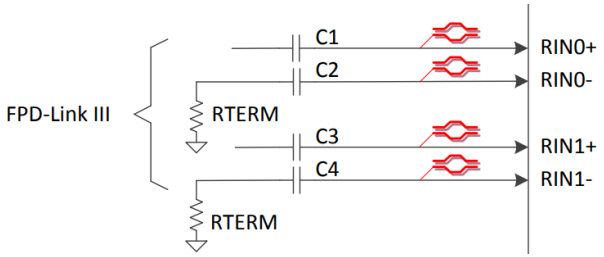
Step 1: Hardware verification

- Verify the RIN± and Rx ± ports configuration
  - Capacitor values
    - Capacitor values are different with different parts
    - STP and Coax setups are different
  - Termination resistors



C1-C4 = 0.1µF (50 WV; 0402) with DS90UH/B925/927
= 0.033µF (50 WV; 0402) with DS90UH/B929/947/949

STP setup



C1,C3 = 0.033µF (50 WV; 0402)
C2,C4 = 0.015µF (50 WV; 0402)

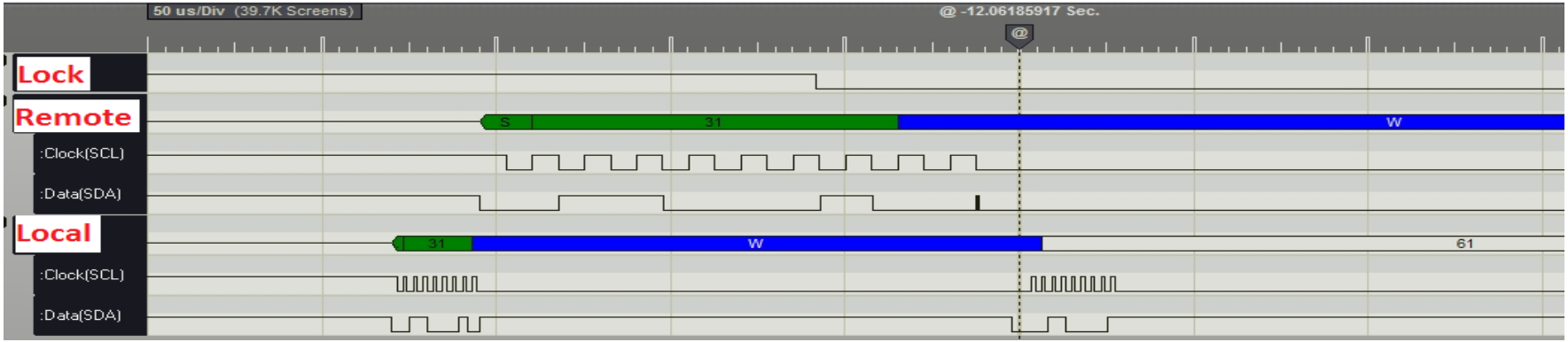
Coax setup

Step 2: Check I2C Communication - Local

- If one of the devices is unresponsive locally, check the other possible addresses to see if it strapped into the wrong address.
- Verify the pull-up resistors are present and are the correct values.
- Measure the power pins and PDB to ensure device is powered up.
- Measure the I2C bus and capture the failed transactions for further analysis.

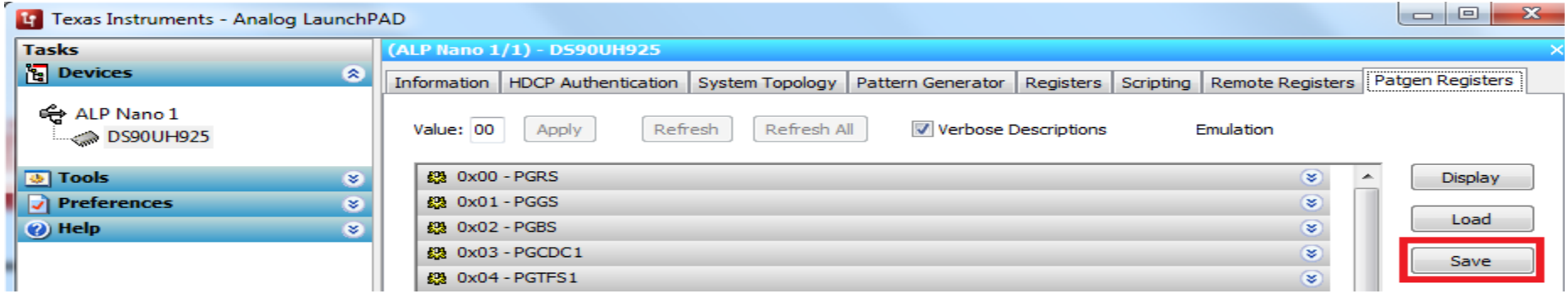
Step 2: I2C Communication - Remote

- If there are remote I2C communication issues, try to capture both remote and local buses along with the DES Lock status.
- Here is an example with a bus analyzer where remote transactions were failing due to Lock going low.

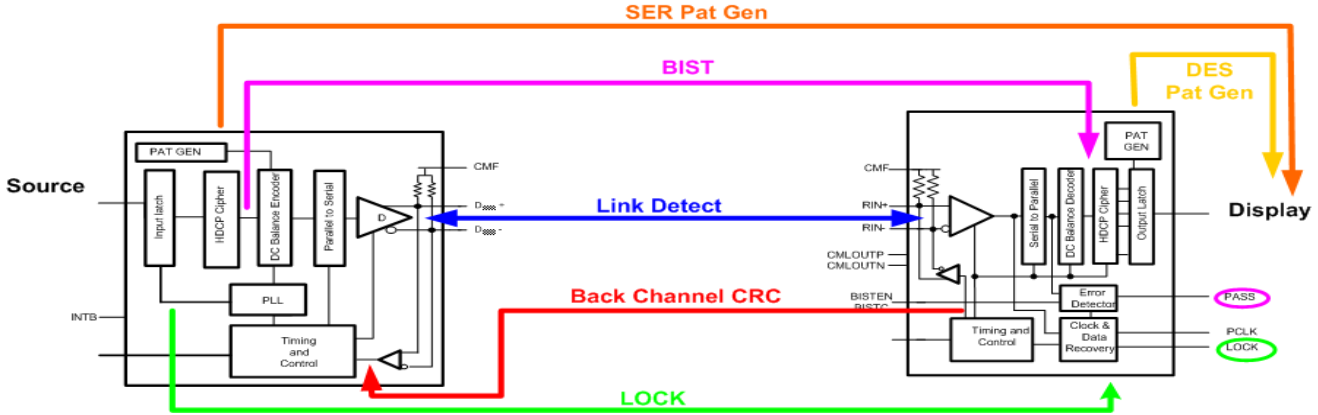


Step 3: Get the Register Dump

- It is very useful to get a register dump of both SER and DES when there is an issue happening.
- It may be necessary to connect to both sides individually to read back this information.
- Compare this to the datasheet register section.



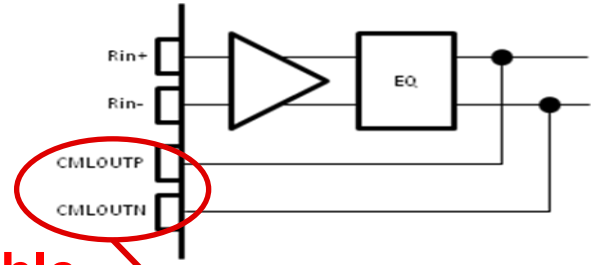
Step 4: Utilizing Link Diagnostics



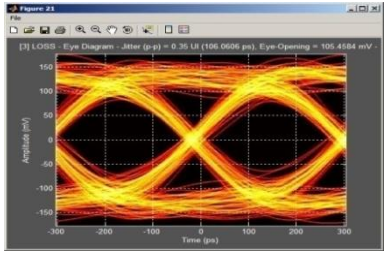
- **LOCK: Verifies link established between SER and DES – DES has "locked" to incoming serial data stream. Monitor LOCK pin.**
- **BIST (Built-in Self Test): Verifies data integrity of link between SER and DES. Monitor PASS pin.**
- **CRC: Integrity of backchannel link. Error reporting via register.**
- **PAT GEN: Visually validate data path without video source. Test pattern generated by SER or DES.**
- **LINK DETECT: Remote verification of link between SER and DES. Monitor register in SER.**

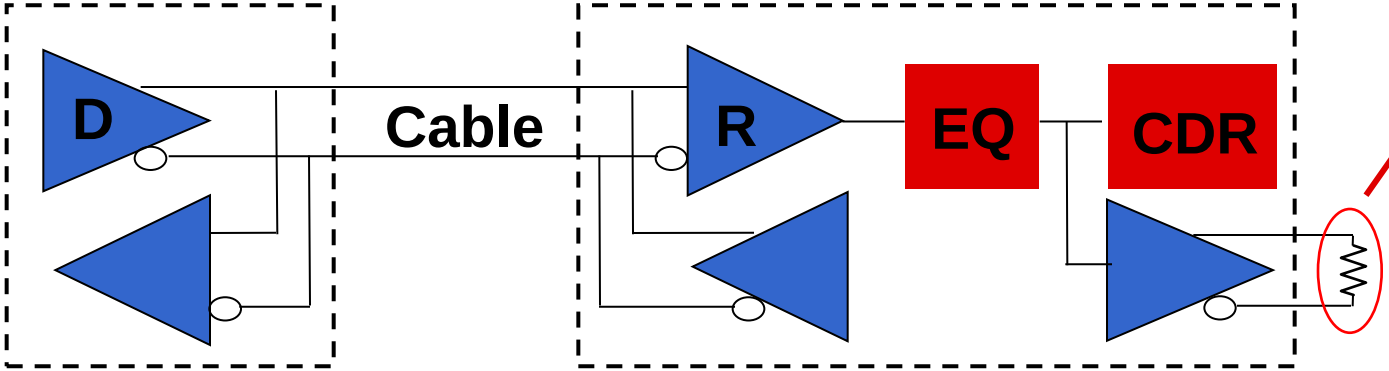
Tips to simplify trouble-shooting

- **Provide access/test points to link diagnostics**
  - **LOCK** – indicates Des PLL lock status to incoming serial stream
  - **PASS** – indicates status / results of BIST
  - **CMLOUT+/-** with 100 Ohm termination ➔ monitor eye opening of equalized signal
- **I2C Bus**
  - Provide access points on both Ser and Des board
  - Read status registers for diagnostics
  - Enable **CMLOUT+/-** for eye monitoring



Enable via I2C



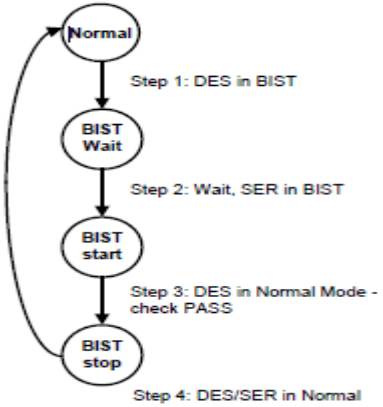


BIST Overview

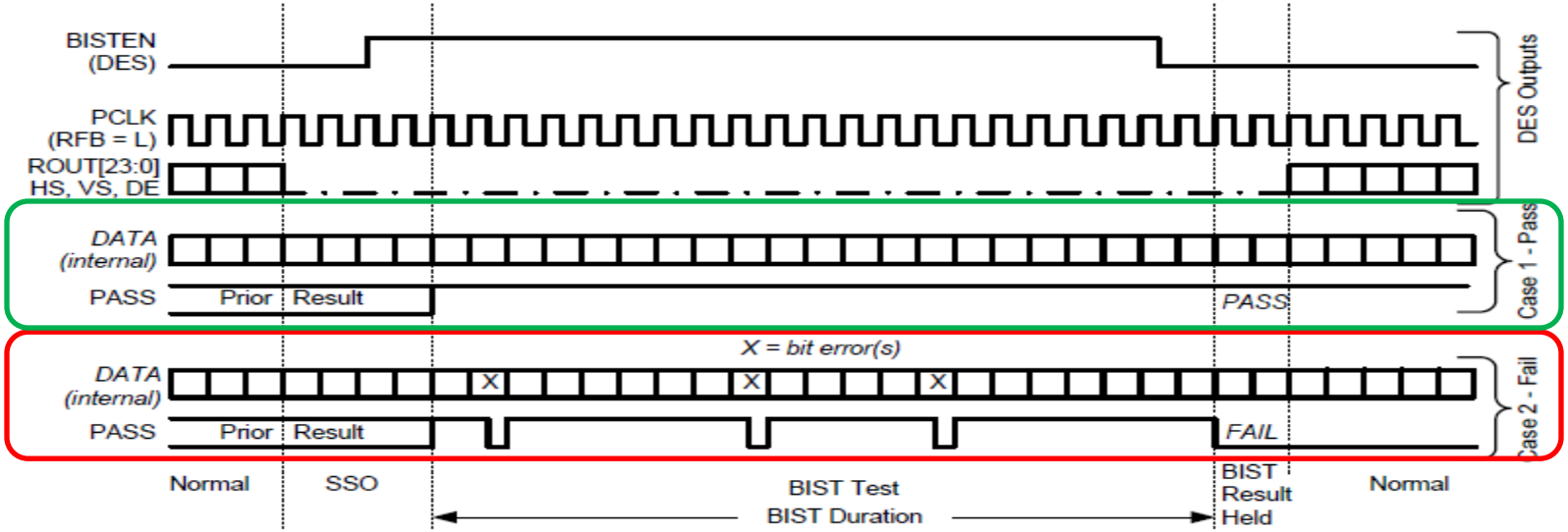
- Speed Built In Self Test (BIST) feature supports the testing of the FPD-Link interface including high speed serial link (FC) and the low-speed back channel (BCC)
- BIST mode is pin- or register-selectable and includes the following features:
  - PASS pin status
  - BIST generator (w/ PRBS7 pattern)
  - BIST error counter register (FC)
  - CRC counter register (BCC)
    - Back channel errors – checks integrity of the back channel simultaneously with the forward channel

BIST Operation

- **Step 1:** Enable BIST on deserializer. Select the proper clock source.
- **Step 2:** Deserializer sets serializer into BIST mode. Deserializer acquires LOCK and PASS pin goes to High. BIST starts check the datastream. If error is detected in payload, the PASS will switch Low and increment BIST error counter.
- **Step 3:** Stop BIST mode on deserializer. Deserializer stops checking data. Final test results is held on PASS pin status.
- **Step 4:** Return to normal operating mode.

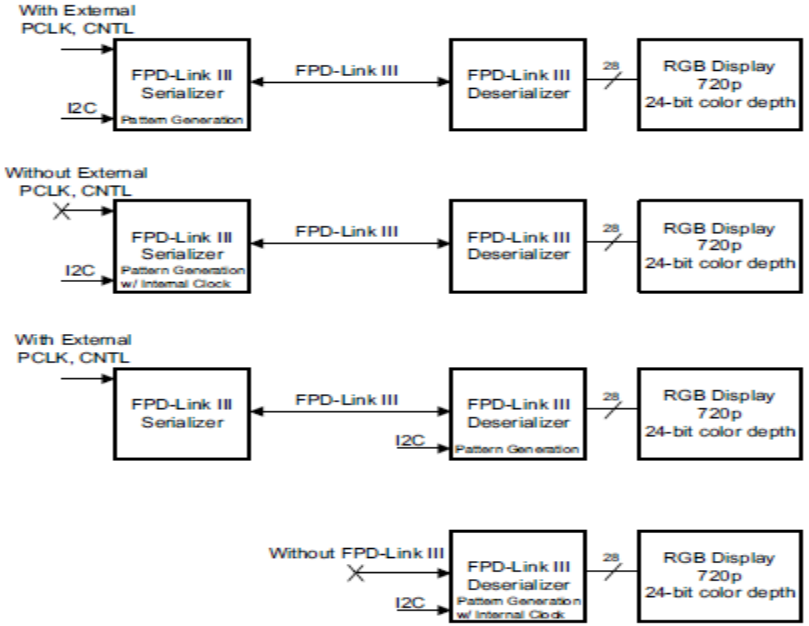


Example BIST Waveforms (DS90UB925/926)



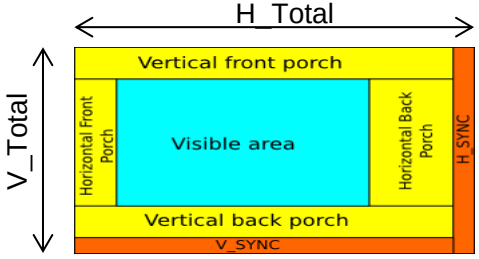
Internal Pattern Generator Overview

- Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices – *www.ti.com/lit/an/snla132c/snla132c.pdf*



Internal Timing Parameters

- Pixel Clock Divider
- Total Horizontal Width
- Total Vertical Width
- Active Horizontal Width
- Active Vertical Width
- Horizontal Sync Width
- Vertical Sync Width
- Horizontal Back Porch
- Vertical Back Porch
- Horizontal Sync Polarity
- Vertical Sync Polarity



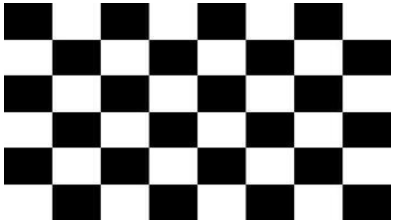
Programmable Pattern Selection

Full screen primary color patterns

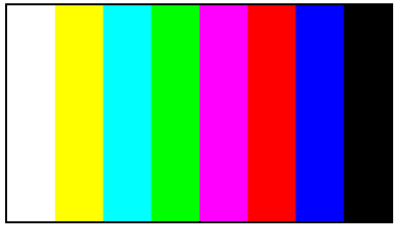
Horizontal gray shade patterns

Vertical gray shade patterns

Full screen programmable color

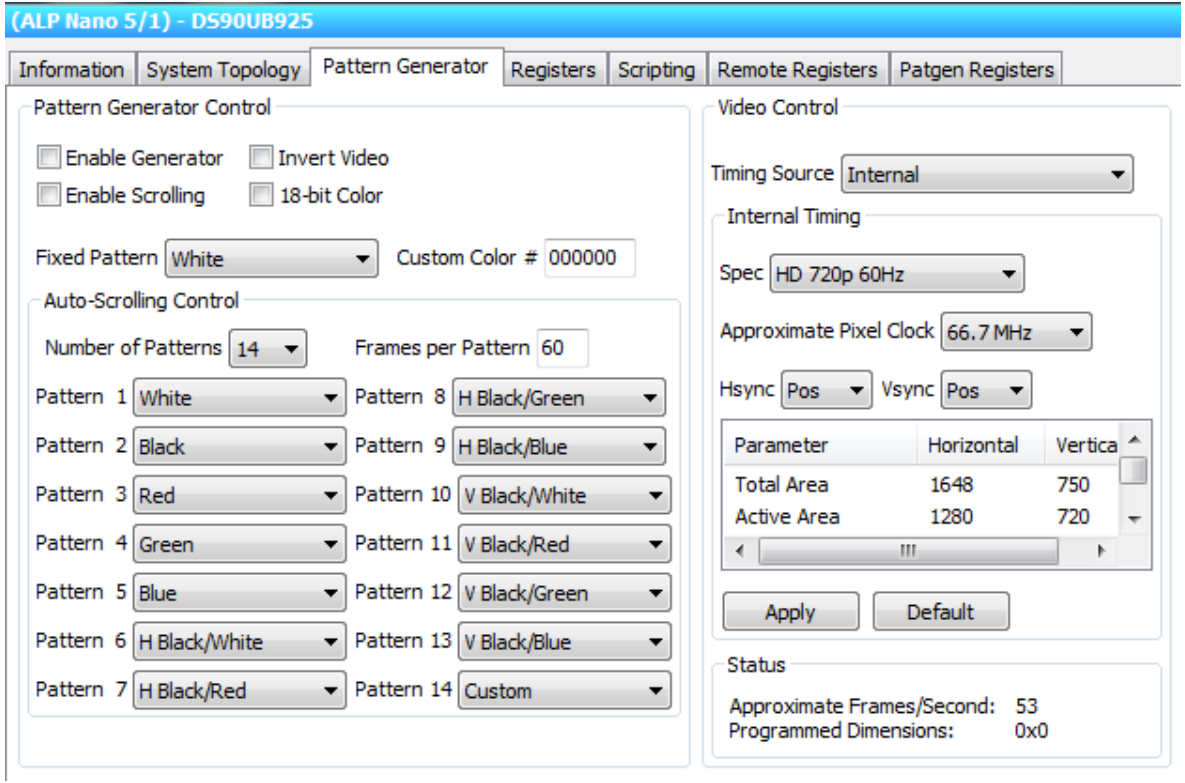


Checkerboard pattern



Vertical color bars pattern

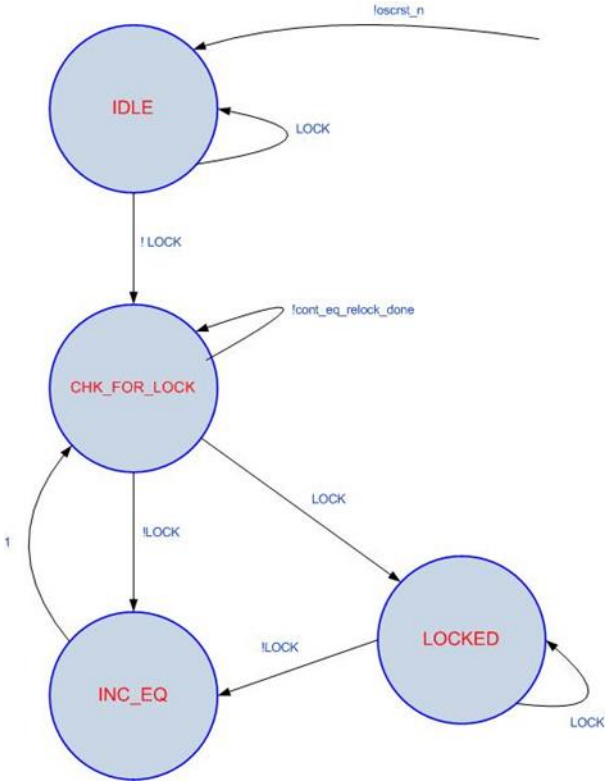
ALP GUI for Pattern Generator (DS90UB925)



AEQ details

- AEQ Restart
- Programmable relock time
- AEQ Floor/ Max
- AEQ Error Threshold (954)

ADAPTIVE_EQ_RELOCK_TIME	RW	0x4	Time to wait for lock before incrementing the EQ to next setting 000 : 164 us 001 : 328 us 010 : 655 us 011 : 1.31 ms 100 : 2.62 ms 101 : 5.24 ms 110 : 10.5ms 111 : 21.0 ms Values will scale with reference clock frequency.
AEQ_1ST_LOCK_MODE	RW	1	AEQ First Lock Mode This register bit controls the Adaptive Equalizer algorithm operation at initial Receiver Lock. 0 : Initial AEQ lock may occur at any value 1 : Initial Receiver lock will restart AEQ at 0, providing a more deterministic initial AEQ value
AEQ_RESTART	RW/SC	0	Set high to restart AEQ adaptation from initial value. This bit is self clearing. Adaption will be restarted.
SET_AEQ_FLOOR	RW	1	AEQ adaptation starts from a pre-set floor value rather than from zero - good in long cable situations
EQ_STATUS	R	0x00	Adaptive EQ Status - setting direct to analog
AEQ_MAX	RW	0xF	Adaptive Equalizer Maximum value This register sets the maximum value for the Adaptive EQ algorithm.
ADAPTIVE EQ FLOOR VALUE	RW	0x2	When AEQ floor is enabled by the SET_AEQ_FLOOR register bit (0xD2[2]), the starting setting is given by this register.

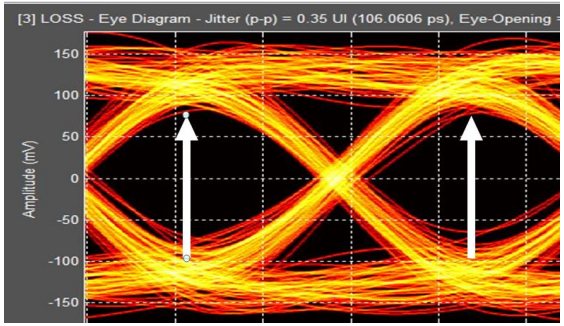


Typical 94x AEQ settings range for a cable loss range

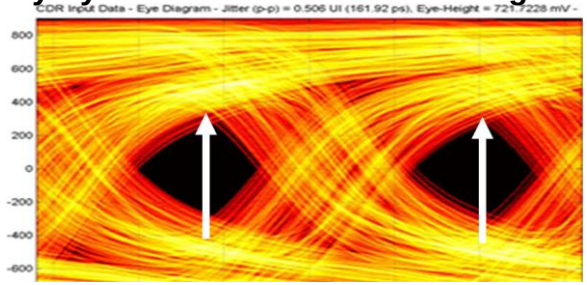
Loss (Range)	Acceptable Equalizer range
0 – 3dB	0 - 1
3 – 4dB	1 - 2
4 – 6dB	2 - 3
6 – 9.5dB	3 - 4
9.5 – 10.5dB	4 - 5
10.5dB – 13.5dB	5 - 9
13.5dB – 16dB	10 - 15
>16dB	15

Strobe Positioning – s filter

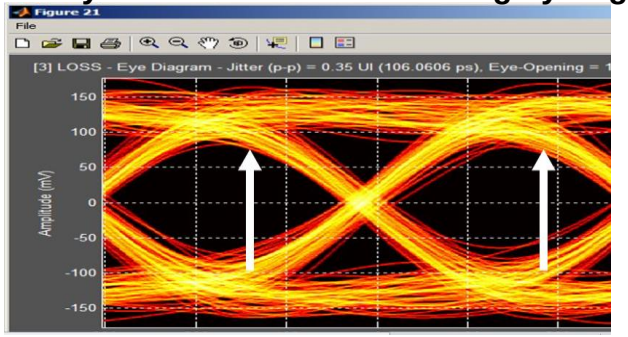
Clean Eye Normal Strobe Positioning



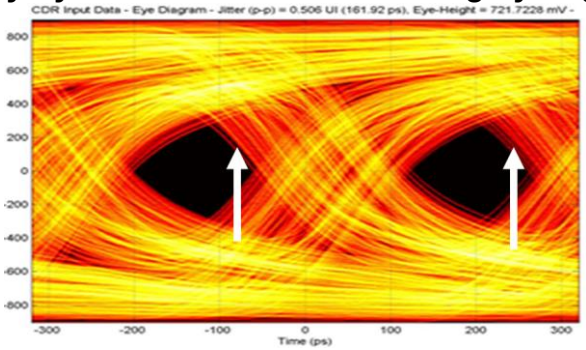
Noisy Eye Normal Strobe Positioning



Clean Eye Offset Strobe Positioning by Register



Noisy Eye Offset Strobe Positioning by Register



Typical Customer Issue for IVI application

Troubleshooting FPD for Display Applications

Commonly encountered: No Image, and Image Flicker/Distortion

No Image

- LOCK status – expect HIGH
- No LOCK (static LOW) ➔
  - Clock/data/sync present at SER input?
  - Cable connected & correct polarity?
  - Differential signal present at DES inputs?

Image Flicker / Distortion

- LOCK status – expect HIGH
- LOCK toggling ➔
  - Quality of input PCLK? (jitter, etc.)
  - Power supply noise?
  - LVCMOS inputs – overshoot, undershoot?
  - Quality of serial data eye diagram?
- LOCK high ➔
  - Sync signals on RGB/LVCMOS?
  - Rising/Falling edge selection on LVCMOS?

Check Lock Status of FPD-Link

- The LOCK output reporting pin serves the purpose of validating the link integrity of the connection between the SER and DES.
- When the LOCK status is high, the PLL in the DES is locked and validates the data and clock recovered from the serial input and is available on the parallel bus and PCLK outputs.
- If the LOCK status is low, then the PLL is not locked, meaning that the serial data isn't being fully recovered and the data at the output does not represent the data transferred from the SER. For example, while using the EVM, this status can be easily checked by monitoring the LOCK pin or LED labeled "LOCK" on the DES EVM

Lock Unstable

- There are many possible reasons for lock to be unstable.
- Use FPD-Link III Conformance document to measure at the different link test points: CMLOUT on DES, SER output, and PCLK input.
- This narrows down where to investigate.
  - If CMLOUT doesn’t meet typical spec, but SER output does, look at board layout and cable/connector characteristics.
  - If SER output doesn’t meet spec but PCLK input does, look at SER power noise and board layout.
  - If PCLK input does not meet spec, try adjusting PLL divider ratios on processor source, or adding jitter cleaner.

Image Flickering with Stable Lock

- This usually means that there is a problem with the Sync signals, HS / VS / DE.
- Measure these signals to see if they are consistent from frame to frame.
- This is easy with RGB output, but if using OLDI output then an adapter could be used, possibly using an EVM.

Full Link Debug/Troubleshooting (DS90Ux92xQ)

- **#1: Deserializer to Display**
  - Utilize Internal Pattern Generator feature (Refer to AN-2198)
  - Use internal clock/timing mode
  - Select pattern and enable Pattern Generator
  - If no picture seen, check clock and resolution information
  - If errors seen on the pattern, check RGB/HS/VS/DE connections to display
    - Continuity
    - Setup & Hold time
  - If no issues, proceed to next step
- **#2: Deserializer Receive**
  - Check that LOCK = H (static)
    - If LOCK = L, check cable connection
    - If LOCK ≠ H, debug layout and signal integrity
  - Check Link Detect (device control registers)
    - If Link Detect = 0, check for cable continuity and correct pin-out
  - If LOCK = H (static) Run BIST
    - May identify some issues with link integrity margin
    - Activate from Deserializer (some chipsets also require serializer configuration – See datasheet)
    - PASS pulses (1 PCLK) low if there is an error during BIST. PASS remains LOW after BIST is disabled

Full Link Debug/Troubleshooting (continued)

- **#3: Check Eye Diagram (CML Loop-through driver)***
  - Turn on Deserializer CML loop-through driver from control register (see device datasheet)
  - Capture eye diagram with >4GHz BW oscilloscope
  - If eye closed, try adjusting equalizer
  - Refer to device datasheet for eye diagram guidelines

- **#4: Serializer Pattern Generator**
  - Configure Serializer pattern generator (Refer to AN-2198)
  - Use internal clocking/timing mode and observe pattern
    - If issues observed, confirm issue with link signal integrity
    - If no issues, observed, change pattern generator to use source clock and timing
  - Use external clocking/timing mode and observe pattern
    - If issue observed, check source RGB/HS/VS/DE connections and Setup/Hold time
    - Check source clock jitter characteristics (refer to input jitter tolerance specifications in device datasheet)
    - Jitter issue means customer may have to utilize a jitter cleaner

* Some customers do not have necessary equipment. Skip this step if unavailable

Troubleshooting of Basic I2C Issues

- No communication with device? Likely incorrect ID, Aliasing
  - Make sure the deserializer has loaded correct serializer ID
  - Confirm address set properly – ID[x] for SER and DES
  - I2C configuration registers set properly
- Errors in communication?
  - Monitor CRC backchannel error register
  - Make sure edge rates are appropriate for the datarate
  - Poor signal integrity
    - Glitches or spikes on I2C SCL clock input signals
    - Glitches or spikes on I2C SDA buses
  - Setup and hold time violations
  - Excessive over-/under-shoot

TEXAS INSTRUMENTS

HS, VS, DE