PCI Express Architecture

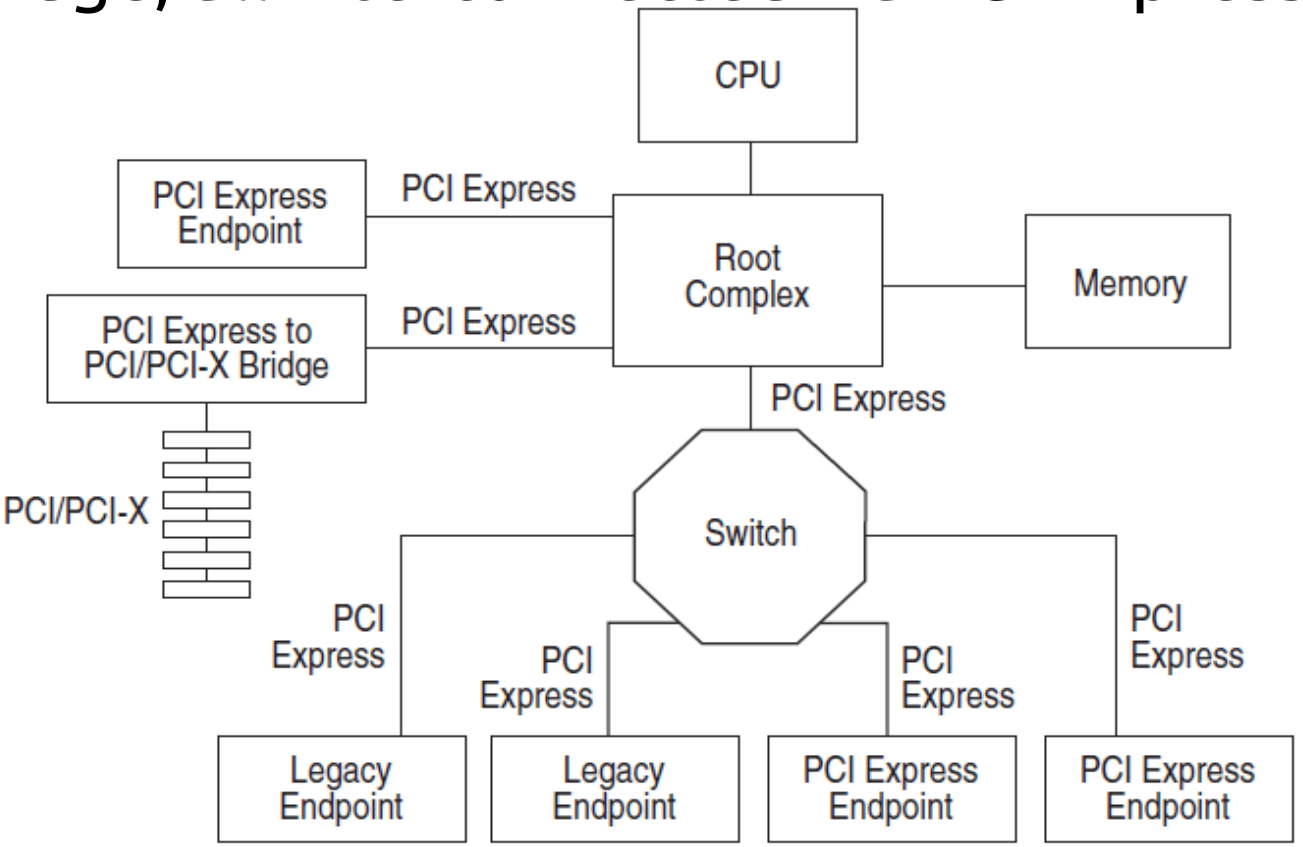
In a Nutshell

Root Complex (RC)

- Root Complex (RC) – The interface between the CPU and the PCIe buses may contain several components (processor interface, DRAM interface, etc.) and possibly even several chips.
- May support one or more PCI Express Ports – Root Ports.
- **Logically** aggregates PCIe hierarchy domains into one single PCIe hierachy.

Root Complex

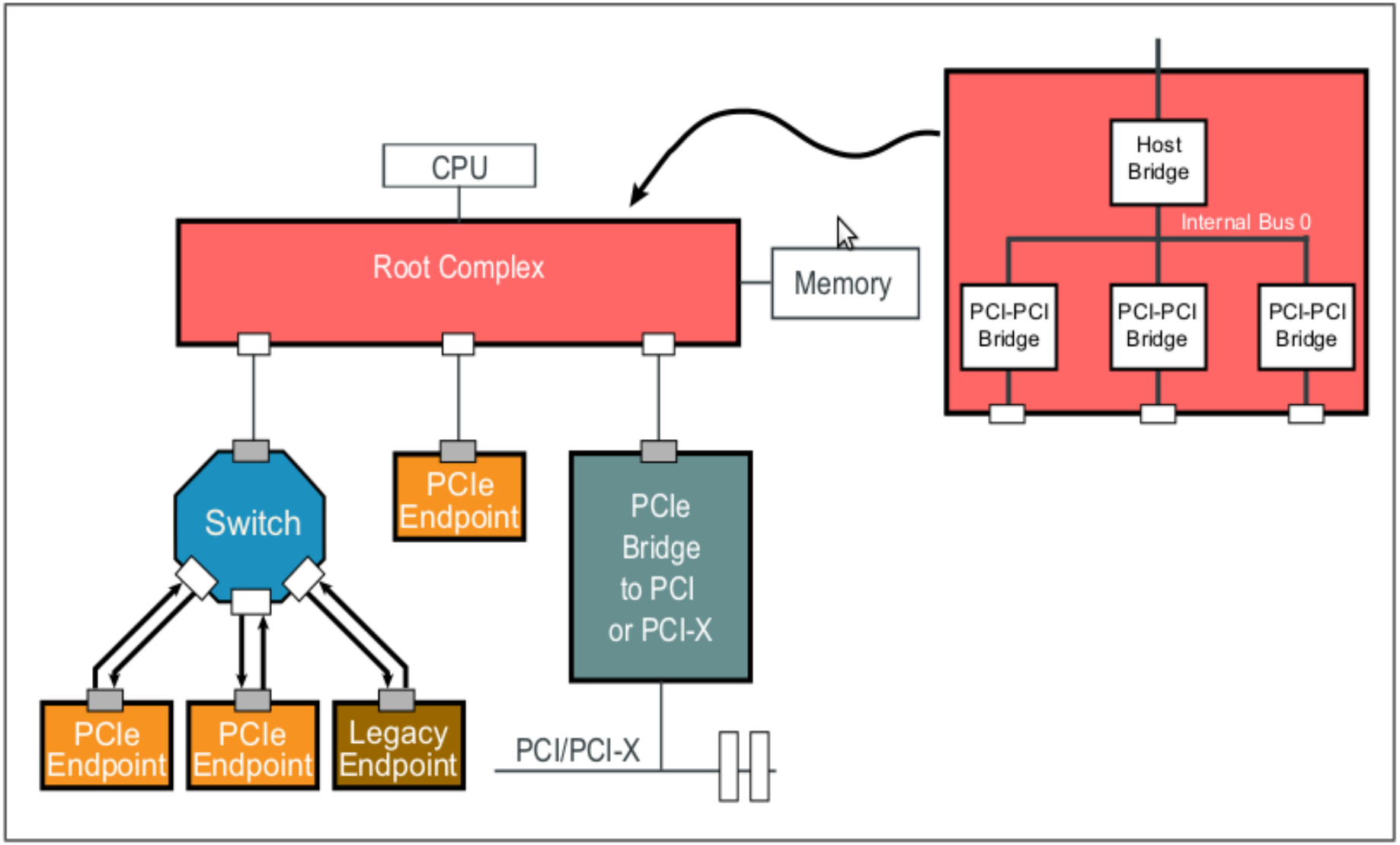
- Single fabric instance referred to as a hierarchy – composed of a RC , multiple Endpoints (I/O devices), a Switch, and a PCI Express to PCI/PCI-X Bridge, all interconnected via PCI Express Links



PCIe Root Port

- Each Root Port defines a separate hierarchy domain.
- Each hierarchy domain may be composed of a single Endpoint or a sub-hierarchy containing one or more Switch components and Endpoints
- The capability to route peer-to-peer transactions between hierarchy domains through a Root Complex is **optional** and implementation dependent.

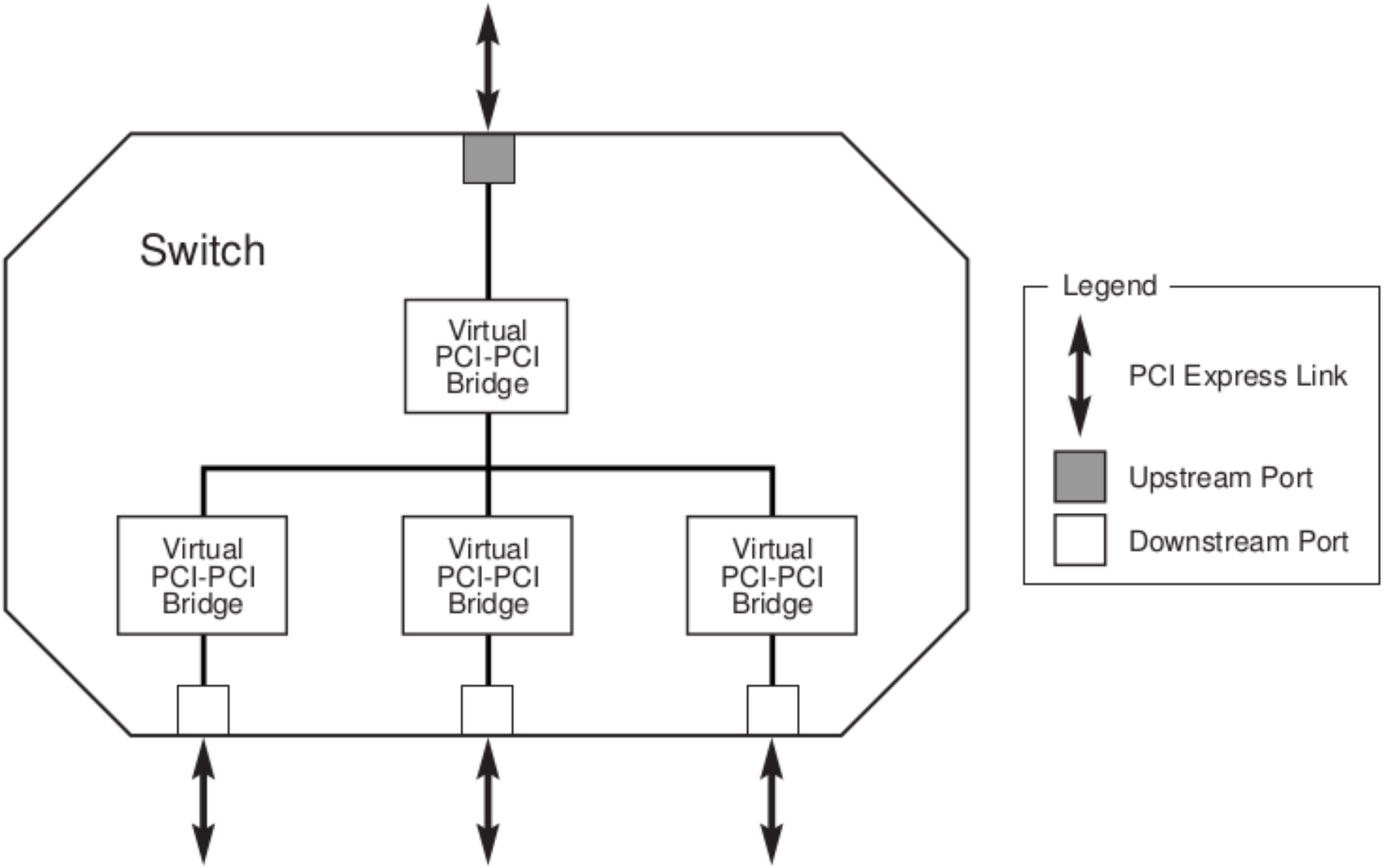
PCIe Root Port



Switches and Bridges

- Switches provide an aggregation capability and allow more devices to be attached to a single Root Port. They act as packet routers and recognize which path a given packet will need to take based on its address or other routing information.
- Bridges provide an interface to other buses, such as PCI or PCI-X, or even another PCIe bus.
- Switch may have several Downstream Ports but can only have one Upstream Port.

Virtual PCI-PCI Bridge

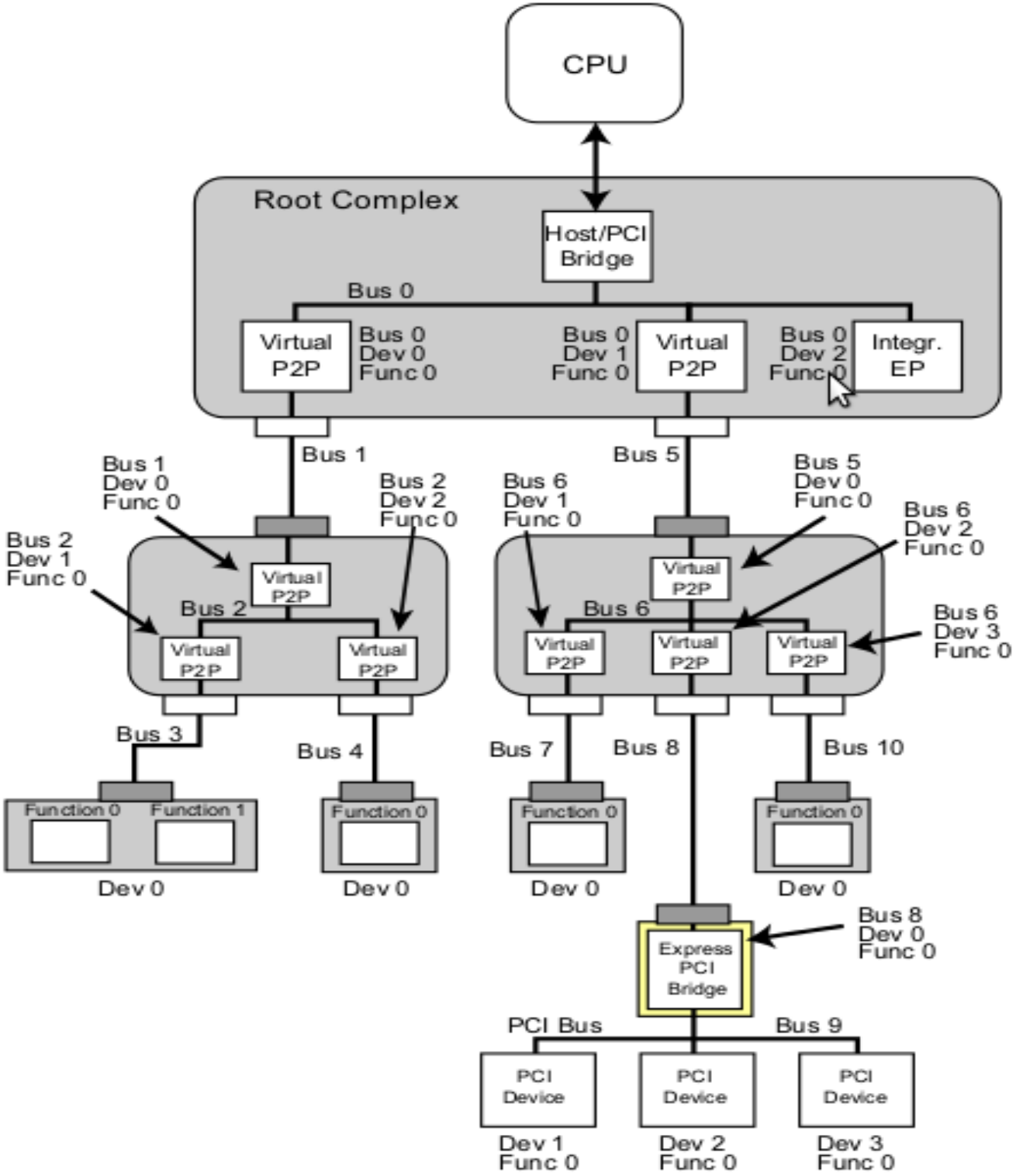


PCIe Endpoint Devices

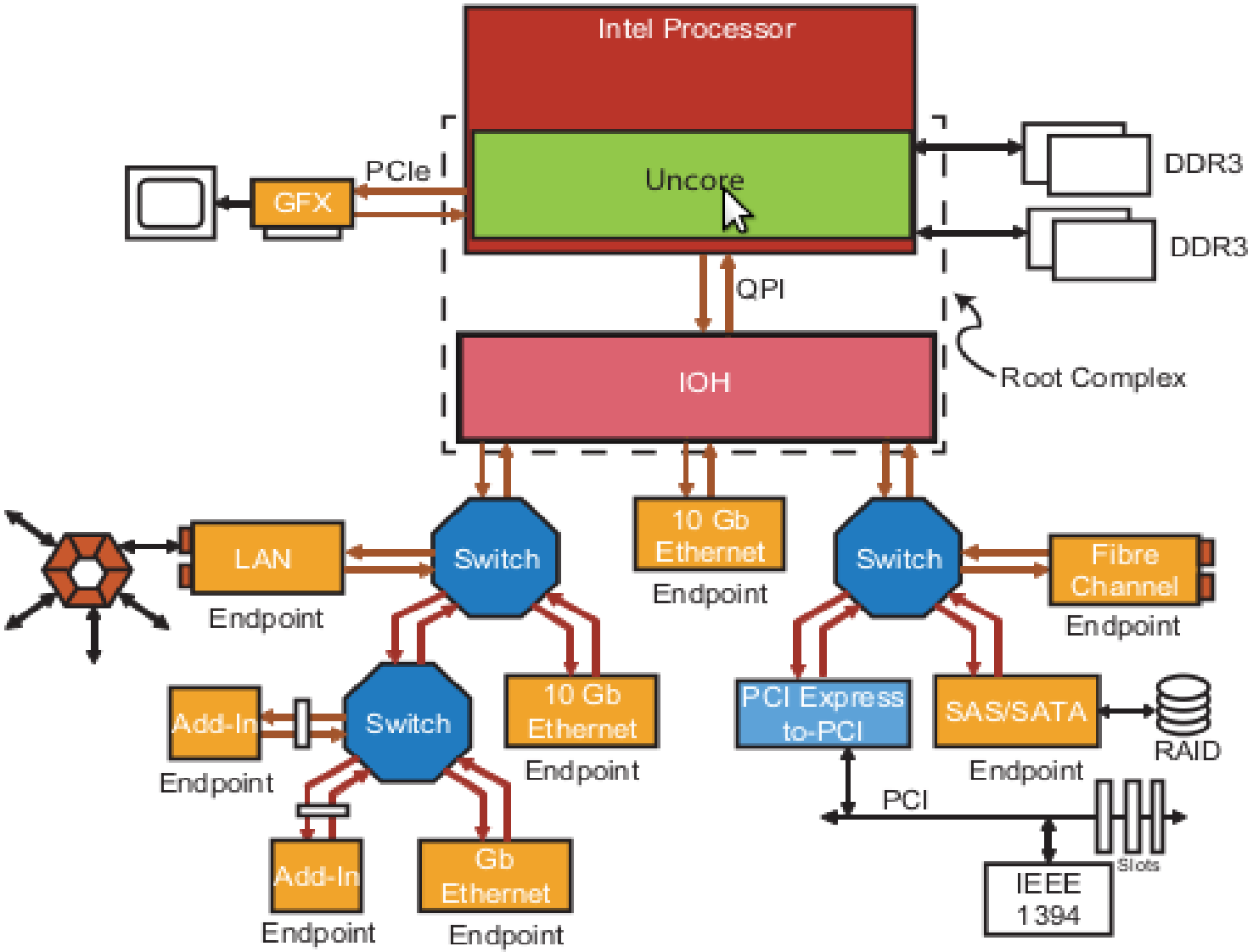
- Not Switches or bridges and act as initiators and Completers of transactions on the bus.
- They reside at the bottom of the branches of the tree topology and only implement a single Upstream Port (facing toward the Root).

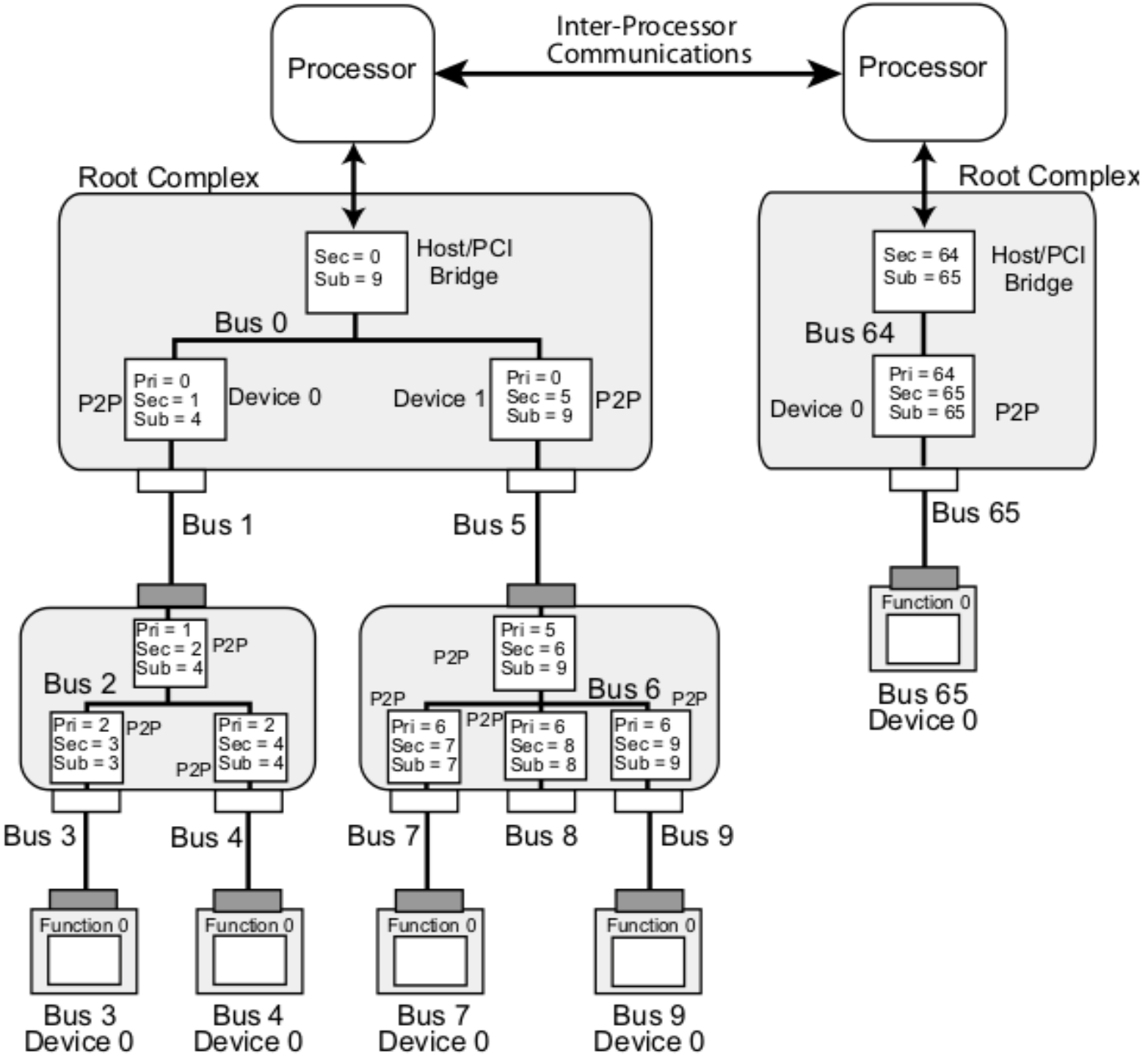
Enumeration

- The process by which configuration software discovers the system topology and assigns bus numbers and system resources.
- On x86 PCIe hierarchy enumeration done by BIOS on hardware initialization state – all registers configured before bootloader.
- System software can re-assign enumeration according to enumeration rules.


CPU
Root Complex
Host/PCI Bridge
Bus 0
Virtual P2P
Bus 0 Dev 0 Func 0
Bus 0 Dev 1 Func 0
Virtual P2P
Bus 0 Dev 2 Func 0
Integr. EP
Bus 1
Bus 5
Bus 1 Dev 0 Func 0
Bus 2 Dev 2 Func 0
Bus 2 Dev 1 Func 0
Virtual P2P
Bus 2
Virtual P2P
Virtual P2P
Bus 6 Dev 1 Func 0
Bus 5 Dev 0 Func 0
Bus 6 Dev 2 Func 0
Virtual P2P
Bus 6
Bus 6 Dev 3 Func 0
Virtual P2P
Virtual P2P
Virtual P2P
Bus 3
Bus 4
Bus 7
Bus 8
Bus 10
Function 0
Function 1
Function 0
Function 0
Function 0
Dev 0
Dev 0
Dev 0
Dev 0
Bus 8 Dev 0 Func 0
Express PCI Bridge
PCI Bus
Bus 9
PCI Device
PCI Device
PCI Device
Dev 1 Func 0
Dev 2 Func 0
Dev 3 Func 0

System Example




Processor
Inter-Processor
Communications
Processor
Root Complex
Root Complex
Sec = 0
Sub = 9
Host/PCI
Bridge
Bus 0
P2P
Pri = 0
Sec = 1
Sub = 4
Device 0
Device 1
Pri = 0
Sec = 5
Sub = 9
P2P
Sec = 64
Sub = 65
Host/PCI
Bridge
Bus 64
Device 0
Pri = 64
Sec = 65
Sub = 65
P2P
Bus 1
Bus 5
Bus 65
Function 0
Bus 65
Device 0
Pri = 1
Sec = 2
Sub = 4
P2P
Bus 2
Pri = 2
Sec = 3
Sub = 3
P2P
Pri = 2
Sec = 4
Sub = 4
P2P
P2P
Pri = 5
Sec = 6
Sub = 9
Bus 6
P2P
P2P
Pri = 6
Sec = 7
Sub = 7
P2P
Pri = 6
Sec = 8
Sub = 8
Pri = 6
Sec = 9
Sub = 9
Bus 3
Bus 4
Bus 7
Bus 8
Bus 9
Function 0
Function 0
Function 0
Function 0
Bus 3
Device 0
Bus 4
Device 0
Bus 7
Device 0
Bus 9
Device 0

Ivy Bridge systems example