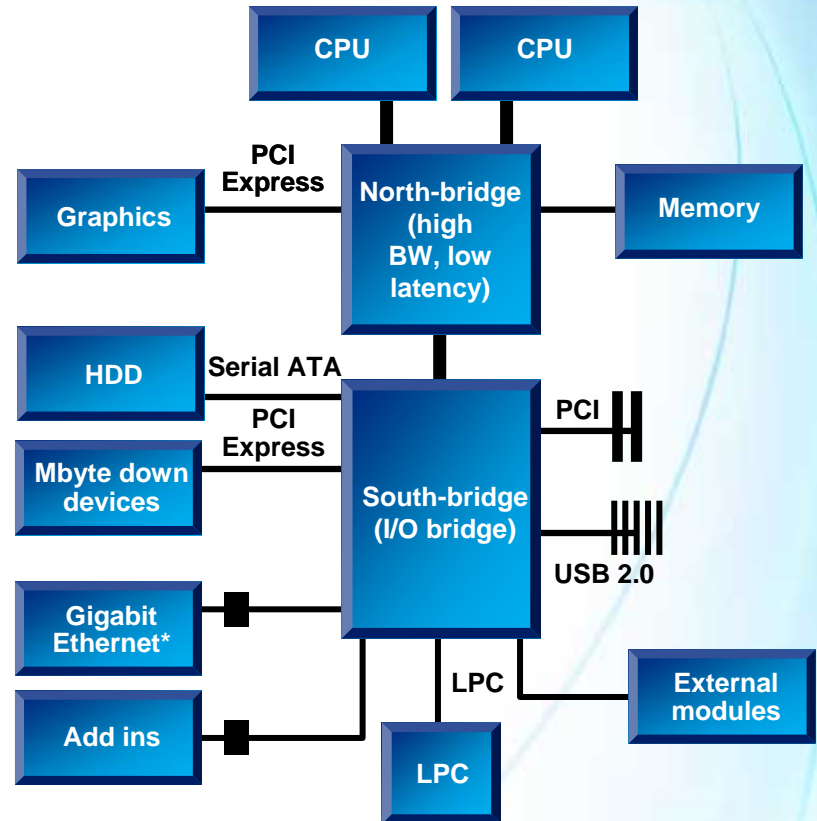# Introduction to PCI Express

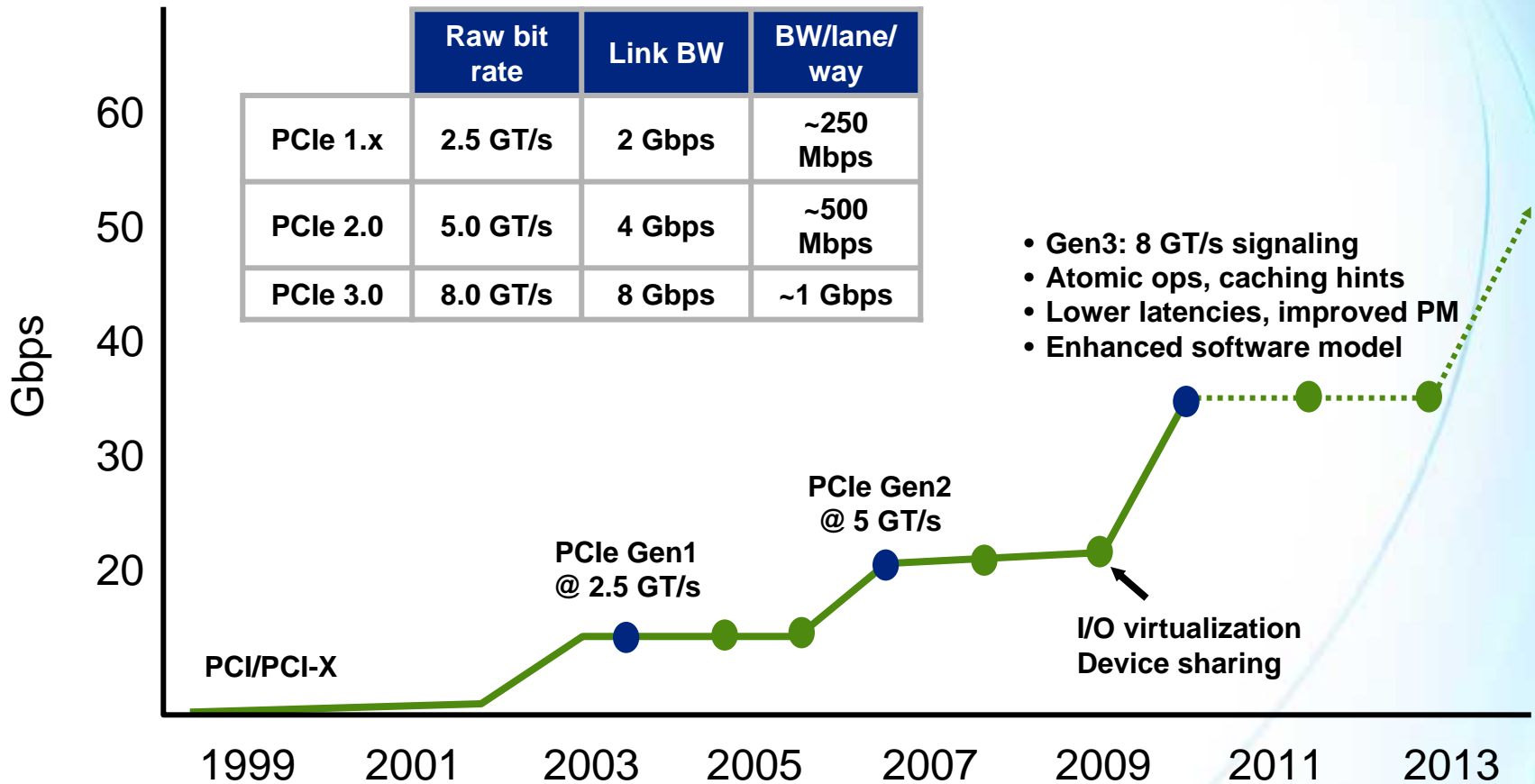*Transceiver Portfolio Workshops 2009*

PCI Express Overview

- PCI Express (Peripheral Component Interconnect Express) is a computer expansion standard introduced by Intel in 2004
  - Officially abbreviated as PCIe (PCI-E is also commonly used)

- PCIe replaces PCI, PCI-X, and AGP

- PCIe complements SERDES-based bus interface to the CPU
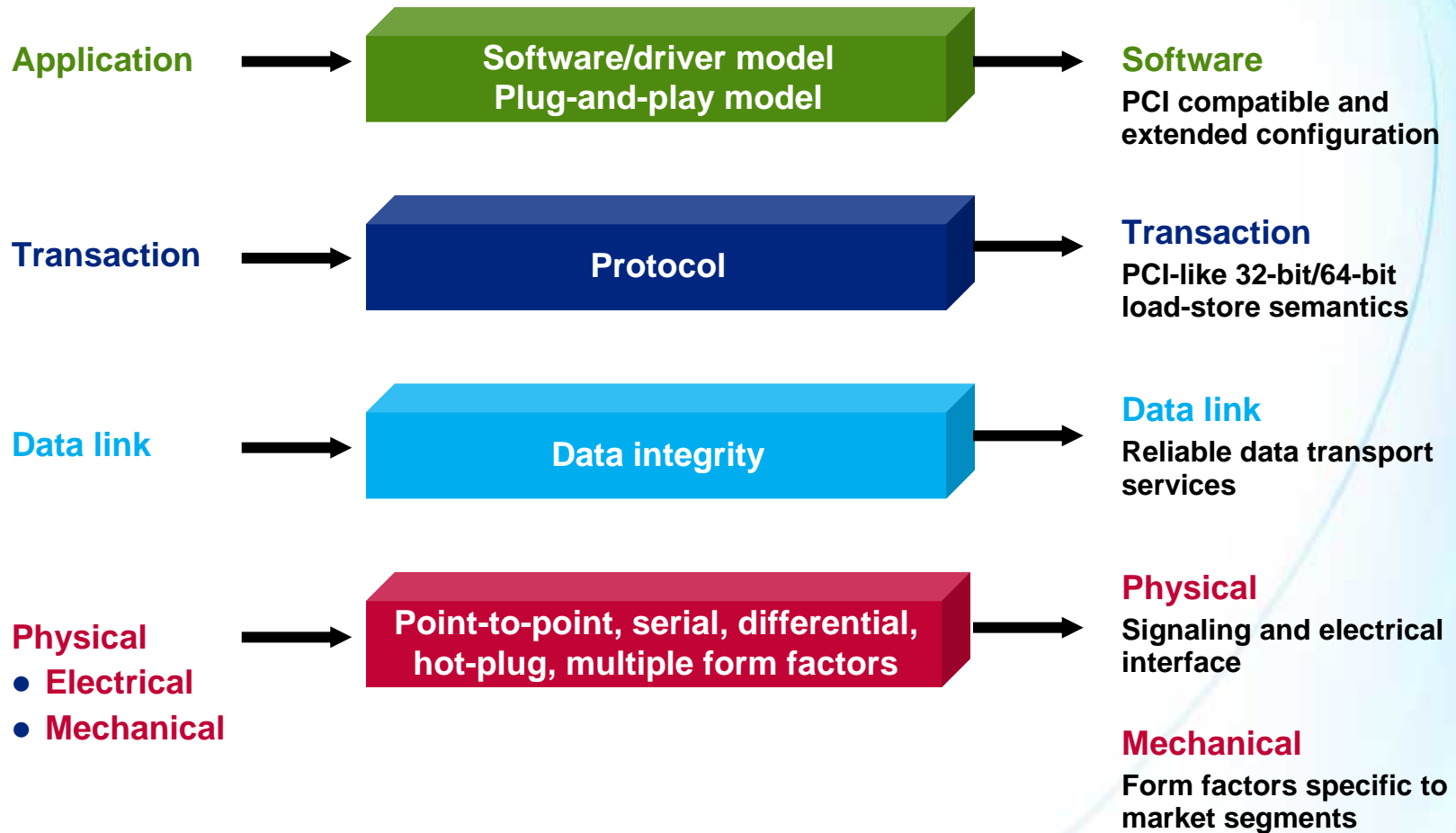
2

PCIe Technology Timeline

	Raw bit rate	Link BW	BW/lane/ way
PCIe 1.x	2.5 GT/s	2 Gbps	~250 Mbps
PCIe 2.0	5.0 GT/s	4 Gbps	~500 Mbps
PCIe 3.0	8.0 GT/s	8 Gbps	~1 Gbps

- Gen3: 8 GT/s signaling
- Atomic ops, caching hints
- Lower latencies, improved PM
- Enhanced software model

PCIe Gen1 @ 2.5 GT/s

PCIe Gen2 @ 5 GT/s

I/O virtualization Device sharing

PCI/PCI-X

Gbps

60 50 40 30 20

1999 2001 2003 2005 2007 2009 2011 2013

Note:
Link BW = 0.8 x (raw bit rate) in Gen1/Gen2 due to 8B/10B encoding
Dotted line is for projected numbers

PCI Express Protocol Stack

Application →	Software/driver model Plug-and-play model	**Software** PCI compatible and extended configuration
Transaction →	Protocol	**Transaction** PCI-like 32-bit/64-bit load-store semantics
Data link →	Data integrity	**Data link** Reliable data transport services
Physical ● **Electrical** ● **Mechanical** →	Point-to-point, serial, differential, hot-plug, multiple form factors	**Physical** Signaling and electrical interface **Mechanical** Form factors specific to market segments

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PCI Express – Point-to-Point Serial Interconnect

- Link: Full-duplex connection between two PCI Express devices

- Lane: Consists of differential signal pairs in each direction
  - 8b10b encoded in Gen1 or Gen2
  - 2.5 Gbps or 5.0 Gbps
  - x1, x2, x4, x8, x16…
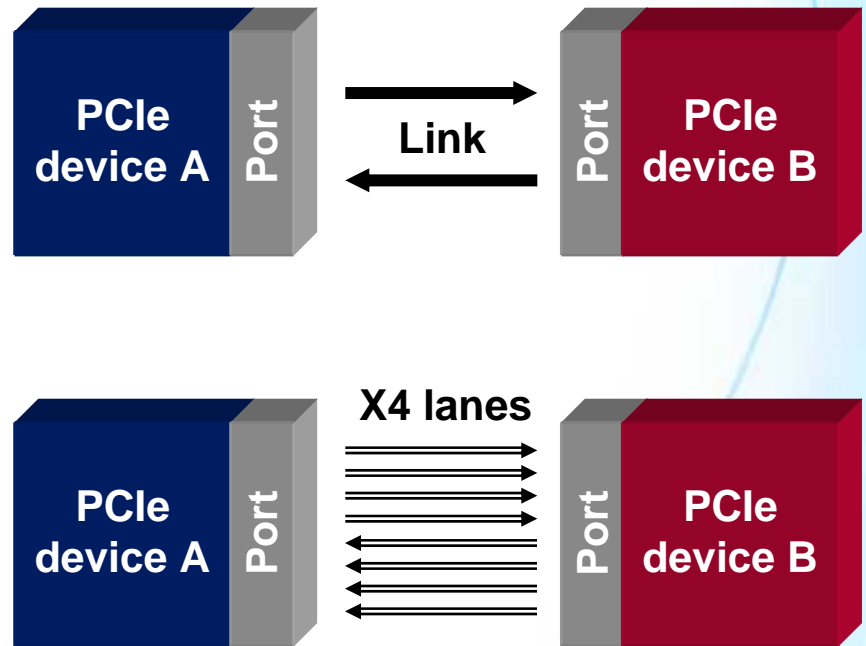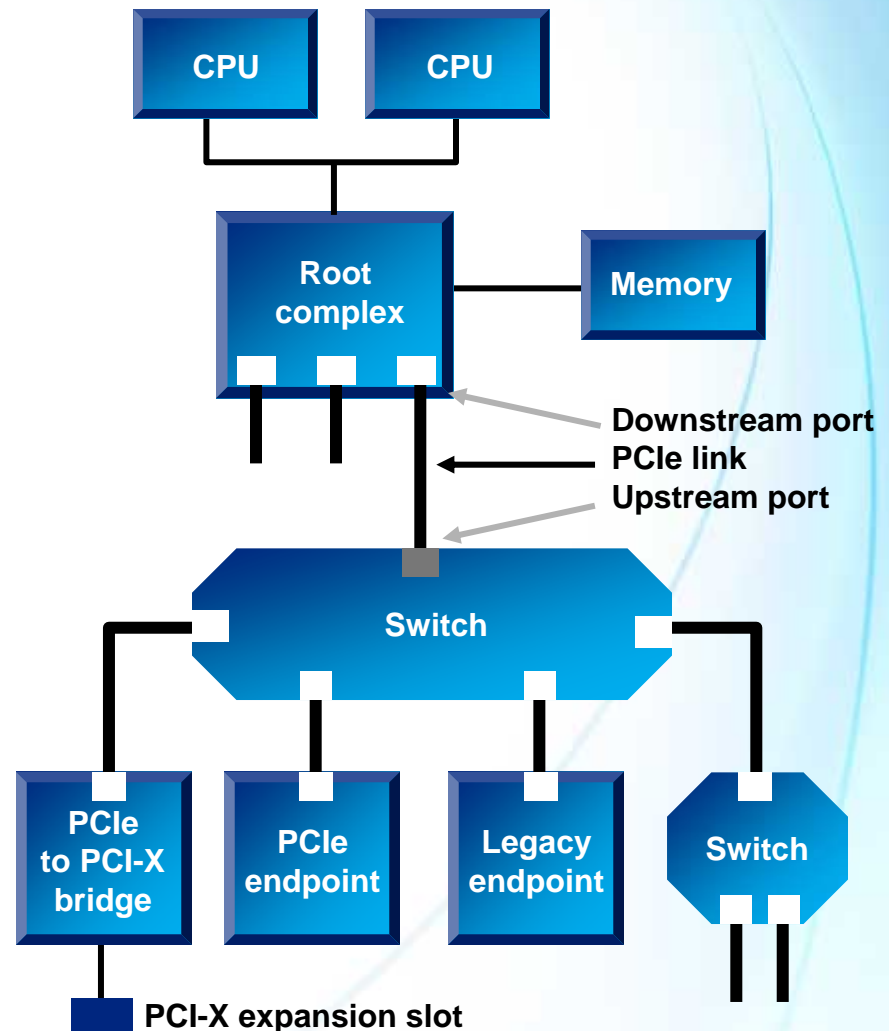
PCIe Functional Elements

- Root complex
  - Connects host CPU/memory complex to PCIe hierarchy
  - One or more downstream ports (= rootports)
  - Rootport discovers, initializes, and enumerates PCIe topology
- Switch
  - Assembly of logical PCIe-to-PCIe bridges
  - One upstream port directed towards root complex
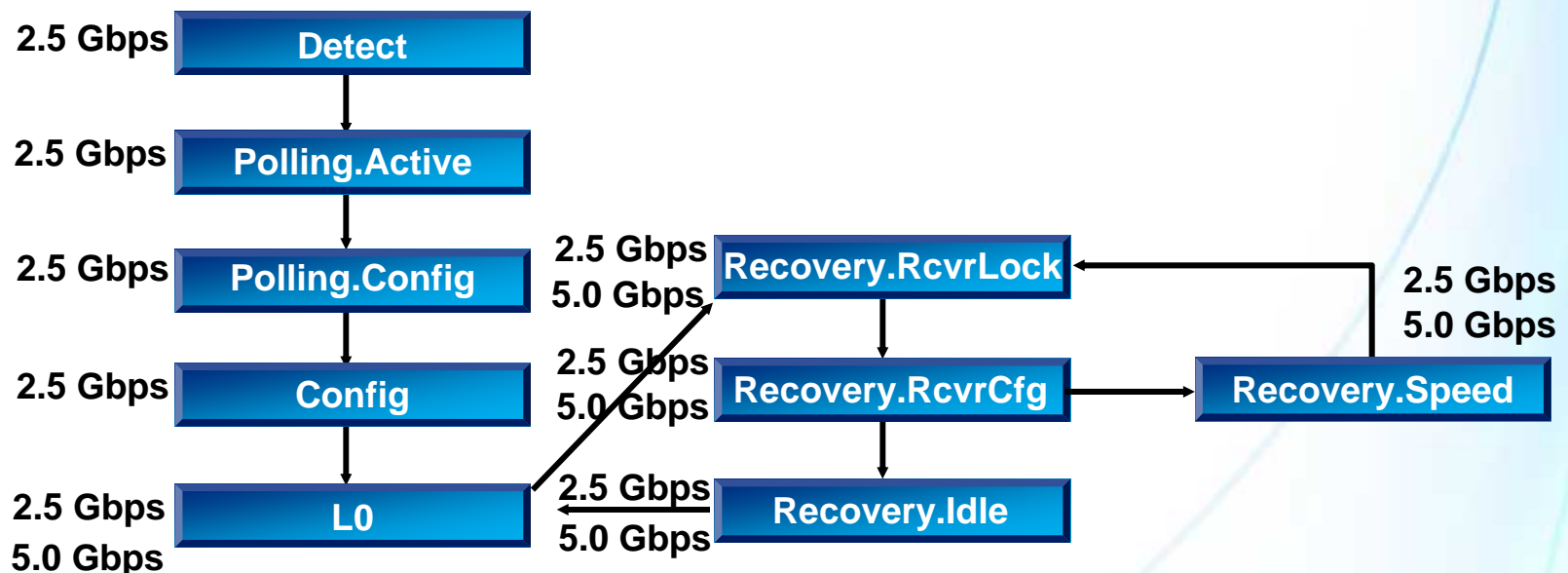 - One or more downstream ports
- Endpoint
  - Legacy and native endpoints e.g. terminal point to PCI, USB, InfiniBand, Fibre Channel, Ethernet...

CPU **CPU**

Root complex

Memory

Downstream port
PCIe link
Upstream port

Switch

PCIe to PCI-X bridge **PCIe endpoint** **Legacy endpoint** **Switch**

PCI-X expansion slot

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Auto Speed Negotiation

- Initially link trains to L0 (normal operation) in 2.5G data rate
- Speeds advertised in training sequence (TS) ordered sets
  - Supported speeds by the other component noted
- Speed change occurs when the link is in electrical idle

2.5 Gbps	**Detect**
2.5 Gbps	**Polling.Active**
2.5 Gbps	**Polling.Config**
2.5 Gbps	**Config**
2.5 Gbps / 5.0 Gbps	**L0**

2.5 Gbps / 5.0 Gbps → **Recovery.RcvrLock**

2.5 Gbps / 5.0 Gbps

2.5 Gbps / 5.0 Gbps

Recovery.RcvrLock → **Recovery.RcvrCfg** → **Recovery.Speed**

2.5 Gbps / 5.0 Gbps

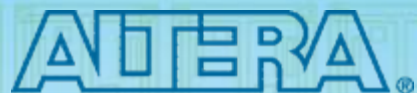**Recovery.RcvrCfg** → **Recovery.Idle**

Future PCIe Direction: I/O Virtualization

- May be useful in multi-core, multi-CPU or multi-line card systems
- PCIe supports single-root or multi-root I/O virtualization modes
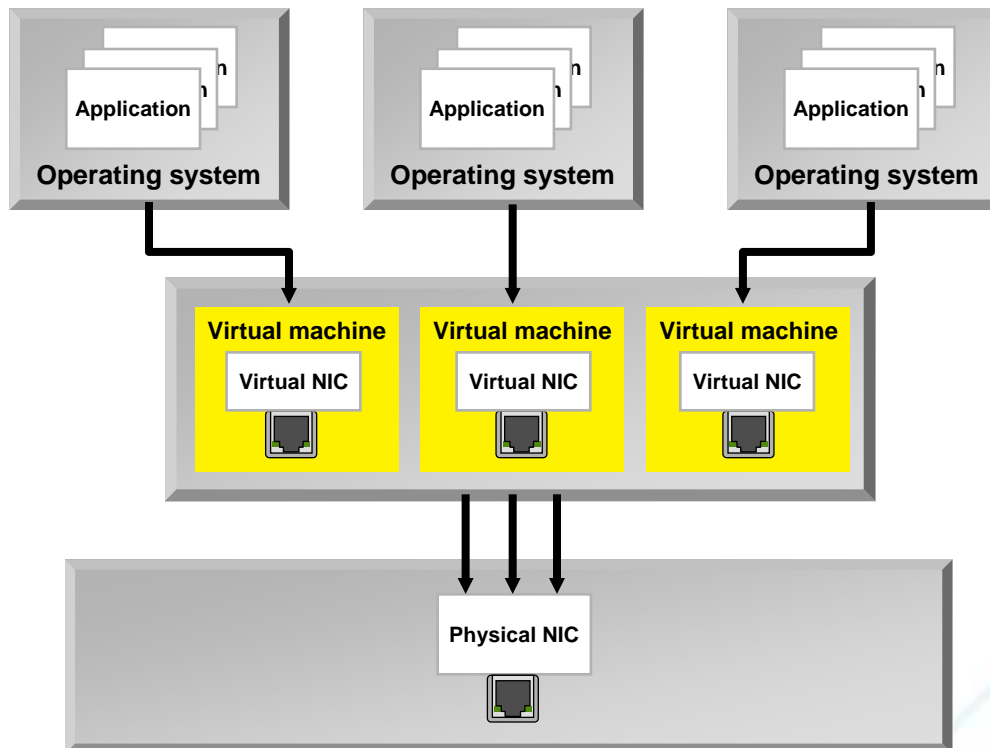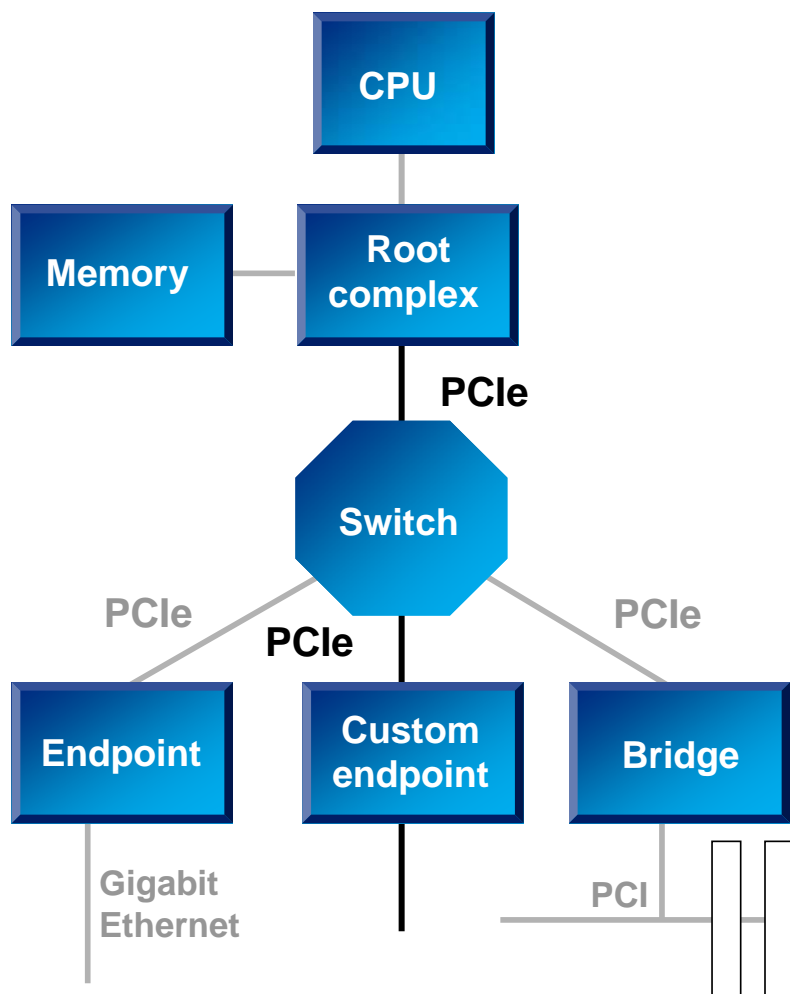

Virtualization is the concept of sharing a single platform (a physical set of hardware like CPU, IO, memory, etc) among multiple software operating environments (e.g. OSs)

Altera PCI Express Landscape

Altera PCI Express Focus

CPU

Memory — **Root complex**

PCIe

Switch

PCIe   **PCIe**   **PCIe**

Endpoint   **Custom endpoint**   **Bridge**

Gigabit Ethernet

PCI

- ■ Ensuring customer success by:
  - – Providing complete PCI Express solutions
  - – Low-cost/high-volume designs to high-performance device families
  - – Altera IP for PCI Express applications
    - ● Endpoint, switch, root complex, non-transparent/transparent bridging support also using partner IP
  - – With a focus on ease of use
  - – A solid commitment to hardware validation

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Altera PCI Express Solutions

Value proposition of hard IP

- Reduce device cost
  - Users can fit designs in smaller FPGA
    - Up to 40 KLE (x8 Gen2 configuration)
- > 50% power savings relative to equivalent soft IP core
- Shorter design and compile times
  - Easier timing closure
- Pre-verified complex IP

	Hard PCI Express IP	Soft PCI Express IP
Generation	Gen1 and Gen2	Gen1
Configuration	X1, x4, x8	X1, x4, x8
Supported devices	Stratix IV GX, HardCopy IV GX, Stratix IV GT, and Arria II GX FPGAs	Stratix GX, Stratix II GX, Stratix IV GX, HardCopy IV GX, Stratix IV GT, Arria GX, and Arria II GX FPGAs
Development kits	Stratix IV GX and Arria II GX FPGAs	Arria GX, Arria II GX, Stratix IV GX, and Stratix II GX FPGAs

PCIe Support in Altera Devices

Device	Hard IP Gen1/2		Soft IP Gen1	
	Supported	PCI Express configuration	Supported	PCI Express configuration
Arria II GX *(PCIe Gen1 only)*	☑ 1 per device	X1, x4, x8	☑	X1, x4
Stratix IV GX	☑ 2 to 4 per device	x1, x4, x8	☑	x1, x4
HardCopy IV GX	☑ 1 to 2 per device	x1, x4, x8	☑	x1, x4
Stratix IV GT[1]	☑	X1, x4	☑	X1, x4
Arria GX			☑	x1, x4
Stratix II GX			☑	x1, x4, x8
Stratix GX			☑	x1, x4
Cyclone II[2]			☑	x1

[1]Only supported by one quad in devices with F1932 package
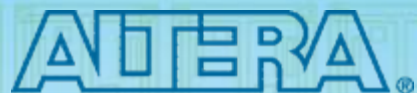[2]Cyclone II FPGA uses an external PCIe PHY

Altera PCI Express Solutions

- Industry-leading solutions
  - Stratix IV GX FPGA is industry's only shipping FPGA solution with hard IP support for PCIe Gen2
  - Stratix IV GX FPGA is industry's only FPGA solution with hard IP support for Gen2 x8 configurations
  - Arria II GX FPGA is the industry's first low-cost 40-nm FPGA with hard IP support for PCIe Gen1 x1, x4, x8

- Low-risk, hardware-verified solutions
  - PCI-SIG compliance workshops
  - Interoperability with multiple ASSP vendors
  - 5 generations of transceiver-based FPGAs with PCI Express support
  - Development kits/demo boards

PCI Express IP Cores

Altera PCIe Hard IP Features

- Endpoint (EP)/rootport (RP) dual-mode core
  - RP for embedded applications only
  - Can dynamically switch between EP and RP modes

- PCIe Base rev 1.1 or 2.0 compliant protocol stack
  - Integrated TL, DLL, PHY MAC, and transceivers
    - 2.5 Gbps (Gen1) and **5.0 Gbps**[*] (Gen2) per lane

- x1, x4, x8 initial link width configurations
  - Supporting down-configuration (including x2)

- Configurable maximum payload size
  - 128, 256, 512, **1K**[*] and **2K**[**] bytes

- 1, **2**[*] or **4**[*] hard IP cores per device

- 1 or **2**[*] virtual channels

- Single function support

- High-performance throughput
  - Close to the maximum theoretical bandwidth

(*) Available only in Stratix IV GX and HardCopy IV GX devices
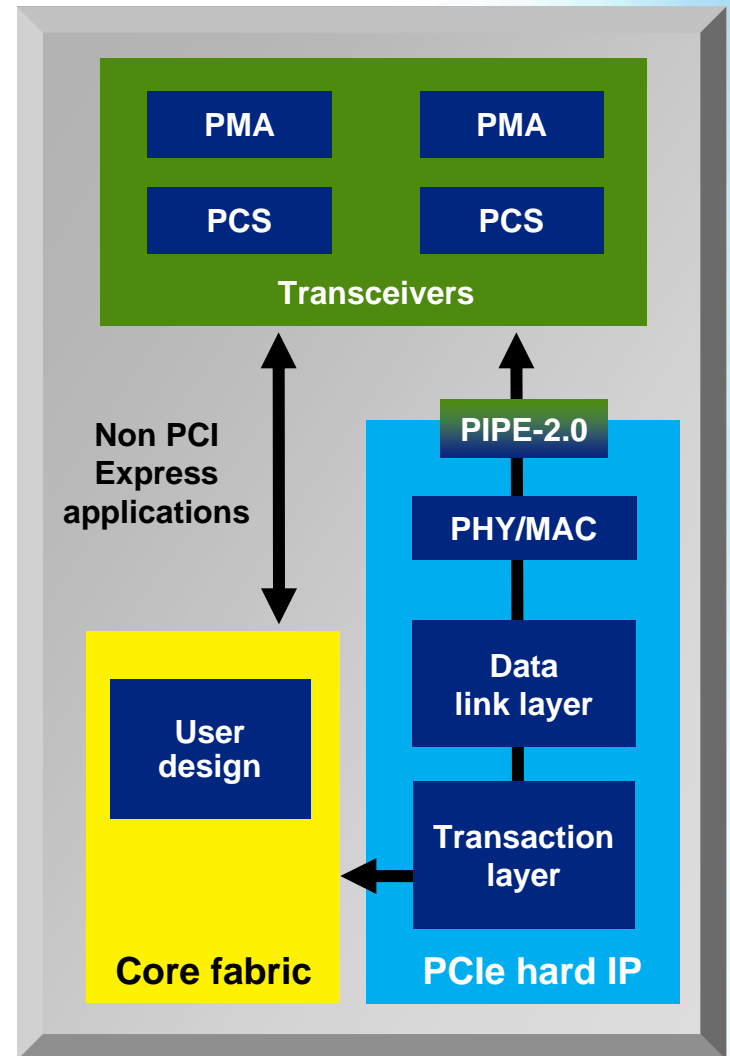**(**) Not available in HardCopy IV GX ASIC**

Notes:
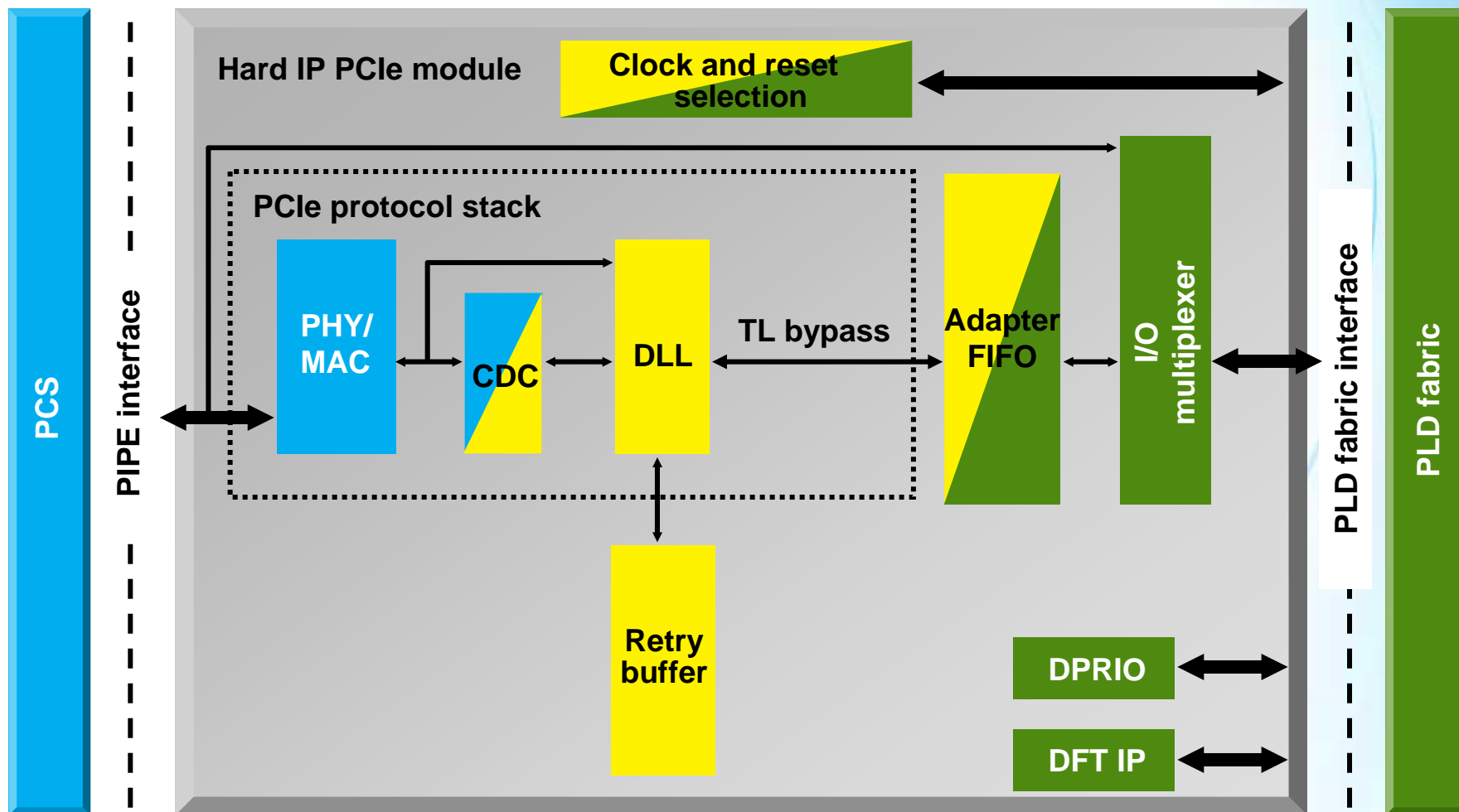**-** The HIP does not support:: x16 link width, IO Virtualization, Gen3

15

PCI Express Made Easy

- Built-in, pre-verified PCIe hard IP

- Guaranteed timing

- Flexible Gen1 and Gen2 x8, x4, x2, x1, rootport, and endpoint configurations
  - Stratix IV GX/GT and HardCopy IV GX devices
    - PCIe Gen1 and Gen2
  - Arria II GX FPGA – PCIe Gen1

- SOPC Builder ready

- Configured with PCIe Compiler MegaWizard™

- Complete example design provided

- Reduced costs
  - Saves up to 15K LEs
  - No license fees

| PMA | PMA |
| PCS | PCS |

Transceivers

Non PCI Express applications

PIPE-2.0

PHY/MAC

Data link layer

User design

Transaction layer

Core fabric

PCIe hard IP

| Soft logic | PCI Express hard IP | PCS/PMA |

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Transaction Layer Bypass Block Diagram

CDC = Clock domain crossing FIFO

Soft IP Core for PCI Express

Physical layer

Upper protocol layers   **Physical coding sub-layer**

PCI Express IP core x1 x4 x8

PIPE interface

| PCS | SERDES x1 |
PCS	SERDES x1
PCS	SERDES x1
PCS	SERDES x1
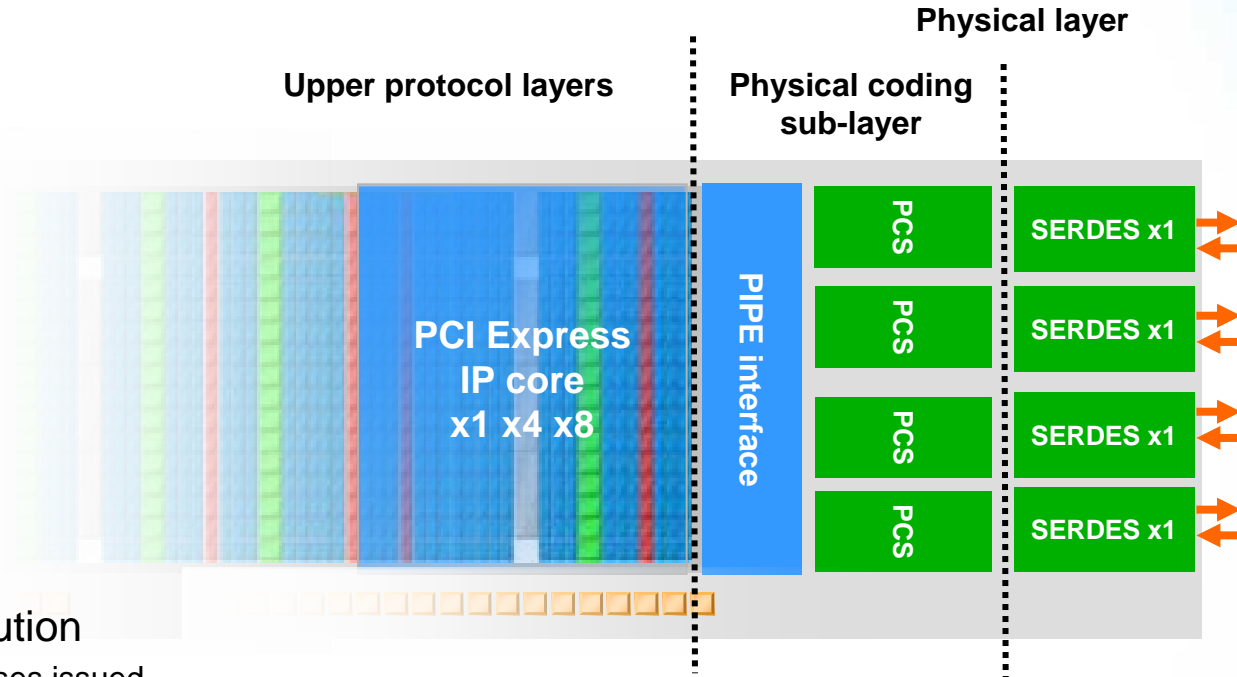
- **Proven solution**
  - ~150 licenses issued
  - PCI Express 1.1 compliance
  - Extensive performance benchmarking data across multiple chipsets/platforms
  - Additional interoperability with multiple ASSPs

- **Flexible and feature rich**
  - Easy timing closure with support for incremental compilation
  - Easy integration using SOPC Builder (x1, x4)
  - Configurable maximum payload up to 2 Kbyte and configurable retry buffer
  - Optional end-to-end cyclic redundancy code (ECRC) generation/checking and advanced error reporting (AER)
  - Flexible reference clock support (100, 125, or 156.25 MHz)

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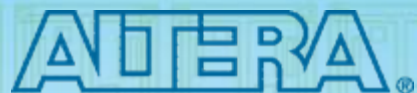
PCI Express Testing

Preliminary PCI Express Characterization Testing

- PMA and PCS Gen1 and Gen2 compliant
- HIP Gen1 and Gen2 complete (x8 Gen2 in process)

Characterization test	Compliant to spec.
Tx electrical buffer	✓
Tx AC/DC parameters	✓
CMU jitter generation across modes	✓
CMU jitter generation statistical analysis	✓
CMU jitter transfer	✓
CDR jitter transfer	✓
CDR jitter tolerance	✓
Rx signal detect threshold	✓
Rx signal detect timing	✓
Rx / Tx return loss	✓
Rx / Tx impedance	✓
CDR lock to data	✓
CDR f_{MAX} vs V_{ID} and V_{CM}	✓
PMA PCIe compliance test using PCI Express electrical test software: SIGtest version 3.1.9	✓

Characterization test	Compliant spec.
PIPE power state transition	✓
PIPE forcing negative disparity	✓
PIPE auto speed negotiation	✓
PPM detector behavior after speed negotiation	✓
PIPE Tx electrical idle response time	✓
PIPE rate match FIFO clock tolerance	✓
PIPE pipestatus signal verification	✓
PCIe HIP PHY and data link layer bring up	✓
PCIe HIP Gen1 ×1 stress test	✓
PCIe HIP Gen1 → Gen2 auto speed negotiation	✓
Tx lane-to-lane skew	✓
Tx detect Rx	✓
Tx intra differential pair skew	✓
CDR run-length violation	✓
CDR clock PPM difference tolerance	✓
CDR lock to reference	✓

PCIe Hard IP Testing

- **Interoperability testing**
  - Compatibility/functionality with chipsets
    - Core generator with verifying payloads (built in DMA engine)
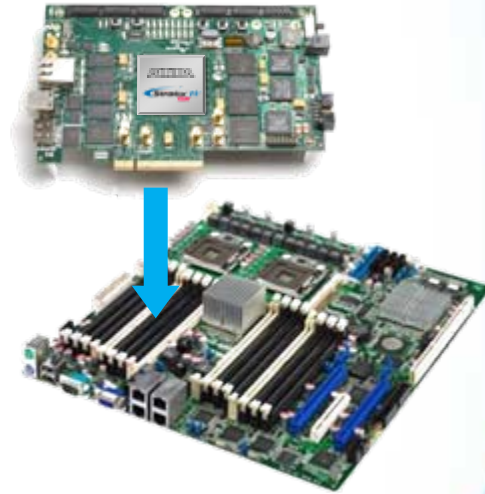 - Test for PCIe compliance using PCI-SIG tests

- **Performance testing**
  - Testing throughput of PCIe link
  - Stress test using the chain DMA architecture

- **Test configurations**
  - Modes
    - PCI Express Gen1 x1, x4, x8
    - PCI Express Gen2 x1, x4

Altera PCIe Gen2 development card

PCIe Gen2 motherboard

PCIe Gen2 platforms			
	Motherboard	**Chipset**	**Processor**
AMD	**Asus M3A78-T**	**790GX/SB750**	**AMD790GX**
Intel	**Asus P5Q-EN**	**Intel-645**	**LGA775**
Intel	**DX58S0**	**Tylersburg**	**Core I7**

Preliminary Results of PCI Express Hard IP Bandwidth Testing – Tylersburg Chipset

HIP configuration	DMA write	DMA read	Simultaneous read/write
HIP:Gen1:x8:128 bits	1,691 Mbps	1,695 Mbps	1,683/1,449 Mbps
HIP:Gen1:x8:64 bits	1,774 Mbps	1,522 Mbps	1,524/1,631 Mbps
HIP:Gen2:x4:64 bits	1,772 Mbps	1,528 Mbps	1,528/1,634 Mbps
HIP:Gen2:x4:128 bits	1,670 Mbps	1,613 Mbps	1,607/1,402 Mbps

- **Theoretical maximum bandwidth**
  - Gen1 x8, Gen2 x4: 2,000 Mbps
- **Stratix IV GX hard IP is close to theoretical maximum now**

PCI-SIG Industry Testing – PCI-SIG

FPGA/PHY	Config.	PCIe IP	PCI-SIG qualification
Arria II GX (Gen1)	X1, x4, x8	Hard IP	Q309
Stratix IV GX (Gen1 and Gen2)	X1, x4, x8	Hard IP	☑ 1Q09
Arria GX (Gen1)	x1,x4	Soft IP	☑ 2Q07
Stratix II GX (Gen1)	x1, x4, x8	Soft IP	☑ 2Q06
Cyclone II/TI x1 (Gen1)	x1	Soft IP	☑ 1Q06
Cyclone II/Philips x1 V (Gen1)	x1	Soft IP	☑ 4Q05
Stratix GX (Gen1)	x1, x4	Soft IP	☑ 1Q05

■ **PCI-SIG qualification across all target lane configurations**
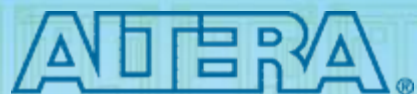
Development Kits

Stratix IV GX and HardCopy IV GX Development Kit

- PCI Express short form factor
- Included daughtercards
  - HSMC loop-back
  - HSMC debug
- Included software
  - Quartus II Development Kit Edition
    - 12-month license
  - Example designs
    - Board design test system
    - Nios II web server features system remote update
    - myFirst Nios and FPGA
- Documentation
  - User guide
  - Reference manual
 - Schematics
  - Layout design files

| Preliminary schedule	
Book orders	March 28, 2009
FAE boards	March 28, 2009
Production	May 15, 2009

Arria II GX Development Kit

- **PCI Express short form factor**

- **Included daughtercards**
  - HSMC loop-back
  - HSMC debug

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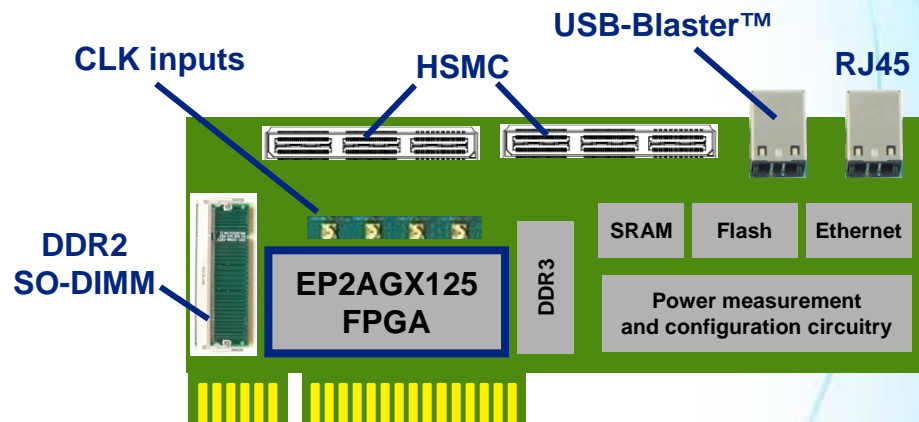
Preliminary schedule	
Book orders	**July 2009**
FAE boards	**July 2009**
Production	**Aug. *Limited quantities End Sept **1-week lead-time**

Stratix II GX Development Kit

- ~500 developments kits shipped
- Complete PCI Express experience
  - PCI-SIG compliant Stratix II GX EP2SGX90F1508C3 FPGA/board
  - PCI-SIG compliant x1, x4, x8 IP core (OpenCore Plus)
  - 1-year Quartus II software license
  - Board schematics, layout information
  - Example design and supporting documentation
- Modular and scalable design
- System level memory
  - DDR2 333-MHz components
  - QDR2 300-MHz components
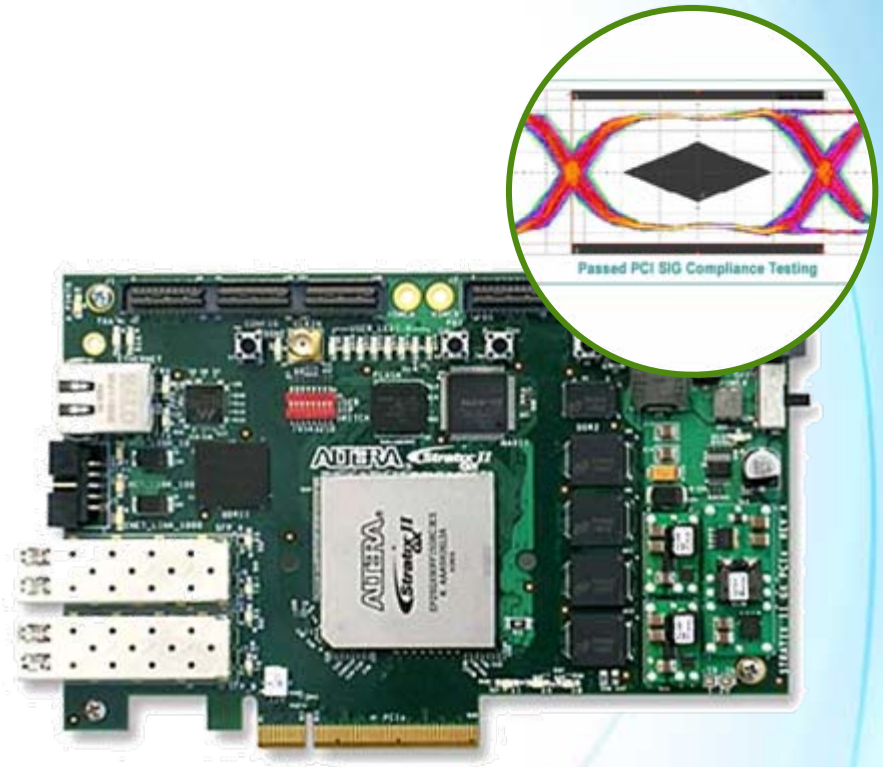
Out-of-the-box proven PCI Express experience

Arria GX Development Kit

- PCI Express x1, x4 compliance

- Gigabit Ethernet (with daughtercard)

- Serial RapidIO® 1.25 and 2.5 Gbps (with daughtercard)

- DDR2

- 1 HSMC connector

- JTAG header

- Complete documentation and support

28

![ALTERA logo]

Thank You

Hard IP and Soft IP Features Comparison

Features	Hard IP	Soft IP	
	MegaWizard™ Plug-In Mgr	MegaWizard Plug-In Mgr	SOPC Builder
Gen1/Gen2	Yes/Yes	Yes/No	Yes/No
x1/x4/x8	Yes/Yes/Yes	Yes/Yes/Yes	Yes/Yes/No
Avalon®-MM Interface	Yes (with a wrapper)	No	Yes
Avalon-ST 64b/128b I/F	Yes/Yes	Yes/No	No/No
Desc/data interface	No	Yes	No
Legacy endpoint	Yes	Yes	No
I/O and messages	Yes	Yes	No
Max payload size	128B-2KB	128B-2KB	128B-256B
Num of VC	2	1-4	1
Reordering of OOC	No	No	Yes
Reqs cross 4KB boundary	No	No	Yes
Nr of tags (NP reqs)	32 or 64	4 to 256	16
ECRC forwarding	Yes	No	No
MSI-X	Yes	No	No
Rootport	Yes	No	No
License required	No	Yes	Yes