INFORCE COMPUTING

Display Interfaces

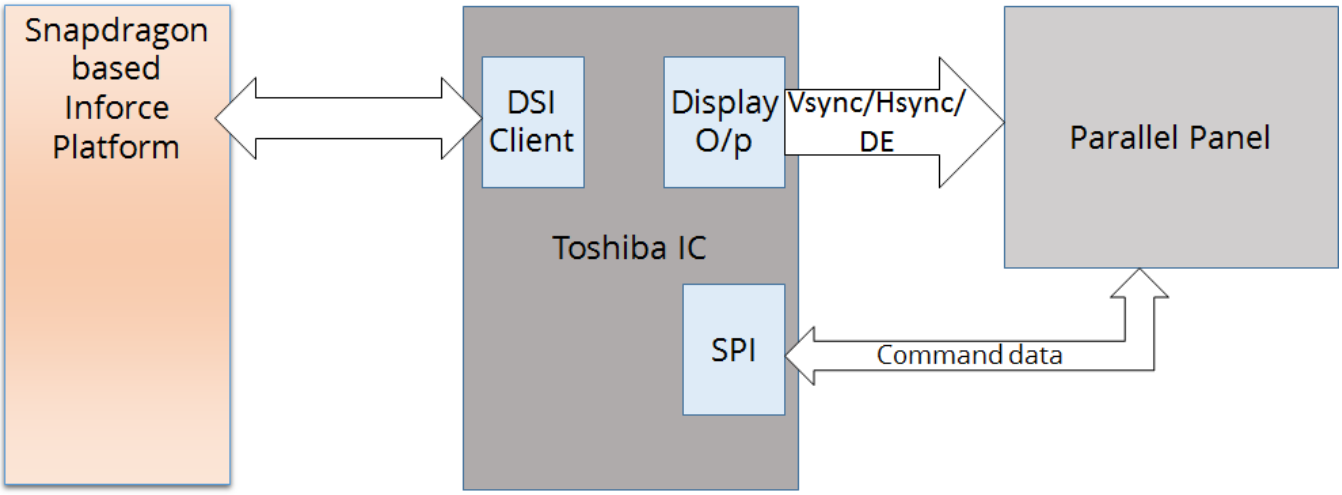
Snapdragon processors natively support a few popular graphical displays like MIPI-DSI/LVDS and HDMI or a combination of these. HDMI displays that output any of the standard resolutions typically work out of the box on Snapdragon based platforms but displays of other electrical interfaces require programming to be done. Different use-cases on Snapdragon processors' based systems necessitate different types of displays that have to work. It thus becomes essential to do signal conversions when required to support all kinds of displays. Certain use-cases may require an additional independent display of the same type, say a second HDMI port, to be supported which also require conversions from one type to the other. The display interfaces can be categorized as:

- **Parallel RGB Interface** - A parallel interface configuration usually has a full data width, but no address bus. A RGB interface is a special kind of parallel interface. This interface works for displays without a frame buffer. Thus the display get updated manually, by providing both pixel data and timing signals from a control unit.
- **LVDS** – Low Voltage Differential Signaling is a unidirectional digital data display interface in which an LVDS transmitter IC is used to encode up to 24 bits of data per input clock onto four differential serial pairs. It involves serialization of the input data, distributing it among the four (or eight) serial pairs, and transmitting it at a clock rate seven times the original. An LVDS receiver accepts the data and clock pairs, uses the clock to both de-serialize the data and to regenerate the original-rate pixel clock, and provides the video data, control signals, and clock as separated outputs.
- **MIPI-DSI** - MIPI's Display Serial Interface (DSI) is also an unidirectional digital data interface between the processor and the display. The interface typically consists of 4 data lanes and each data lane consists of two differential pins and two pins of differential clocks. A 4-lane interface would thus consist of four differential pairs (8 pins) plus one differential clock pair (2 pins) thus totaling 10 signal pins.
- **HDMI** – HDMI interface delivers uncompressed digital video and multi-channel audio through TMDS which again is a differential signaling technology for transmitting high-speed serial data. The three main color components of video signals, red, green and blue, are broken out and sent separately over a shielded pair of twisted pair of wires together with a clock signal, to lower the possibility of any interference, thus totaling 12 pins of the connector.

Display solutions from Inforce

MIPI-DSI to Parallel RGB format

The use-case necessitated a very small LCD panel of around 2" and DSI panels of this size aren't commonly available. Parallel RGB interface LCD screens though are easily available in this size and since Snapdragon 805 supports DSI alone natively, a conversion of DSI lanes to parallel 16 bit RGB (656) format was required. We chose a Toshiba IC that de-serializes the high-speed serial data stream from Snapdragon via DSI interface into a parallel stream to output to the display panel.



DSI Receiver capabilities

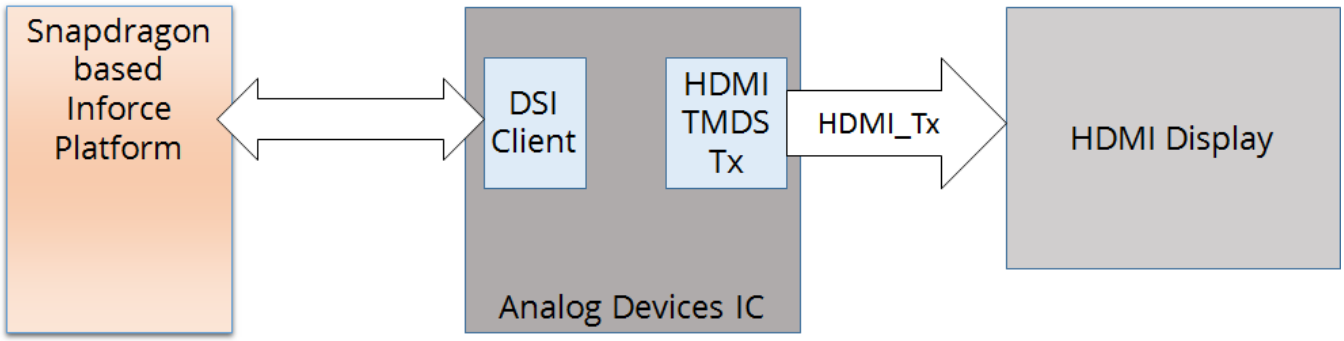
- MIPI DSI-RX Data 2-lane, CLK 1-lane with data rates up to 800 Mbps/lane
- Video input frame rates: Up to 60 fps for XGA, 30 fps for 720P
- Video input data formats: RGB888, RGB666 and RGB565.

Display Host capabilities

- Bus speed up to 70 MHz with data rate up to 210 Mbytes/s
- Supports up to 60 fps for XGA, 30 fps for 720P
- Supports the following pixel formats:
    - RGB666 18 bits per pixel
    - RGB666 loosely packed 18 bits per pixel
    - RGB565 16 bits per pixel
    - RGB565 loosely packed 16 bits per pixel
    - RGB888 24 bits per pixel

DSI to HDMI

Snapdragon 410 natively supports only MIPI-DSI display interface. Application space use-cases require HDMI displays to be supported since they are plug-and-play and are widely available in all sizes and standard resolutions. To implement this conversion, we chose an IC from Analog Devices that provides a MIPI-DSI input port and an HDMI data output in a 49-Wafer Level Chip Scale Package.



DSI Receiver capabilities

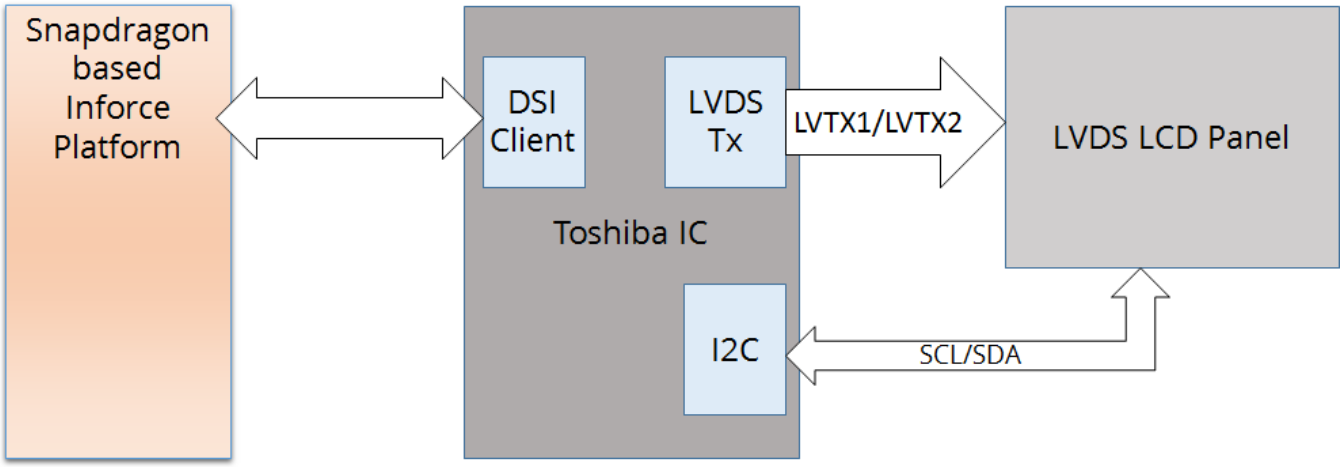
- Low power MIPI/DSI receiver
- 2-, 3-, or 4-lane DSI receiver
- Supports up to 800 Mbps per lane
- Compatible with DPHY V.0.90 and DSI V.1.02
- Supports inputs of 16-bit RGB 4:4:4; 24-bit RGB 4:4:4; 30-bit RGB 4:4:4

HDMI (TMDS) out capabilities

- 80 MHz operation supports all video and graphics resolutions from 480i to 1080p at 30 Hz
- Programmable 2-way color space converter
- Supports 36-, 30-, or 24-bit RGB 4:4:4; 36-, 30-, or 24-bit YCbCr 4:4:4
- Automatic input video format timing detection (CEA-861E)
- S/PDIF for stereo LPCM or compressed audio up to 192 kHz
- 2-channel uncompressed LPCM I2S audio up to 192 kHz

DSI to LVDS

LVDS is a preferred display type for industrial use-cases owing to its ubiquitous availability in small sized panels. Snapdragon 410 natively supports only MIPI-DSI display interface and thus a conversion to LVDS was necessary. To implement this conversion, we chose a low power bridge chip from Toshiba that enables video streaming output over DSI link to drive LVDS-compatible display panels. To cater to industrial use-cases, we also ensured that the entire platform, including this display conversion supports extended temperature range.



DSI Receiver capabilities

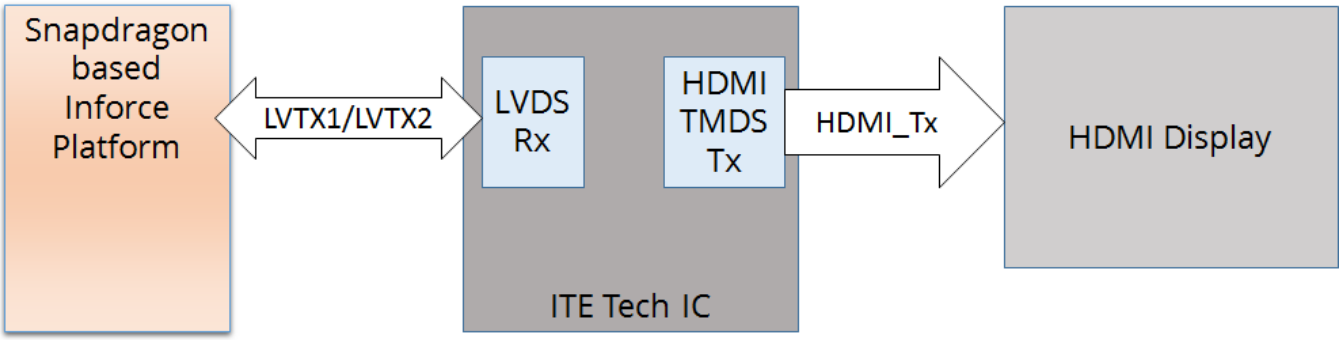
- Configurable 1- up to 4-Data-Lane DSI Link with bi-directional support on Data Lane 0
- Maximum bit rate of 1 Gbps/lane
- Supports inputs of 16-bit RGB565; 18-bit RGB666; 24-bit(loosely packed) RGB666; 24-bit RGB888
- Compatible with DPHY V.0.90 and DSI V.1.02
- Supports up to WUXGA resolutions (1920×1200 24-bit pixels) to dual-link LVDS display panel.

LVDS FPD Link Transmitter capabilities

- Supports single-link or dual-link
- Maximum pixel clock speed of 135 MHz for single-link or 270 MHz for dual-link
- Supports outputs of RGB666 18 bits per pixel; RGB888 24 bits per pixel
- Features Toshiba Magic Square algorithm which enables a RGB666 display panel to produce a display quality almost equivalent to that of an RGB888 24-bit panel

LVDS to HDMI

Video conferencing use-cases necessitate multiple HDMI outputs. Snapdragon 600 processors support one each of LVDS and HDMI display interfaces natively and thus the LVDS output had to be converted to a second HDMI output to cater to this use-case. To do this conversion, a high-performance single-chip De-SSC LVDS to HDMI converter IC from ITE Tech was used.



LVDS RX Capabilities

- Supports single-link or dual-link
- Support input clock rate up to 150MHz
- Support input color depth up to 10bit
- Support De-SSC (De-Spread Spectrum)

HDMI (TMDS) out capabilities

- 225 MHz operation supports all video and graphics resolutions from 480i to 1080p at 60 Hz
- HDMI 1.4a transmitter compatible with HDMI 1.3, HDCP 1.2
- S/PDIF for stereo LPCM or compressed audio up to 192 kHz
- 8-channel uncompressed LPCM I2S audio up to 192 kHz

Other display related solutions

Apart from the various interface conversions described above, Inforce is capable of delivering many other display related solutions like:

- Add support for non-standard resolutions on HDMI which requires precise programming of the HDMI PLL for the required clock frequency.
- Add support in the kernel for any MIPI-DSI panel. The newer Snapdragon processors require bootloader changes too to accomplish this.
- Drive multiple independent MIPI-DSI display panels. Note that Inforce will create hardware to bring out individual D-PHY connectors on its platform and implement the required software to support this feature.
- Have any display interface as primary or secondary/external to replace the default screen mirroring.