

Engineering



Timer



Design

Preliminary

2015.01.20

Version 1.0

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0.1 Target

- Write a sequential design with verilog.

0.2 Specification

- File Name: TIMER.v
- Module Name: TIMER
- I/O Port

Port Name	Width	Attribute	Description
SYSCLK	1	Input	System Clock All registers must be synchronous with this clock. The period time of this clock is 1 second.
RST_B	1	Input	Global Reset Signal Asynchronous reset. Active low.
TIME_MIN	3	Input	Minute Number The number which the minute should reach.
TIME_SEC	6	Input	Second Number The number which the second should reach.
START	1	Input	Start Timer One pulse signal. When START==1, It start to timer.
MINUTE	3	Output	Timer Output the Current Minute Number Minute of timer.
SECOND	6	Output	Timer Output the Current Second Number Second of timer.
TIME_UP	1	Output	Time End One pulse signal. Active high.

0.3 Requirement

- Synchronous with the rising edge of system clock
- Asynchronous reset
- Match HE coding style, run he_vcheck to ensure quality of design
- When start the timer, TIME_MIN and TIME_SEC are valid and mustn't change until time end
- If TIME_MIN and TIME_SEC are both 0, TIME_UP will be valid with START at the same time
- After TIME_UP asserted, MINUTE and SECOND must hold until RST_B is valid.
- RST_B will be valid before every START

0.4 Waveform

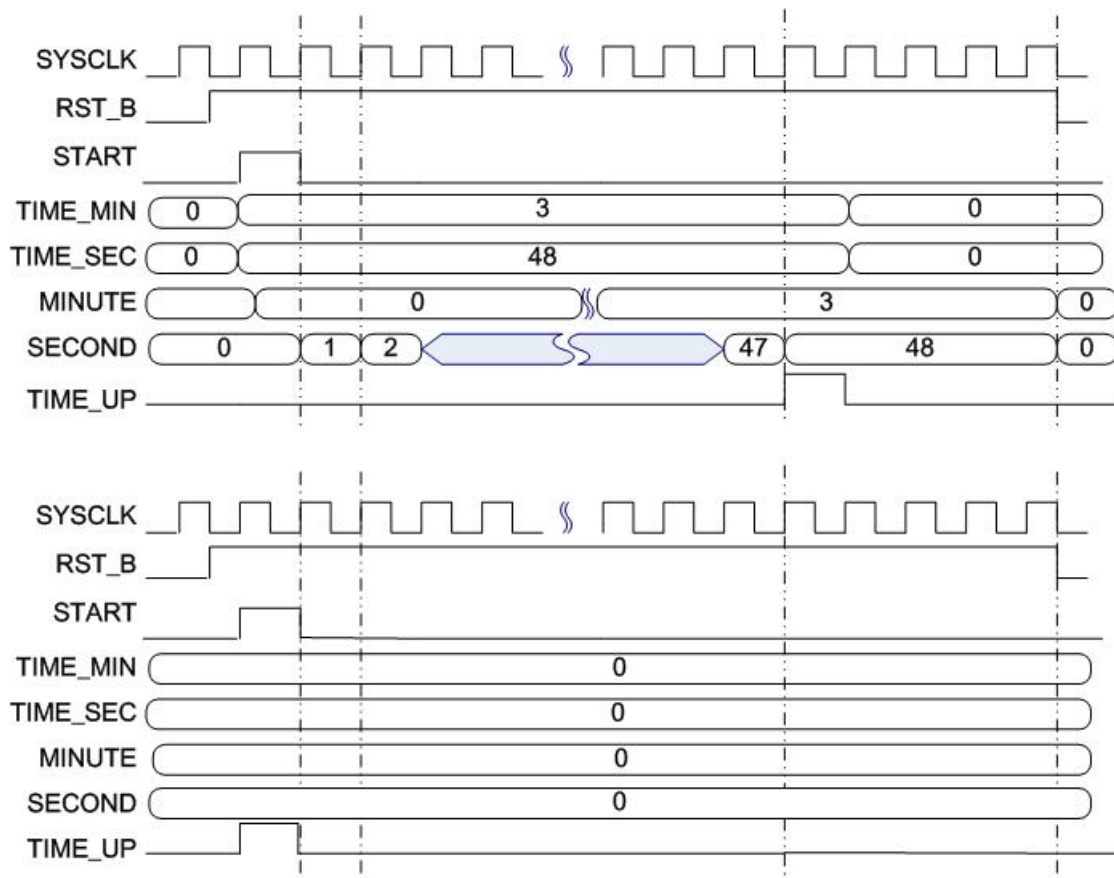


Figure 0.4.1: Waveform of Timer