

Sequence Detector

Design

Preliminary

2015.03.20

Version 1.0

SUNPLUS TECHNOLOGY CO. reserves the right to change this documentation without prior notice. Information provided by SUNPLUS TECHNOLOGY CO. is believed to be accurate and reliable. However, SUNPLUS TECHNOLOGY CO. makes no warranty for any error that may appear in this document.

Contact your local SUNPLUS sales office or your distributor to obtain the latest version of device specifications before placing your order. No responsibility is assumed by SUNPLUS for any infringement of patent or other rights of third parties that may result from its use.

In addition, SUNPLUS products are not authorized for use as critical components in life support devices/systems or aviation devices/systems, where a malfunction or failure of the product may reasonably be expected to result in significant injury to the user, without the express written approval of SUNPLUS.

SUNPLUS and SUNPLUS logo are trademarks or registered trademarks of SUNPLUS corporation or its subsidiaries.

Copyright © 2007 Sunmedia Corporation

0.1 Target

Implement the sequence detector design that can detect four consistency data according to the configuration mode and output the flag.

- Support increment mode that can detect four consistency increment data
- Support decrement mode that can detect four consistency decrement data
- Support steadiness mode that can detect four consistency same data

0.2 Specification

- File Name: SEQ_DETECTOR.v
- Module Name: SEQ_DETECTOR
- I/O Port

Port Name	Width	Attribute	Description
RST_B	1	I	System Reset Low active, when this pin is asserted, all flip-flops must be reset to their default value
SYSCLK	1	I	System Clock Free running clock, all registers must be synchronous with SYSCLK
IN_VALID	1	I	Input Valid High active, the input signal MODE and DATA_IN will only be valid when IN_VALID == 1. When IN_VALID == 0, the input MODE and DATA_IN should be ignored, and the state should be the same with when IN_VALID == 1
MODE	2	I	Detect Mode This signal determines the detecting mode <ul style="list-style-type: none">– 00: Increment detecting mode, which four consistency increment data like 1, 2, 3, 4 or 15, 0, 1, 2 can set OUT_VALID to logic 1– 01: Decrement detecting mode, which four consistency decrement data like 5, 4, 3, 2, or 0, 15, 14, 13, can set OUT_VALID to logic 1– 10: Steadiness detecting mode, which four consistency same data like 0, 0, 0, 0 can set OUT_VALID to logic 1– 11: Same to IN_VALID == 0
DATA_IN	4	I	Input Data It will only be valid when IN_VALID == 1 and MODE != 2'b11

OUT_VALID	1	O	Output Valid High active, it will be asserted when 4 consistency data has been received according to the detecting mode
DATA_OUT	4	O	Output Data When OUT_VALID is asserted, DATA_OUT should equal to DATA_IN, otherwise it should equal to 0

0.3 Requirement

- Synchronous with posedge clock
- Asynchronous Reset
- Use Melay FSM
- Match HE Coding Style
- No error with HE vcheck

Sunplus Confidential

0.4 Waveform

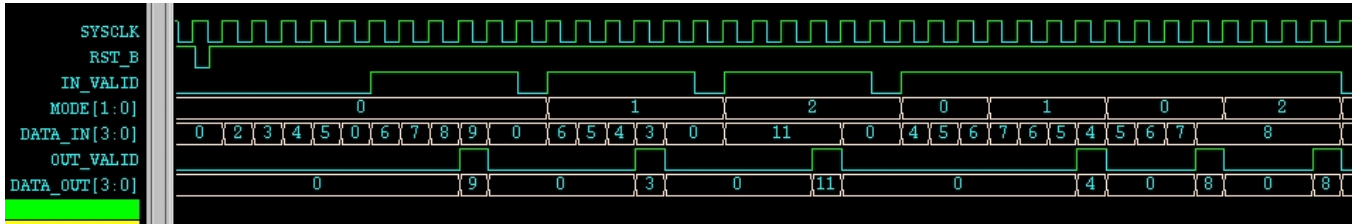


Figure 0.4.1: Waveform a

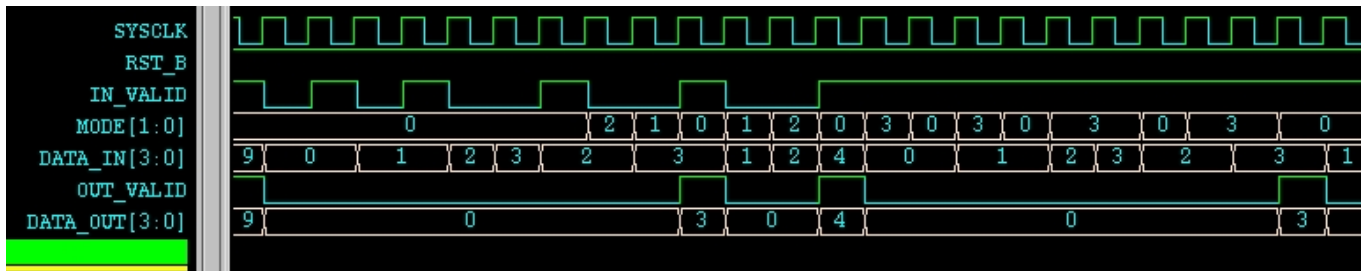


Figure 0.4.2: Waveform b