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Architectures	ARM	AARCH64	MIPS32	RV32E	RV32 / RV64	System V i386	System V x86_64
Arguments	r0 - r3	r0 - r7 specially r8	a0 - a3 ($4 - $7)	a0 - a5 (x10 - x15)	a0 - a7 (x10 - x17)	none	rdi, rsi, rdx, rcx (r7, r6, r2, r1) r8, r9
Additional arguments	stack	stack	stack	stack	stack	stack (right to left)	stack (right to left)
Return value	r0, r1	r0 - r7 *r8	v0, v1 ($2, $3)	a0, a1 (x10, x11)	a0, a1 (x10, x11)	eax, edx (r0, r2)	rax, rdx (r0, r2)
Stack pointer	sp (r13)	SP	sp ($29)	sp (x2)	sp (x2)	esp (r4)	rsp (r4)
Stack alignment	8-byte	16-byte	8-byte	4-byte	16-byte	16-byte	16-byte at call
Frame pointer	fp (r11)	fp (r29)	fp ($30)	fp (x8)	fp (x8)	ebp (r5)	rbp (r5)
Return address	lr (r14)	lr (r30)	ra ($31)	ra (x1)	ra (x1)	*(ebp + 4)	*(rbp + 8)
Scratch registers	r0 - r3 ip (r12) lr (r14)	r0 - r7 r8 r9 - r18 lr (r30)	v0, v1 ($2, $3) a0 - a3 ($4 - $7) t0 - t7 ($8 - $15) t8, t9 ($24, $25) ra ($31)	ra (x1) t0 - t2 (x5 - x7) a0 - a5 (x10 - x15)	ra (x1) t0 - t2 (x5 - x7) a0 - a7 (x10 - x17) t3 - t6 (x28 - x31)	eax, ecx, edx (r0, r1, r2)	rax, rcx, rdx (r0, r1, r2) rsi, rdi (r6, r7) r8 - r11
Preserved registers	v1 - v8 (r4 - r11) sp (r13)	r19 - r29 SP	s0 - s7 ($16 - $23) sp, s8 ($29, $30)	sp (x2) s0, s1 (x8, x9)	sp (x2) s0, s1 (x8, x9) s2 - s11 (x18 - x27)	ebx, esp, ebp, esi, edi (r3, r4, r5, r6, r7)	rbx, rsp, rbp (r3, r4, r5) r12 - r15
Thread pointer	TPIDRRO	TPIDR	UserLocal (cp0-reg4-sel2)	tp (x4)	tp (x4)	gs.base	fs.base
Global pointer			gp ($28)	gp (x3)	gp (x3)		
zero register		rzr	zero ($0)	zero (x0)	zero (x0)		
Platform register	r9	r18					
References	http://wiki.osdev.org/Calling_Conventions						
	http://www.slideshare.net/YiHsiuHsu/riscv-introduction						
	http://stackoverflow.com/questions/21748272/stack-alignment-on-x86						
	http://cons.mit.edu/sp14/x86-64-architecture-guide.html						
	https://www.uclibc.org/docs/tls.pdf						
From	Taiwan Linux Kernel Hackers						
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Acknowlegement	I would like to thank the following people for their time, feedback, and ideas: Scott Tsai, Bruce Hoult, Michael Clark, Benjamin Scherrey and Po-wei Huang						