Seminar 7

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Topic 1

1. Topic

In this topic, we are required to compare the hard-switching with ZVS QRC (zero-voltage-switching quasi-resonant converter) on a typical buck converter.

To be more specific, for hard-switching Buck converter, we need:

1) Observe the switching waveform of power switch Q
2) Plot loss curve

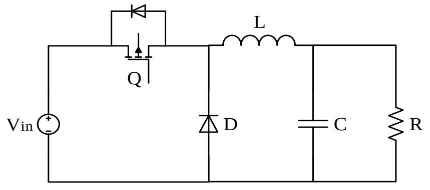


Fig.1 Hard-Switching Buck Converter

For ZVS QRC Buck converter:

1) Observe the switching waveform of power switch Q
2) Plot loss curve and compare with previous case

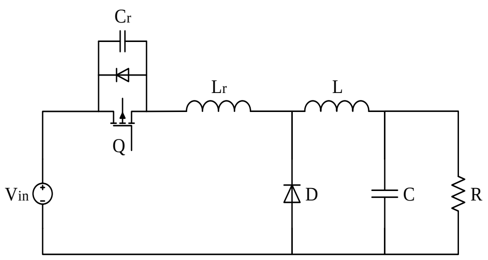


Fig.2 ZVS QRC Buck Converter

2. Simulation Model

2.1 Hard-Switching Buck Converter

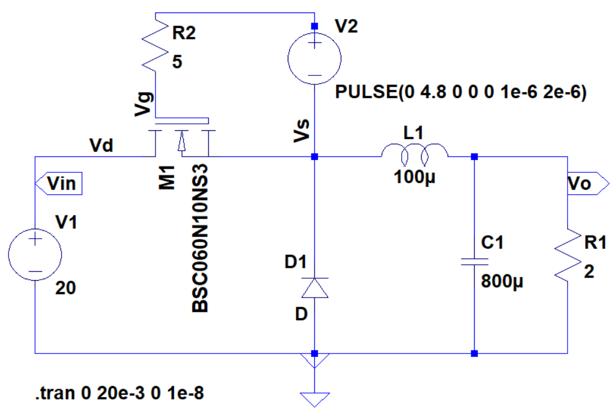


Fig.3 Hard-Switching Buck Converter Simulation Model

For hard-switching Buck converter, we built up the model above to carry out the simulations.

2.2 ZVS QRC Buck Converter

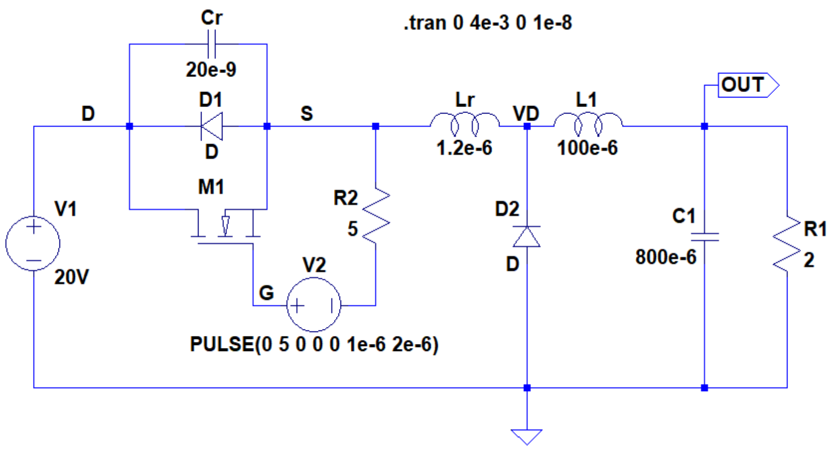


Fig.4 ZVS QRC Buck Converter Simulation Model

For ZVS QRC Buck converter, we added an extra parallel resonant capacitance, an anti-parallel diode, and a series resonant inductor.

3. Parameter Setup

3.1 Major Parameter

L	C	L_r	C_r	R	D	f_s	V_{in}
$100uH$	$800uF$	$1.2uH$	$20nF$	2Ω	0.5	$500kHz$	$20V$

3.2 Device Parameter

Switching Device	Switch Type	Vgs
BSC060N10NS3	NMOS	4.8V 5V

For our group, we are required to use BSC060N10NS3 as our switching device. It is a NMOSFET, which means it can be conducted only when the gate-to-source voltage is larger than the threshold voltage.

Therefore, we need to assign an appropriate value for the magnitude of gate-source voltage. If the gate voltage is too large, it may cause extra power loss. If the gate voltage is too small, it may not reach the minimum threshold voltage for the switch to work properly.

3 Electrical characteristics
at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.0	2.7	3.5	V	V_{DS}=V_{GS}, I_D=90 μA
Zero gate voltage drain current	I_{DSS}	- -	0.01 10	1.0 100	μA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1.0	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	5.3 6.6	6.0 11.5	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=6 V, I_D=25 A
Gate resistance	R_G	-	1.6	-	Ω	-
Transconductance	g_{fs}	43	85	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A

Fig.5 Static Characteristics of BSC060N10NS3

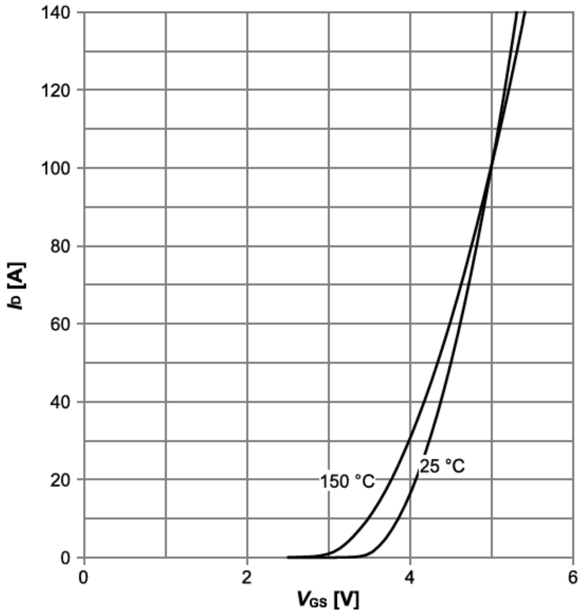


Fig.6 Transfer Characteristic Plot of BSC060N10NS3

From Figure 5, we can see that the maximum gate threshold voltage for this device is 3.5V. Plus Fig 6, we finally assigned 4.8V for the hard-switching converter and 5V for ZVS QRC. We set the value of the resistor between gate and source terminal to be 5 ohm so that the charging and discharging period of the switch can be faster, and the Miller Plateau can be somewhat avoided.

4. Simulation Results of Hard-Switching Buck Converter

4.1 Theoretical Analysis

The Buck Converter is selected as the main circuit for this topic, which is commonly used for DC chopping by controlling the duty cycle D of the switching device to change the magnitude of output voltage U_o. The theoretical relationship is pretty simple:

$$U_o = \frac{t_{on}}{T}E = DE = 10V$$

$$I = \frac{U_o}{R} = 5A$$

However, the formula above is acquired under the circumstance that power switching loss is totally neglected, and everything else is ideal. In practical, the performance of this circuit can be seriously impacted, especially by the switching loss, which can be shown in Fig 7.

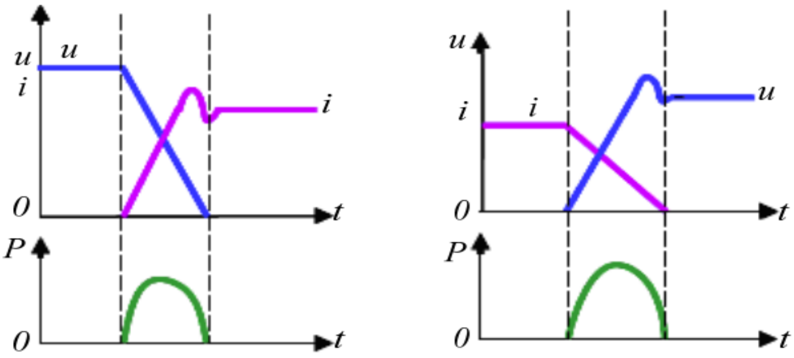


Fig.7 The Waveform of the Switching Process for Hard-Switching

4.2 Switching Waveform

Before we start, we need to first assure an appropriate measurement range when the circuit has been on the steady state.

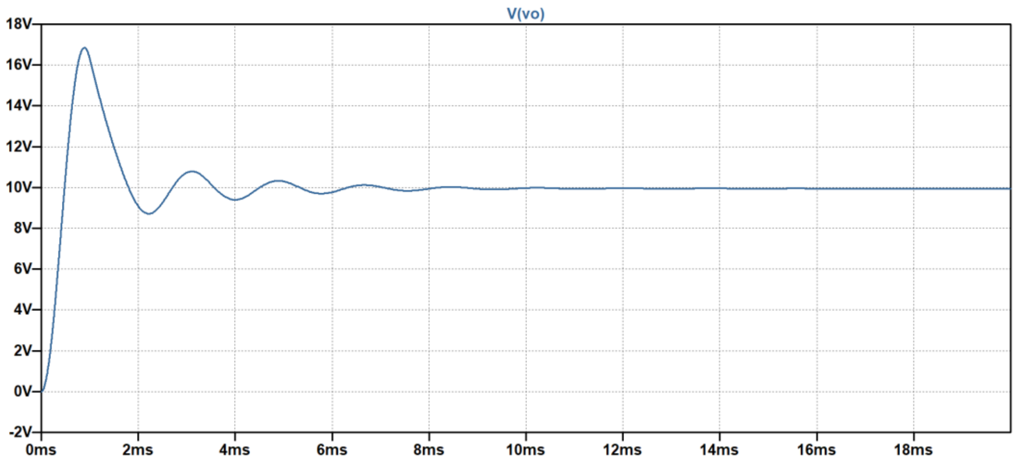


Fig.8 The Waveform of the Output Voltage

As shown in Fig 8, the output voltage has first experienced a transient oscillating period, then become steady around 10V after 18ms.

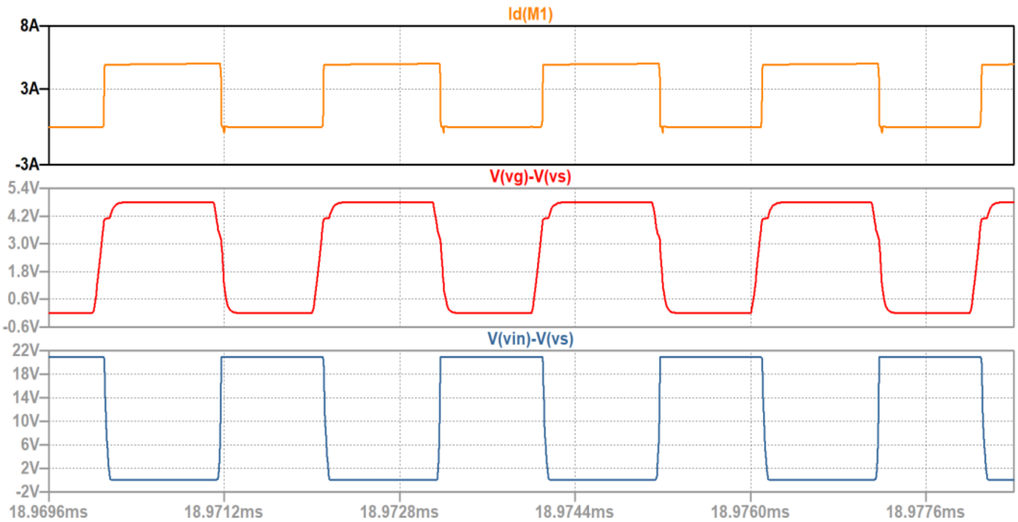


Fig.9 The Waveform of the Switch Current, Gate voltage and Switch Voltage

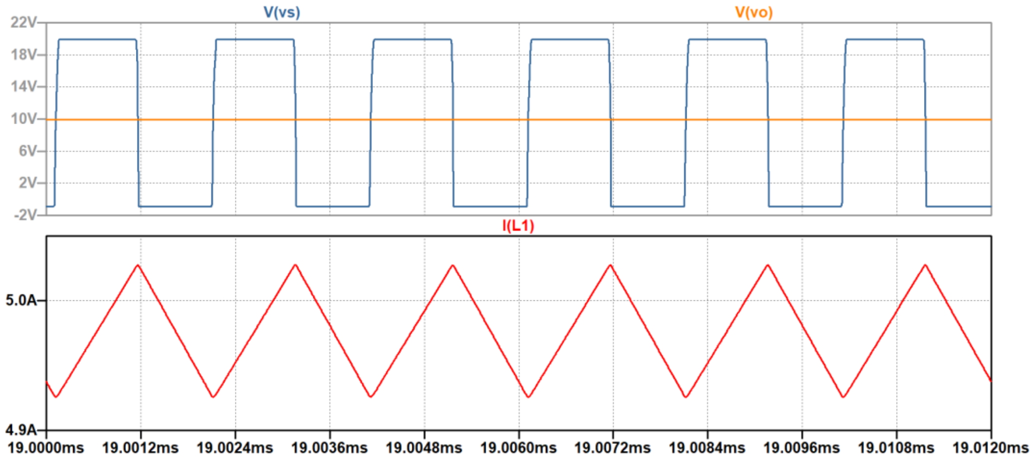


Fig.10 The Waveform of the Switch Voltage (blue), Output Voltage (orange) and the Inductor Current (red)

4.3 Loss Curve

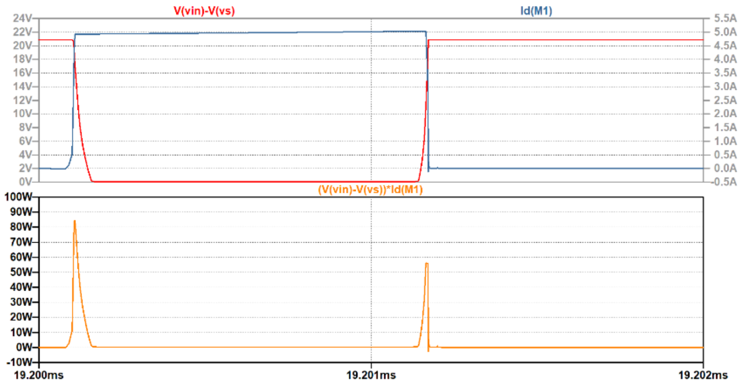


Fig.11 The Switching voltage, switching current and switching loss curve within one period

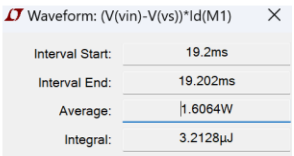


Fig.12 Switching power loss

As what has been shown in Fig 11, we can see that there are overlaps areas for the switching voltage and current resulting in the switching power loss.

The followings are the waveforms of the switching voltage, current and the power loss for the turning-on, on-state, turning-off and off-state periods.

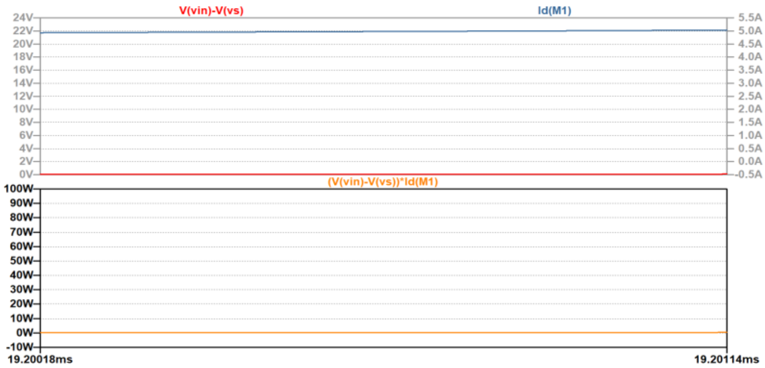


Fig.13 The Switching voltage, switching current and switching loss curve for on state

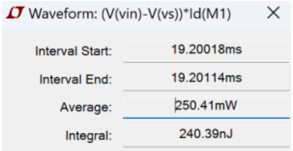


Fig.14 Switching Power Loss for On-State

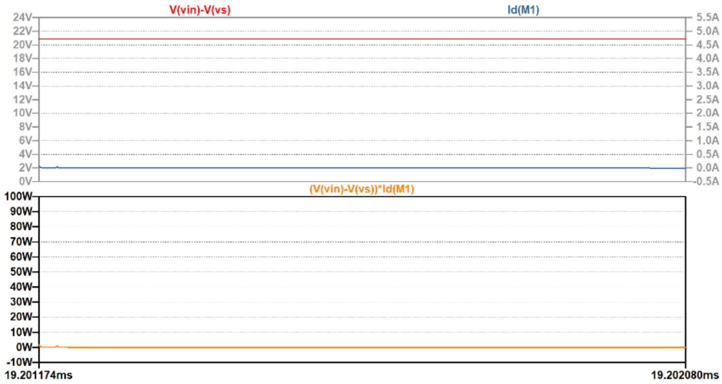


Fig.15 The Switching voltage, switching current and switching loss curve for off state

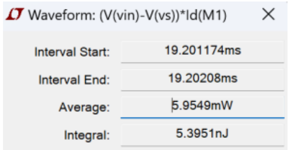


Fig.16 Switching Power Loss for Off-State

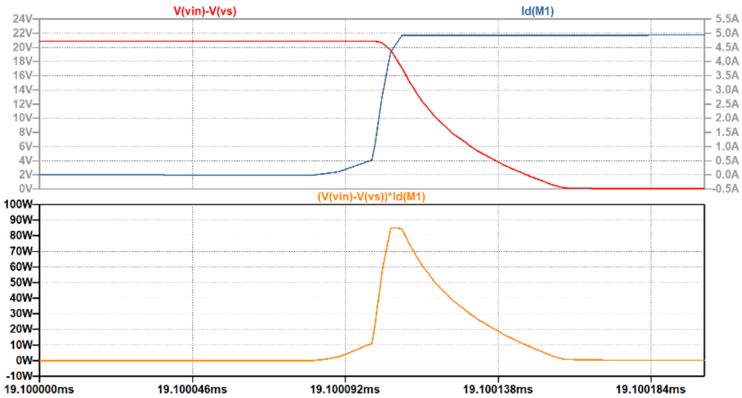


Fig.17 The Switching voltage, switching current and switching loss curve for Turning On

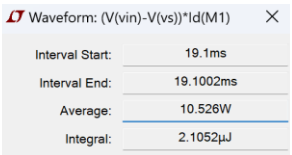


Fig.18 Switching Power Loss for Turning-On

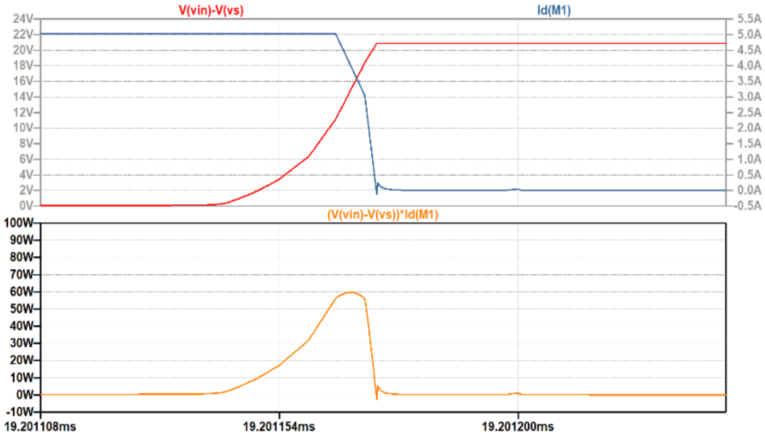


Fig.19 The Switching voltage, switching current and switching loss curve for Turning Off

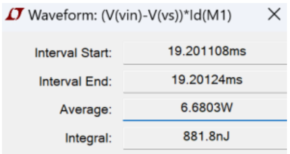


Fig.20 Switching Power Loss for Turning-Off

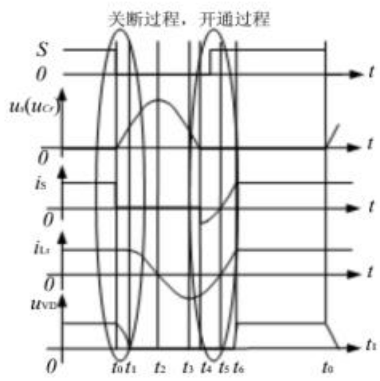
	On stage loss	Off stage loss	Turn on loss	Turn off loss	Total loss
Average	250.41mW	5.9549mW	10.526W	6.6803W	1606.4mW
Integral	240.39nJ	5.3951nJ	2105.2nJ	881.8nJ	3212.8nJ

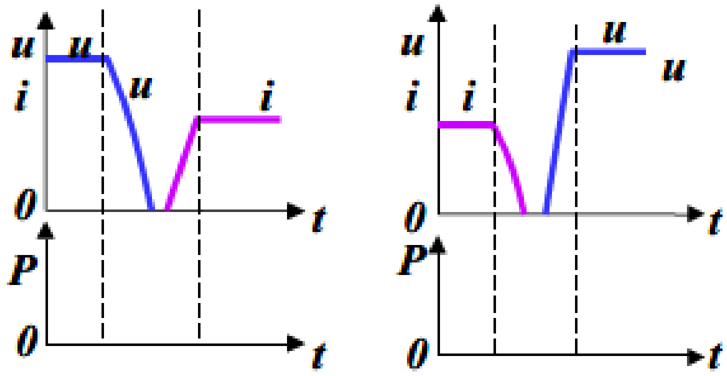
As shown in the table, we can see that most of the power loss is dissipated on the turning-on state and the turning-off state.

5. Simulation Results of ZVS QRC Buck Converter

5.1 Theoretical Analysis

It is known that the ZVS QRC, compared with the hard-switching circuit, has extra resonant inductance L_r and resonant capacitance C_r, whose values are much smaller. Another difference is an extra anti-parallel diode VD_S across the switch. When S is off, resonance occurs between L_r and C_r and the waveforms of voltage and current in the circuit are more like sinusoidal half-waves. This resonance decreases the slope of the switching voltage and current, and the overlap area during the turning-on and turning-off state can be avoided. Consequently, the switching power loss can be greatly reduced.





a) Turn-off process b) Turn-on process

Fig.21 Theoretical Switching Waveform for ZVS QRC

t0 ~ t1: Before t0, switch S is on, diode VD is off, $U_{Cr} = 0$, $I_{Lr} = I_L$. When S is turned off at t0, Cr slows down the increment of the voltage after S is turned off, so the turn-off loss of S is reduced. After S is turned off, VD is not on, and the circuit can be equivalent to Figure 22 a. The inductor Lr +L charges C. Since L is large, it can be equivalent to a current source. At the same time, the voltage at both ends of VD gradually decreases until t1, U_{VD}=0, VD is on. The growth rate of U_{Cr} during this period can be expressed by the following formula.

$$\frac{du_{C_r}}{dt} = \frac{I_L}{C_r}$$

t1 ~ t2: At t1, diode VD is on, inductor L continues to flow through VD, Cr, Lr, U_i form a resonant loop. During the resonance process, Lr charges Cr, U_{Cr} continues to rise, I_{Lr} continues to fall, until the moment t2, I_{Lr} drops to zero, U_{Cr} reaches the resonance peak.

a) $t_0{\sim}t_1$ b) $t_1{\sim}t_2$

Fig.22 ZVS QRC equivalent circuit

t2 ~ t3: After t2, Cr discharges to Lr, the polarity of the I_{Lr} is changed, and U_{Cr} continues to decline until t3, U_{Cr}=U_i, at which time, U_{Lr}=0, reaching the reverse resonance peak.

t3 ~ t4: After t3, Lr reversely charges Cr, and U_{Cr} continues to decline until U_{Cr}=0 at t4.

The equation of the circuit resonance process from t1 to t4 is:

$$\begin{cases} L_r\dfrac{di_{Lr}}{dt} + u_{C_r} = U_i \\ C_r\dfrac{du_{C_r}}{dt} = i_{Lr} \\ u_{Cr}|_{t=t1} = U_i\text{，}\ \ i_{Lr}|_{t=t1} = I_L\ \ t \in [t_1\text{，}\ t_4] \end{cases}$$

t4 ~ t5: U_{Cr} is at zero, U_{Lr}=U_i, and I_{Lr} decays linearly until time t5, I_{Lr}=0. Since the voltage at both ends of the switch S during this period is 0, S must be turned on during this period to avoid opening loss.

t5 ~ t6: S is in the on-state and I_{Lr} rises linearly until t6, when I_{Lr}=I_L and VD are turned off. The current I_{Lr} change rate from t1 to t6 is

$$\frac{di_{L_r}}{dt} = \frac{U_i}{L_r}$$

t6 ~ t0: S is on, and VD is off.

5.2 Switching Waveform

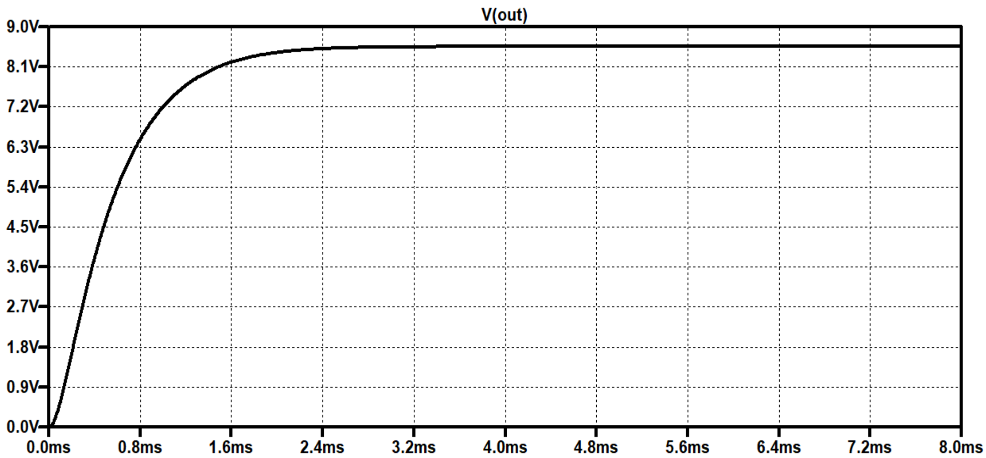


Fig.23 Output Voltage of ZVS QRC

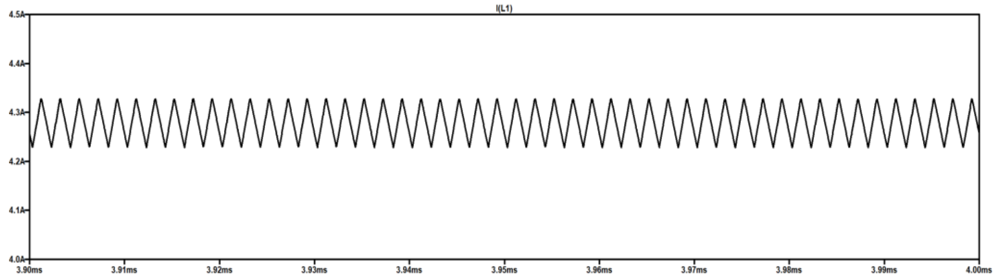
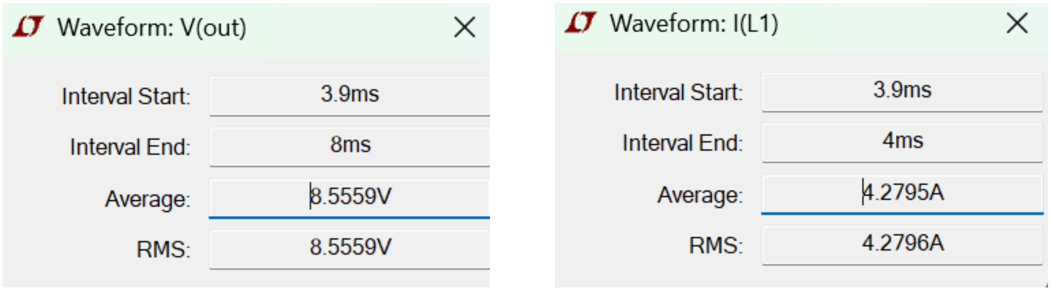


Fig.24 Waveform of the Load Inductor Current



Output voltage

Inductor current

Fig.25 Average Value of the Output Voltage and Inductor Current

From Fig23, we can see that the oscillating process is greatly weaken for the ZVS QRC compared with the Hard-Switching Converter, and the transient period is also shortened correspondingly. In the following part, we choose one switching cycle from 3.9ms to analyze.

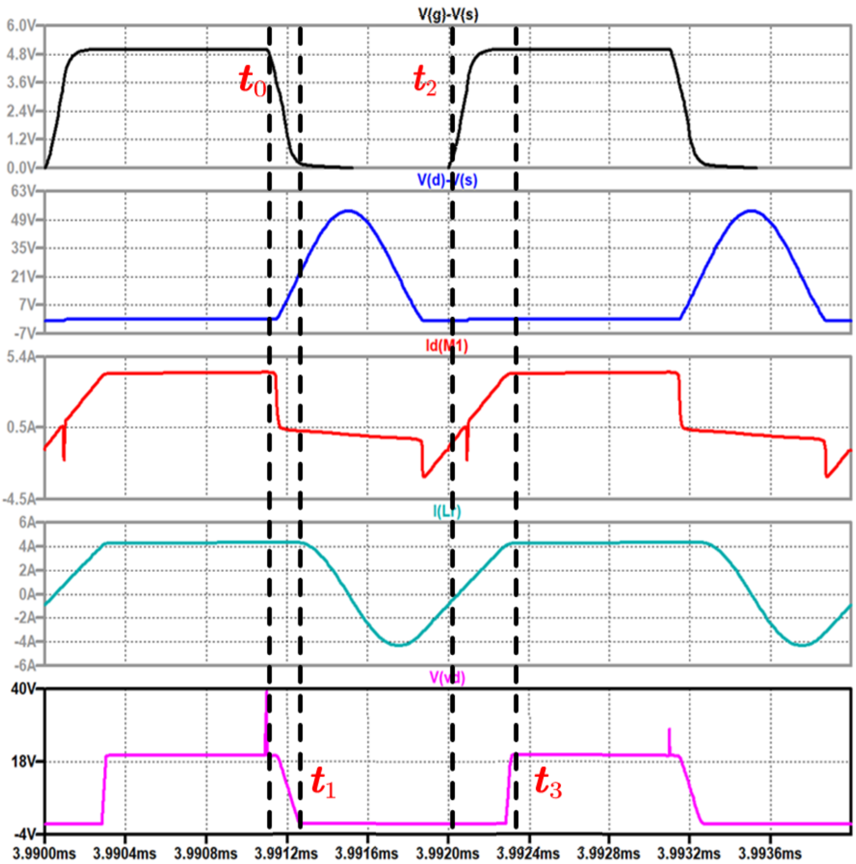


Fig.26 Switching Waveform of ZVS QRC

The plot above shows the waveform of gate voltage, switch voltage, switch current, load inductor current and the voltage between the diode in the Buck converter.

For the existence of the Miller Capacitance in the NMOSFET, the waveform of the gate voltage is not ideal compared to the theoretical waveform. Therefore, we defined the point when the gate voltage begins to drop from 5V as t_0, the point when the diode voltage reaches zero as t_1, the point when the gate voltage begins to rise as t_2, the point when the diode voltage reaches maximum as t_3.

$t_0 \sim t_1$: Turning-Off State; $t_1 \sim t_2$: Off State; $t_2 \sim t_3$: Turning-On State; $t_2 \sim t_0 + T$: On State.

5.3 Loss Curve

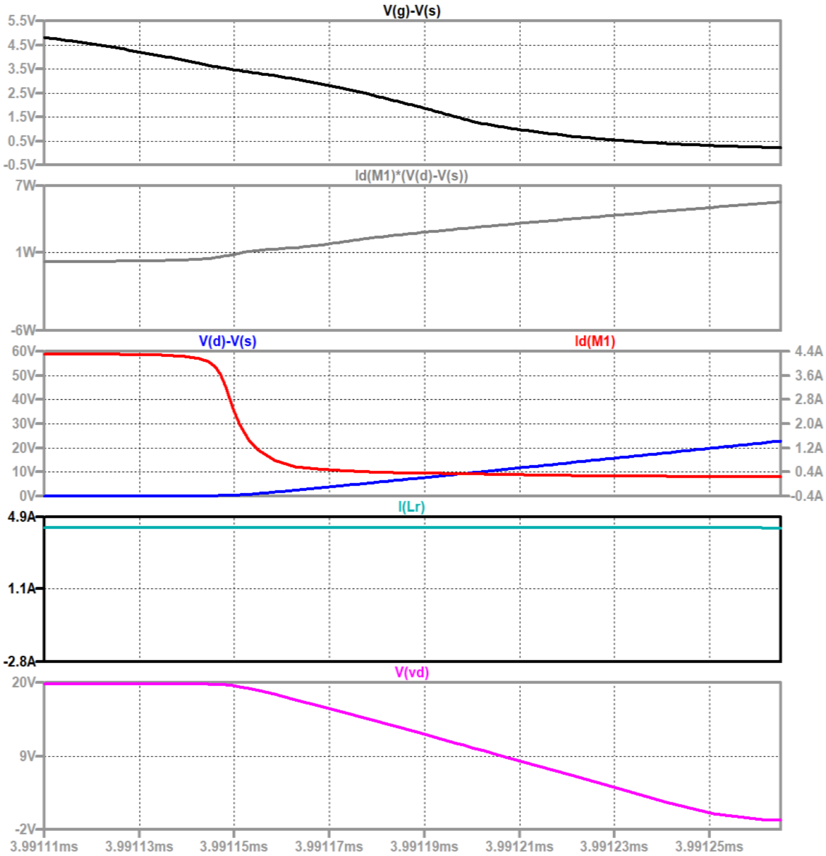


Fig.27 Turning-Off State Switching Waveform of ZVS QRC

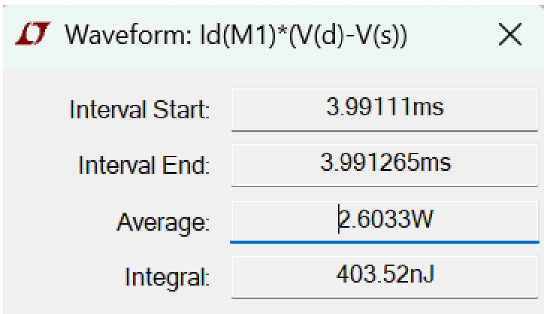


Fig.28 Turning-Off State Switching Power Loss

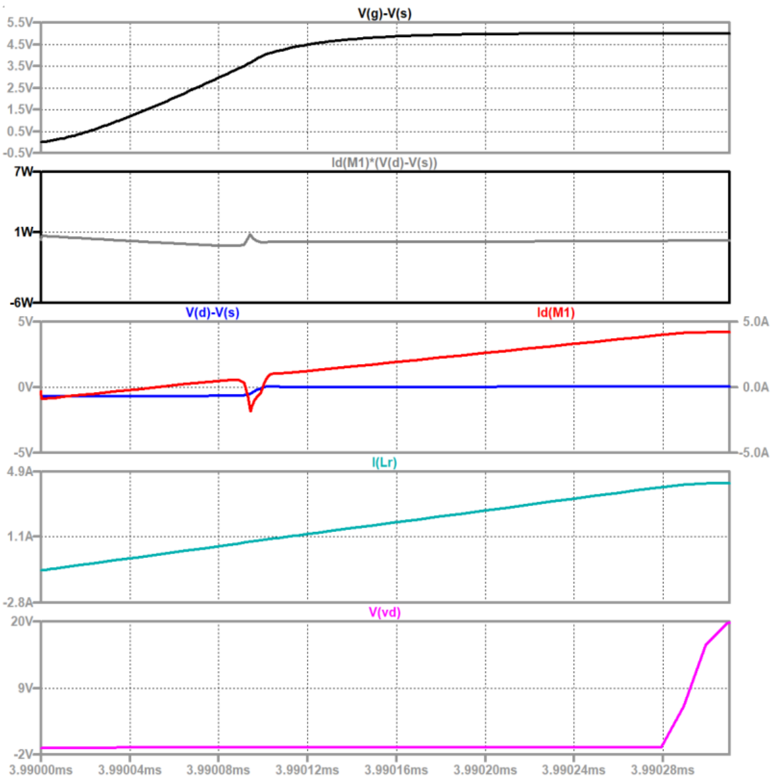


Fig.29 Turning-On State Switching Waveform of ZVS QRC

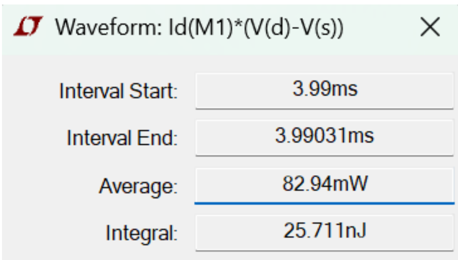


Fig.30 Turning-On Switching Power Loss

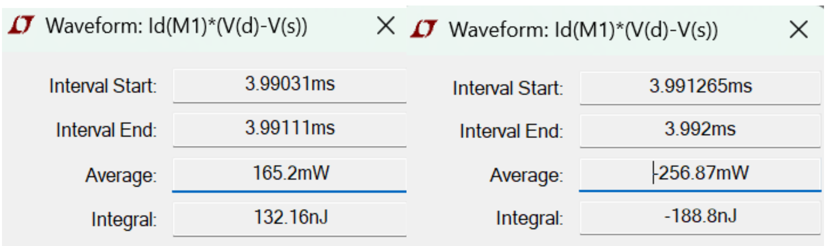


Fig.31 On-State (L) and Off-State (R) Switching Power Loss

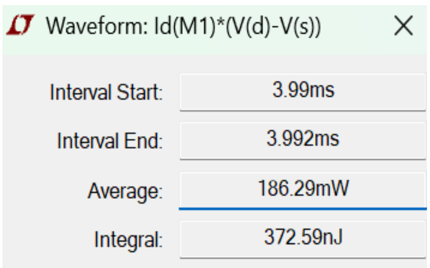


Fig.30 Switching Power Loss within one period

Among them, the reason for the negative off-state loss is that when the resonance peak is reached, the current flowing through the MOSFET is just zero, and then C_r is discharged to L_r, and $i_{L_r}$and $i_s$are reversed. At this time, the MOSFET is under positive voltage, and the flow current is negative, resulting in the entire process of the off-state loss is negative.

Because the MOSFET is switched on before opening, the positive guide voltage drop is very small, so the opening loss is also very small, the average power is in the mW level, and the switching voltage rises from 0 to about 20V during the shutdown process, the range is large, and the current changes are large, so the shutdown loss is very large.

	On stage loss	Off stage loss	Turn on loss	Turn off loss	Total loss
Average	165.2mW	-256.87mW	82.94mW	2.6033W	186.29mW
Integral	132.16nJ	-188.8nJ	25.711nJ	403.52nJ	372.59nJ

6. Analysis of the Results

The four stages and total loss of the two circuits are compared in the following table. There is little difference between on-state loss and off-state loss of soft and hard switches. The on-off loss of the soft switch is greatly reduced compared with that of the hard switch, so the total loss is also reduced.

	On stage loss	Off stage loss	Turn on loss	Turn off loss	Total loss
Average for Hard-Switching	250.41mW	5.9549mW	10.526W	6.6803W	1606.4mW
Integral for Hard -Switching	240.39nJ	5.3951nJ	2105.2nJ	881.8nJ	3212.8nJ
Average for AVS QRC	165.2mW	-256.87mW	82.94mW	2.6033W	186.29mW
Integral for ZVS QRC	132.16nJ	-188.8nJ	25.711nJ	403.52nJ	372.59nJ