Cache

Exercise 2

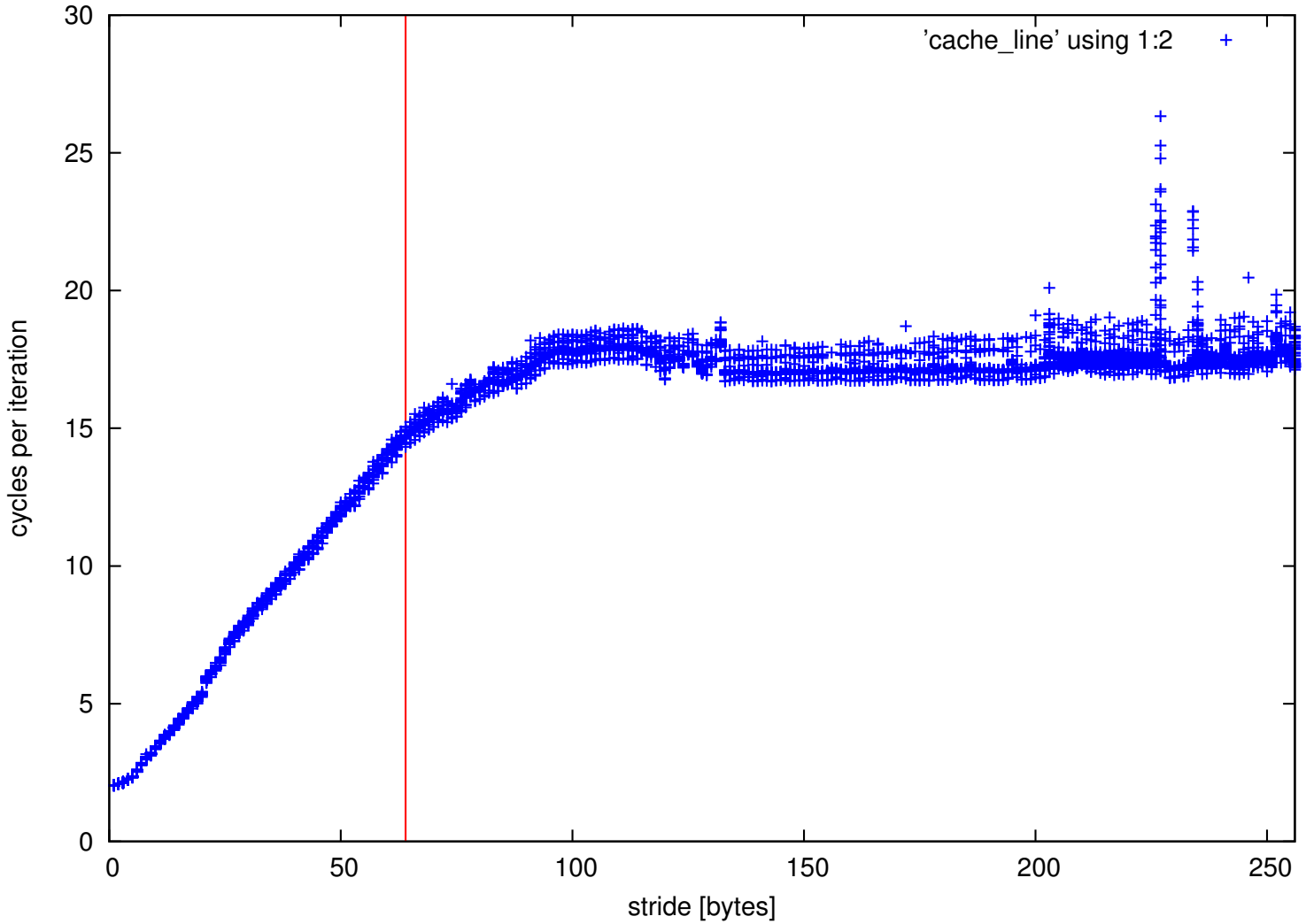
6c8e27db312c23968fc6c6f7bb20dea0

January 11, 2016

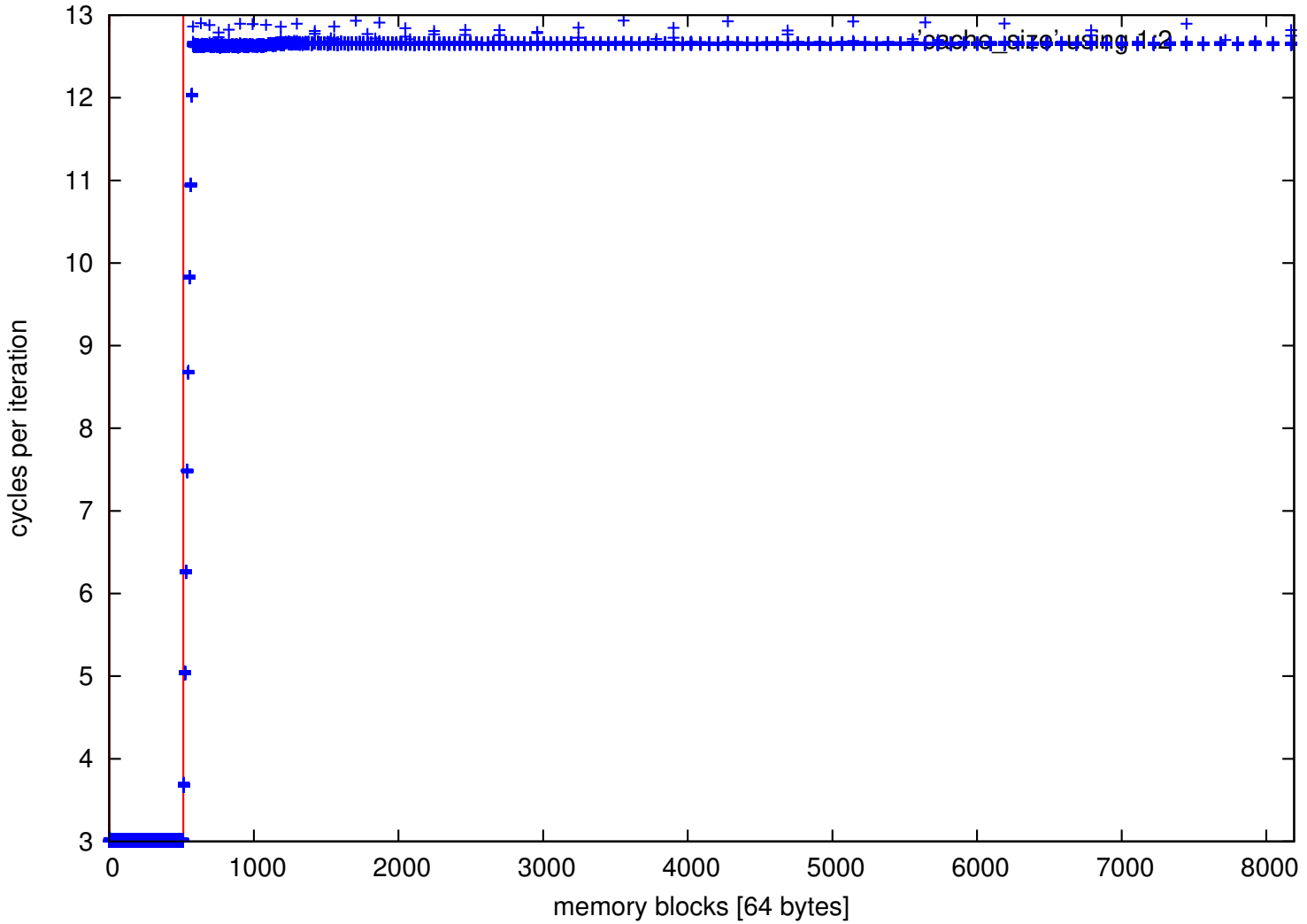
cache_flush

```
static inline void flush_cache(volatile void *ptr,
    size_t len){
for(size_t i = 0; i < len; i++, ptr++)
asm volatile ("clflush (%0)" : : "r"(ptr));
}
```

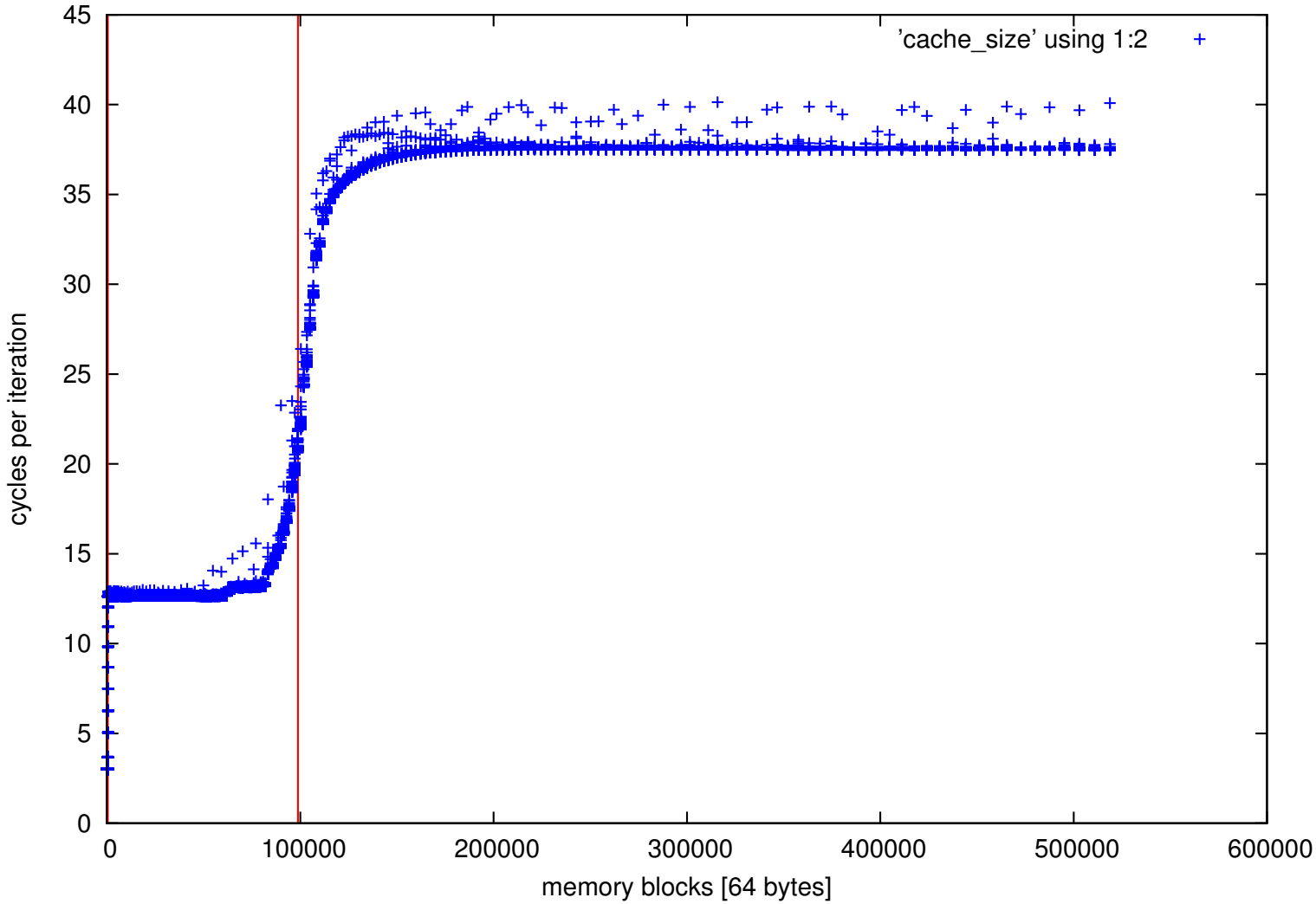
Cache Line Length: C2D t9400



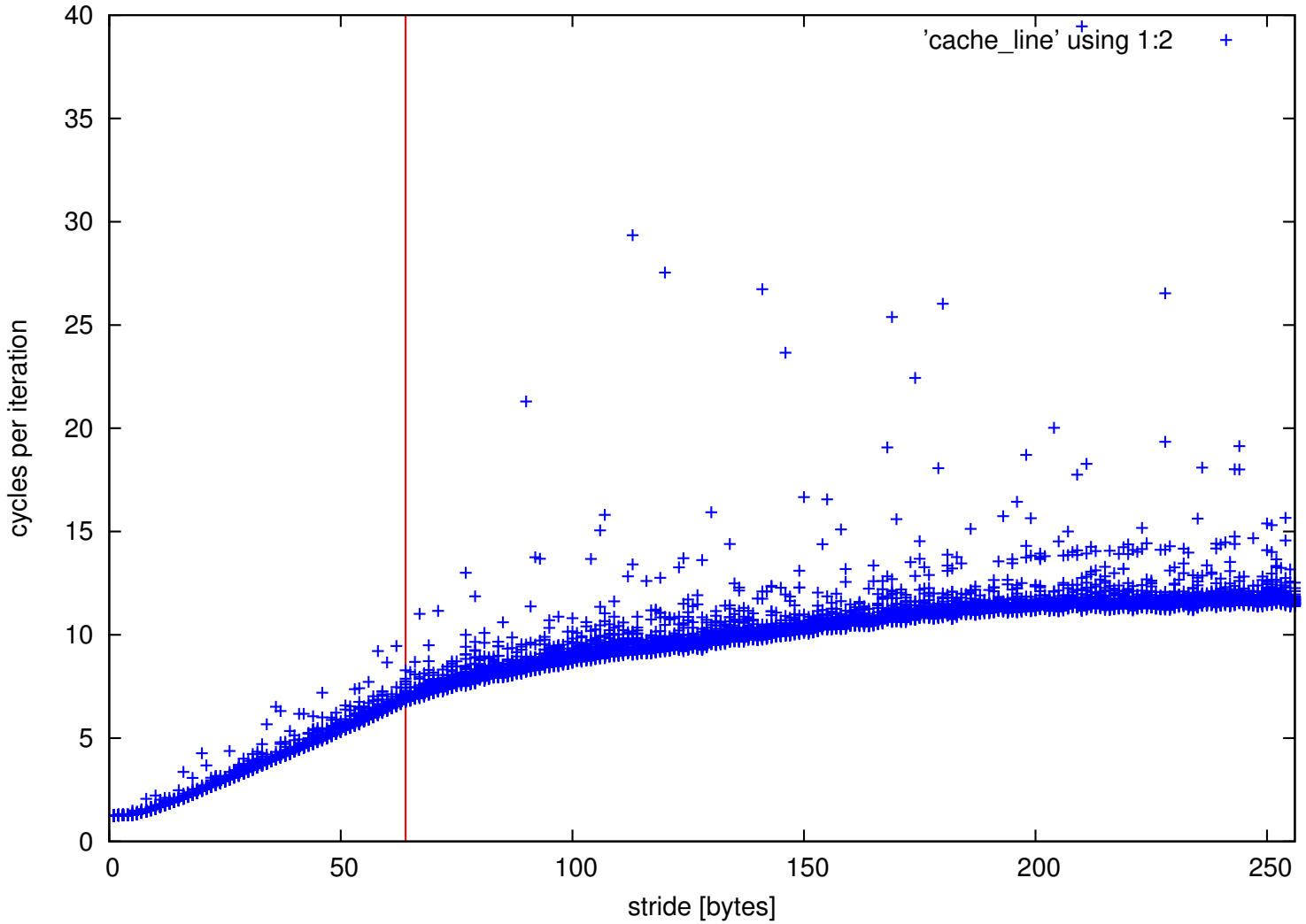
Cache Size Small: C2D t9400



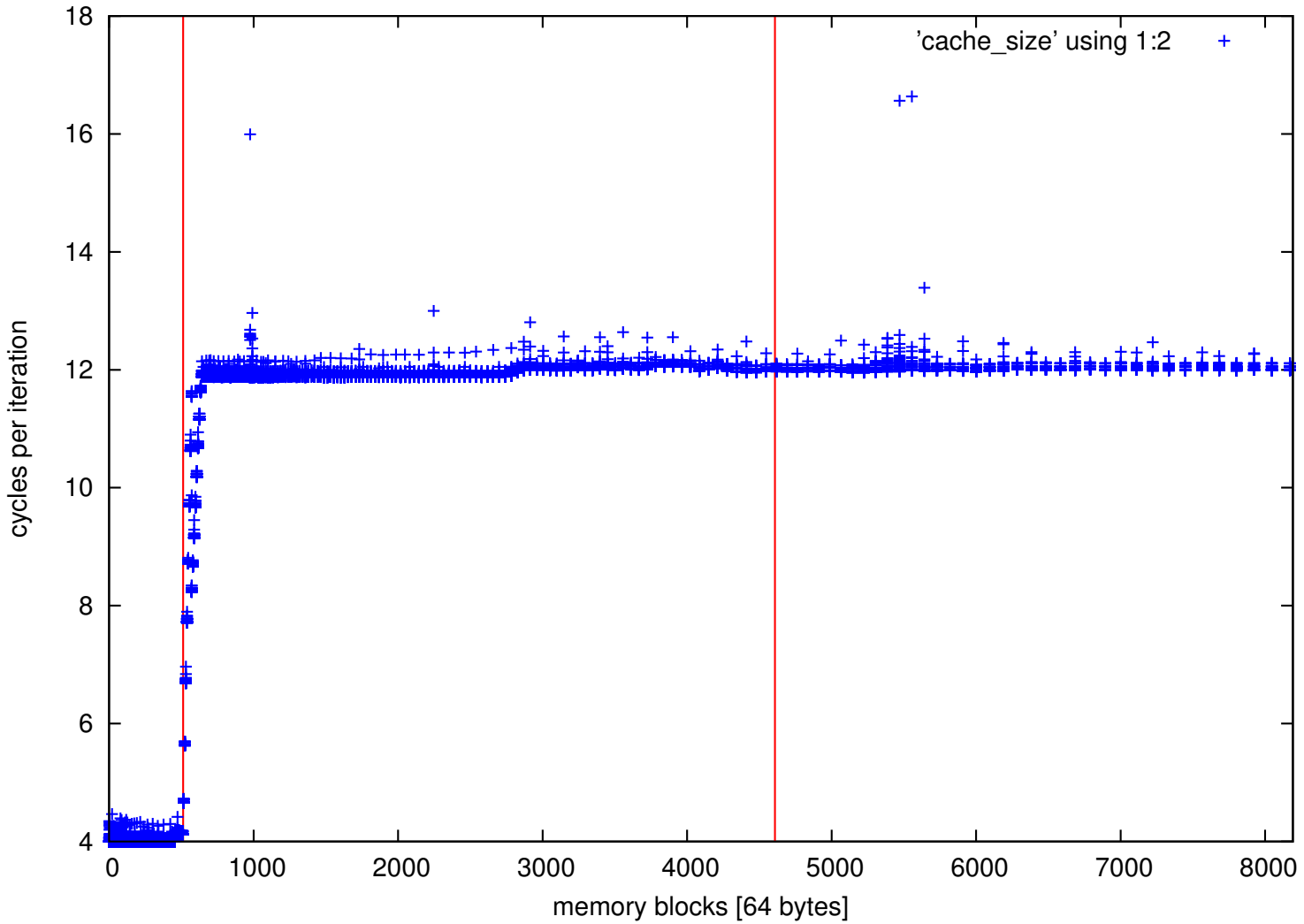
Cache Size: C2D t9400



Cache Line Length: Xeon e3 1230v3



Cache Size Small: Xeon e3 1230v3



Cache Size: Xeon e3 1230v3