Digital IC Design

Exercise 2
Supplement

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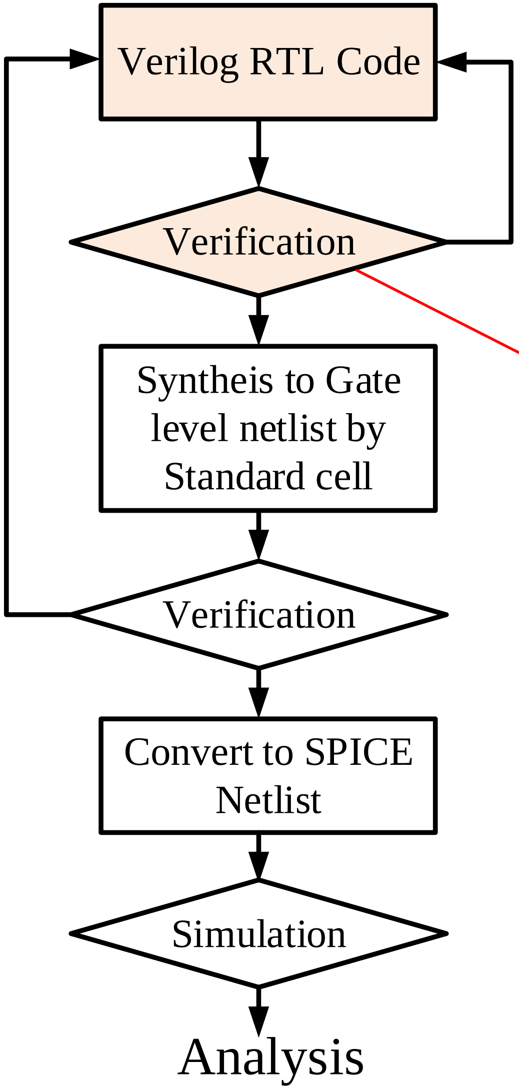
Construct a 4-bit Adder by verilog



Verilog RTL Code

Verification

Syntheis to Gate level netlist by Standard cell

Verification

Convert to SPICE Netlist

Simulation

Analysis

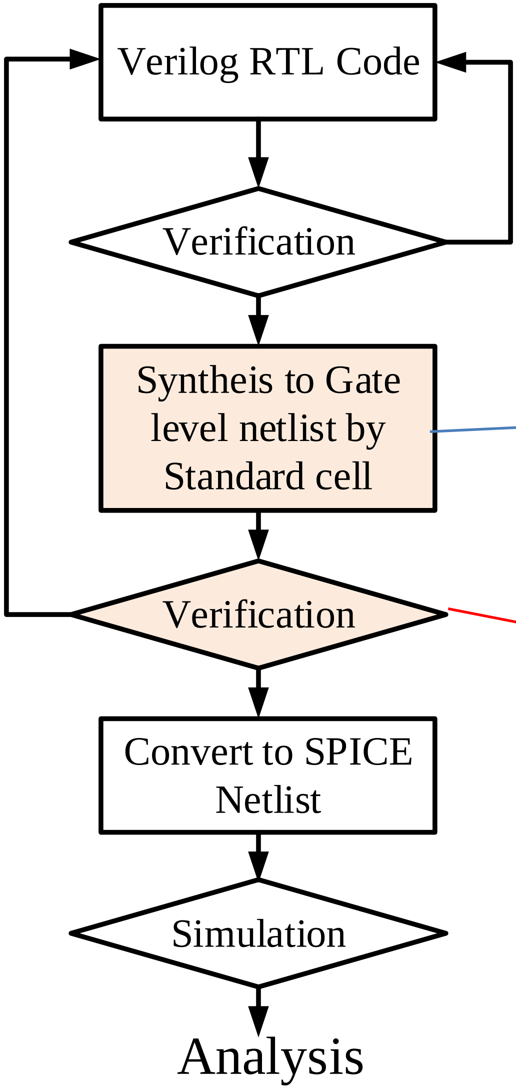
- In this exercise, TA will provide a RTL code of 4-bit adder.
- Verify the behavior.
  - ➢ Write a Testbnech to check.
    (or used the Testbench provided by TA)

Verify in Behavior level:

Command:

```
irun TESTBED_Adder_4bit.v  -define RTL -debug  -notimingchecks -loadpli1 debpli:novas_pli_boot
```

Synthesis



- Synthesis the 4-bit adder.
- Verify 4-bit adder in the gate level.

Synthesis: (covert to gate level)

Command: *dc_shell-t -f syn.tcl | tee syn.log*

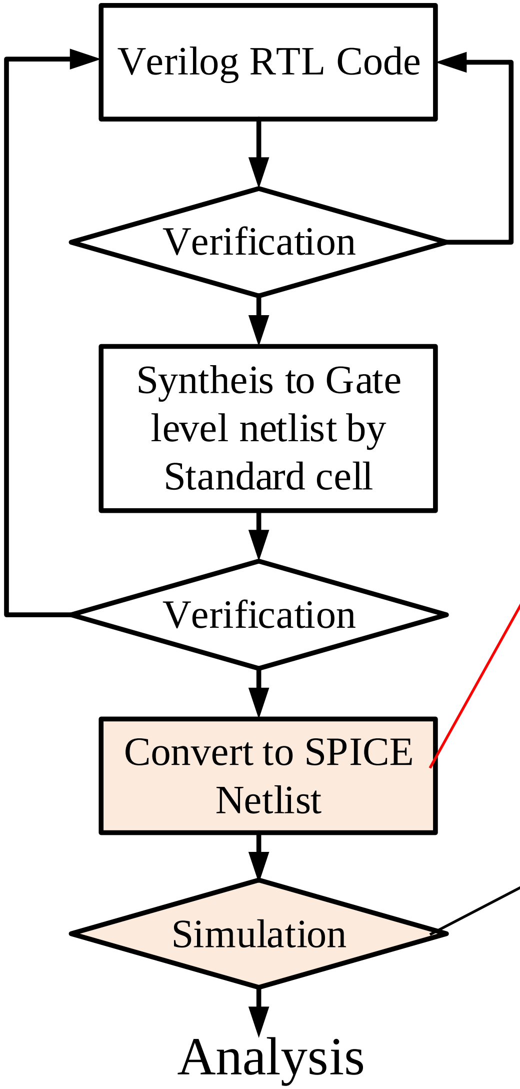
(Used the .tcl provided by TA and modify the path in .tcl)

Verify in Gate level:

Commandirun *irun TESTBED_Adder_4bit.v -define GATE -debug -v /path of NLDM/NLDM/Verilog/asap7sc7p5t_SIMPLE_RVT_TT_08302018.v /path of NLDM/NLDM/Verilog/asap7sc7p5t_SEQ_RVT_TT_08302018.v /path of NLDM/NLDM/Verilog/asap7sc7p5t_INVBUF_RVT_TT_08302018.v -nontcglitch*

Convert to SPICE Netlist

- Convert the gate level 4-bit adder to spice.
- Measure the delay & power of 4-bit adder by Hspice.



Convert to SPICE Netlist:

Step1. convert .v to .sp → command: *./Verilog2Spice*

Strp2. add the VSS & VDD pin → command: *python3.8 pin_adder_VSS_VDD.py*

You need to generate the input Vector file for HSPICE simulation

```
**** Input Vector ****
.VEC 'pattern_adder_4bit.vec‘

**** include the Adder****
.include ‘Adder_4bit_SYN_new.sp'
```

.sp is the SPICE netlist you converted above