DIC HW5

312510190 張家瑋

PART1: Implement a 3x3 convolution kernel without clock gating.

```
add_0_root_add_0_root_add_165_8/U1_17/CON (FAX1_ASAP7_75t_R)
                                                  20.30     916.17 r
add_0_root_add_0_root_add_165_8/U5/Y (INVx1_ASAP7_75t_R)
                                                  15.59     931.76 f
add_0_root_add_0_root_add_165_8/U4/Y (XOR2xp5_ASAP7_75t_R)
                                                  20.20     951.97 f
add_0_root_add_0_root_add_165_8/SUM[18] (Convolution_DW01_add_0)
                                                   0.00     951.97 f
U789/Y (AND2x2_ASAP7_75t_R)                       18.94     970.91 f
U604/Y (NOR2xp33_ASAP7_75t_R)                     12.90     983.81 r
ans_reg_18_/D (DFFHQNx1_ASAP7_75t_R)               0.00     983.81 r
data arrival time                                           983.81

clock clk (rise edge)                           1000.00    1000.00
clock network delay (ideal)                        0.00    1000.00
ans_reg_18_/CLK (DFFHQNx1_ASAP7_75t_R)             0.00    1000.00 r
library setup time                               -14.79     985.21
data required time                                          985.21
-----------------------------------------------------------------------------
data required time                                          985.21
data arrival time                                          -983.81
-----------------------------------------------------------------------------
slack (MET)                                                   1.40


exit
```

實現 convolution without clock gating, clock period 滿足設定之 1000ps

```
Number of ports:                          830
Number of nets:                          4093
Number of cells:                         2921
Number of combinational cells:           2716
Number of sequential cells:               190
Number of macros/black boxes:               0
Number of buf/inv:                        574
Number of references:                      30

Combinational area:               3885.978221
Buf/Inv area:                      406.840325
Noncombinational area:             923.788770
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  4809.766990
Total area:                 undefined
1
```

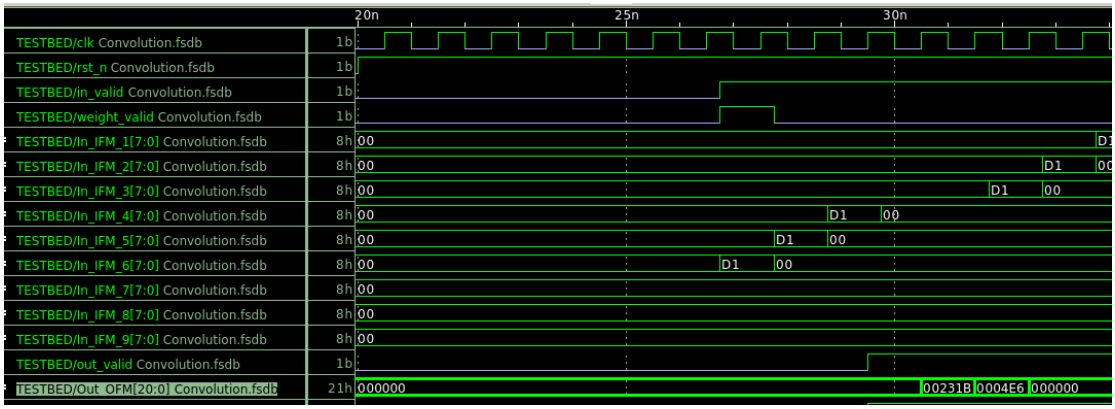
面積小於 5100um^2。

PART2: Use the pattern provided by TA to generate the waveform under gate-level simulation, and measure the power consumption of 3x3 convolution kernel using PrimePower

(1). Without using clock gating

```
  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network                0.0000    0.0000    0.0000    0.0000 ( 0.00%)
register                  2.046e-04 2.186e-06 4.732e-08 2.068e-04 (99.89%)  i
combinational             5.736e-10    0.0000 2.279e-07 2.285e-07 ( 0.11%)
sequential                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                    0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 2.186e-06   ( 1.06%)
  Cell Internal Power  = 2.046e-04   (98.81%)
  Cell Leakage Power   = 2.752e-07   ( 0.13%)
    Intrinsic Leakage  = 2.752e-07
    Gate Leakage       =    0.0000
                         ---------
Total Power            = 2.070e-04  (100.00%)

X Transition Power     =    0.0000
Glitching Power        =    0.0000

Peak Power             = 2.688e-04
Peak Time              =      1205

1
exitInformation: Defining new variable 'DESIGN'. (CMD-041)
Information: Defining new variable 'synthetic_library'. (CMD-041)
```

waveform:



根據 power report，dynamic power 佔了整體 99.8%左右，其中 Internal power 又佔了 dynamic power 的 90%以上，這代表整個電路主要的功耗來自於電晶體切換時 NMOS、PMOS 同時導通所造成的 Short circuit power。

Power consumption 的來源，又以 register 為大宗，combinational 則為其次。

PART3: Power reduction using a data-driven clock gating technique

```
113 ICGx3_ASAP7_75t_R GATED_1(
114         .CLK(clk),
115         .ENA(0),
116         .SE(Enable_1),
117         .GCLK(clk_gate_1)
118 );
```

```
102  assign Enable_1 = (In_IFM_1 == 0)? 0:1;
```

```
205 always @(posedge clk or negedge rst_n) begin
206     if(~rst_n) begin
207         Enable_3_t <= 0;
208     end
209     else if(Enable_3) begin
210         Enable_3_t <= 1;
211     end
212     else begin
213         Enable_3_t <= 0;
214     end
215 end
```

設置 CG 元件，由於 0 乘上任何數字都是 0，因此當 In_IFM 從一個不為零的數字變成 0 的時候，我們可以把 In_IFM_reg 的 clk 給關掉，相加的時候直接輸入 0，這樣可以有效減少 register 切換的次數進而節省 power。

```
Number of ports:                          830
Number of nets:                          4402
Number of cells:                         3231
Number of combinational cells:           3007
Number of sequential cells:               209
Number of macros/black boxes:               0
Number of buf/inv:                        577
Number of references:                      34

Combinational area:               4300.516785
Buf/Inv area:                      410.106245
Noncombinational area:            1225.419827
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  5525.936612
Total area:                 undefined
1
```

(2). Using clock gating

```
  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                     Internal  Switching  Leakage    Total
Power Group          Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network        4.837e-06 7.508e-06 4.084e-09 1.235e-05 (10.13%)
register             1.022e-04 2.976e-06 6.198e-08 1.053e-04 (86.39%)  i
combinational        1.765e-06 2.196e-06 2.699e-07 4.231e-06 ( 3.47%)
sequential              0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box               0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 1.268e-05   (10.41%)
  Cell Internal Power  = 1.088e-04   (89.32%)
  Cell Leakage Power   = 3.360e-07   ( 0.28%)
    Intrinsic Leakage  = 3.360e-07
    Gate Leakage       =    0.0000
                         ---------
Total Power            = 1.219e-04  (100.00%)

X Transition Power     = 3.751e-05
Glitching Power        =    0.0000

Peak Power             = 2.783e-04
Peak Time              =      1205

1
```

使用 CG 後的 power 降到 120uW。

PART4: Compare and analyze the area and critical path

	area	power
Without CG	4809um^2	207uW
With CG	5525um^2	122uW

使用 CG 後，雖然 area 增加約 14.8%，但 power 卻節省 41.1%，可發現 CG 確實大大增加功率效益。

根據公式$P_{internal\ power} = t_{sc} \cdot V_{dd} \cdot I_{peak} \cdot f_{clock}$，internal power 能降這麼多的原因主要是 tsc(NMOS PMOS 同時導通的時間)下降很多，也就是暗示 register 切換(0→1 or 1→0)的次數明顯減少。

Critical Path Without CG:

```
Operating Conditions: PVT_0P7V_25C   Library: asap7sc7p5t_INVBUF_RVT_TT_08302018
Wire Load Model Mode: top

  Startpoint: IFM_3_reg_1_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: ans_reg_18_
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                    Incr       Path
  -----------------------------------------------------------------------------
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  IFM_3_reg_1_/CLK (DFFHQNx1_ASAP7_75t_R)                  0.00       0.00 r
  IFM_3_reg_1_/QN (DFFHQNx1_ASAP7_75t_R)                  54.41      54.41 f
  mult_167_3/a[1] (Convolution_DW_mult_uns_6)              0.00      54.41 f
  mult_167_3/U233/Y (INVx1_ASAP7_75t_R)                   19.27      73.68 r
  mult_167_3/U248/Y (NOR2xp33_ASAP7_75t_R)                25.54      99.22 f
  mult_167_3/U146/CON (FAx1_ASAP7_75t_R)                  23.95     123.17 r
  mult_167_3/U241/Y (INVxp67_ASAP7_75t_R)                 18.77     141.94 f
  mult_167_3/U140/CON (FAx1_ASAP7_75t_R)                  28.38     170.32 r
  mult_167_3/U131/CON (FAx1_ASAP7_75t_R)                  23.88     194.21 f
  mult_167_3/U269/Y (INVx1_ASAP7_75t_R)                   16.31     210.51 r
  mult_167_3/U122/SN (FAx1_ASAP7_75t_R)                   47.44     257.95 r
  mult_167_3/U351/Y (XOR2xp5_ASAP7_75t_R)                 35.83     293.78 r
  mult_167_3/U244/Y (XOR2xp5_ASAP7_75t_R)                 35.37     329.15 r
  mult_167_3/product[6] (Convolution_DW_mult_uns_6)        0.00     329.15 r
  add_7_root_add_0_root_add_167_8/A[6] (Convolution_DW01_add_7)
                                                           0.00     329.15 r
  add_7_root_add_0_root_add_167_8/U1_6/SN (FAx1_ASAP7_75t_R)
                                                          40.04     369.19 r
  add_7_root_add_0_root_add_167_8/U21/Y (INVx1_ASAP7_75t_R)
                                                          17.88     387.07 f
  add_7_root_add_0_root_add_167_8/SUM[6] (Convolution_DW01_add_7)
                                                           0.00     387.07 f
```

根據 timing report，critical path 來自於 IFM_3_reg_1 到 ans_reg_18 的路徑，

Critical Path With CG:

```
Startpoint: Weight_3_reg_1_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: ans_reg_17_
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
Weight_3_reg_1_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)          0.00       0.00 r
Weight_3_reg_1_/QN (ASYNC_DFFHx1_ASAP7_75t_R)          45.51      45.51 f
U865/Y (BUFx2_ASAP7_75t_R)                             26.01      71.52 f
mult_447/b[1] (Convolution_DW_mult_uns_5)               0.00      71.52 f
mult_447/U398/Y (NAND2xp33_ASAP7_75t_R)                24.90      96.42 r
mult_447/U395/Y (XOR2xp5_ASAP7_75t_R)                  38.15     134.57 r
mult_447/U140/SN (FAx1_ASAP7_75t_R)                    55.65     190.22 r
mult_447/U340/Y (XOR2xp5_ASAP7_75t_R)                  36.37     226.59 r
mult_447/U299/Y (XOR2xp5_ASAP7_75t_R)                  24.70     251.28 r
mult_447/product[4] (Convolution_DW_mult_uns_5)         0.00     251.28 r
U639/Y (AND2x2_ASAP7_75t_R)                            22.86     274.14 r
add_7_root_add_0_root_add_519_8/A[4] (Convolution_DW01_add_7)
                                                        0.00     274.14 r
add_7_root_add_0_root_add_519_8/U1_4/SN (FAx1_ASAP7_75t_R)
                                                       38.33     312.47 f
add_7_root_add_0_root_add_519_8/U22/Y (INVx1_ASAP7_75t_R)
                                                       17.30     329.77 r
add_7_root_add_0_root_add_519_8/SUM[4] (Convolution_DW01_add_7)
                                                        0.00     329.77 r
add_3_root_add_0_root_add_519_8/B[4] (Convolution_DW01_add_5)
```

```
                                                                 [illegible]
add_0_root_add_0_root_add_519_8/U10/Y (INVx1_ASAP7_75t_R)
                                                       15.27     797.02 f
add_0_root_add_0_root_add_519_8/U1_14/CON (FAx1_ASAP7_75t_R)
                                                       20.30     817.31 r
add_0_root_add_0_root_add_519_8/U9/Y (INVx1_ASAP7_75t_R)
                                                       15.27     832.58 f
add_0_root_add_0_root_add_519_8/U1_15/CON (FAx1_ASAP7_75t_R)
                                                       20.30     852.88 r
add_0_root_add_0_root_add_519_8/U8/Y (INVx1_ASAP7_75t_R)
                                                       15.27     868.15 f
add_0_root_add_0_root_add_519_8/U1_16/CON (FAx1_ASAP7_75t_R)
                                                       20.30     888.44 r
add_0_root_add_0_root_add_519_8/U7/Y (INVx1_ASAP7_75t_R)
                                                       15.27     903.71 f
add_0_root_add_0_root_add_519_8/U1_17/SN (FAx1_ASAP7_75t_R)
                                                       32.19     935.91 r
add_0_root_add_0_root_add_519_8/U4/Y (INVxp67_ASAP7_75t_R)
                                                       10.92     946.83 f
add_0_root_add_0_root_add_519_8/SUM[17] (Convolution_DW01_add_0)
                                                        0.00     946.83 f
U77/Y (NAND2xp5_ASAP7_75t_R)                           10.32     957.14 r
U76/Y (AND2x2_ASAP7_75t_R)                             21.59     978.73 r
ans_reg_17_/D (DFFHQNx1_ASAP7_75t_R)                    0.00     978.73 r
data arrival time                                                978.73

clock clk (rise edge)                                1000.00    1000.00
clock network delay (ideal)                             0.00    1000.00
ans_reg_17_/CLK (DFFHQNx1_ASAP7_75t_R)                  0.00    1000.00 r
library setup time                                    -19.79     980.21
data required time                                               980.21
-----------------------------------------------------------------------------
data required time                                               980.21
data arrival time                                               -978.73
-----------------------------------------------------------------------------
slack (MET)                                                        1.48
```

根據 timing report，critical path 的起點在 Weight_3_reg_1，終點在 ans_reg_17，如圖所示

還沒 gate 的時候，critical path 會從 IFM 出發，但當使用 CG 後，critical path 起點是從 weight_reg 開始。