DIC HW2

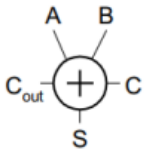
312510190 張家瑋

Exercise 2-1: 1-bit Full Adder standard cell

Full Adder

$S = A \oplus B \oplus C$

$C_{out} = MAJ(A,B,C)$



A	B	C	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Implement 1-bit FA by XOR and MAJ gates in the cell library，實作結果如下:

```
41  x_xor1 a_in  b_in      VDD GND ab_in XOR2x2_ASAP7_75t_R
42  x_xor2 ab_in c_in      VDD GND s_o   XOR2x2_ASAP7_75t_R
43  x_maj  a_in  b_in c_in VDD GND c_o   MAJx2_ASAP7_75t_R
44
```

測出結果如下圖:

```
******
.title ex2_1

****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=   5.3878u  from=   0.             to=  80.0000n
tphl_cout=  39.9992p  targ=   2.0718n   trig=   2.0318n
tr_sout=  43.9107p  targ=   2.0757n   trig=   2.0318n

         ***** job concluded
******
.title ex2_1

****** job statistics summary tnom=  25.000 temp=  25.000 ******

****** Machine Information ******
```

power	Delay = tphl_cout
5.3878 uW	**39.9992 ps**

Exercise 2-2: Different logic family of 1-bit Full Adders

CMOS:

```
******
.title diff_logicfamily_1bit_fa

****** transient analysis tnom=  25.000 temp=  25.000 ******
average_power_cmos=  14.1882u  from=   0.             to= 640.0000n
average_power_cpl=   8.3654u  from=   0.             to= 640.0000n
average_power_dcvs=   5.1702u  from=   0.             to= 640.0000n
tphl_cout_cmos=  71.7991p  targ=   5.2445n   trig=   5.1727n
tr_sout_cmos=  49.7442p  targ=   5.2224n   trig=   5.1727n
tphl_cout_cpl= 187.4632p  targ=   5.3601n   trig=   5.1727n
tr_sout_cpl=  74.7973p  targ=   5.2475n   trig=   5.1727n
tphl_cout_dcvs= 841.1834p  targ=   6.0138n   trig=   5.1727n
tr_sout_dcvs=   2.0202n  targ=   7.1929n   trig=   5.1727n

         ***** job concluded
******
.title diff_logicfamily_1bit_fa
```

```
******  Circuit Statistics  ******
# nodes       =      29 # elements   =      58
# resistors   =       0 # capacitors =       2 # inductors   =       0
# mutual_inds =       0 # vccs       =       0 # vcvs        =       0
# cccs        =       0 # ccvs       =       0 # volt_srcs   =       4
# curr_srcs   =       0 # diodes     =       0 # bjts        =       0
# jfets       =       0 # mosfets    =      52 # U elements  =       0
# T elements  =       0 # W elements =       0 # B elements  =       0
# S elements  =       0 # P elements =       0 # va device   =       0
# vector_srcs =       0 # N elements =       0
```

CPL_type:

```
******
.title diff_logicfamily_1bit_fa

****** transient analysis tnom=  25.000 temp=  25.000 ******
average_power_cmos=  14.1882u  from=   0.             to= 640.0000n
average_power_cpl=   8.3654u  from=   0.             to= 640.0000n
average_power_dcvs=   5.1702u  from=   0.             to= 640.0000n
tphl_cout_cmos=  71.7991p  targ=   5.2445n   trig=   5.1727n
tr_sout_cmos=  49.7442p  targ=   5.2224n   trig=   5.1727n
tphl_cout_cpl= 187.4632p  targ=   5.3601n   trig=   5.1727n
tr_sout_cpl=  74.7973p  targ=   5.2475n   trig=   5.1727n
tphl_cout_dcvs= 841.1834p  targ=   6.0138n   trig=   5.1727n
tr_sout_dcvs=   2.0202n  targ=   7.1929n   trig=   5.1727n

         ***** job concluded
******
.title diff_logicfamily_1bit_fa
```

```
# cccs        =       0 # ccvs       =       0 # volt_srcs   =       4
# curr_srcs   =       0 # diodes     =       0 # bjts        =       0
# jfets       =       0 # mosfets    =      44 # U elements  =       0
# T elements  =       0 # W elements =       0 # B elements  =       0
# S elements  =       0 # P elements =       0 # va device   =       0
# vector_srcs =       0 # N elements =       0
```

DCVS-type:

```
******
.title diff_logicfamily_1bit_fa

****** transient analysis tnom=  25.000 temp=  25.000 ******
average_power_cmos=  14.1882u  from=   0.             to= 640.0000n
average_power_cpl=   8.3654u  from=   0.             to= 640.0000n
average_power_dcvs=   5.1702u  from=   0.             to= 640.0000n
tphl_cout_cmos=  71.7991p  targ=   5.2445n   trig=   5.1727n
tr_sout_cmos=  49.7442p  targ=   5.2224n   trig=   5.1727n
tphl_cout_cpl= 187.4632p  targ=   5.3601n   trig=   5.1727n
tr_sout_cpl=  74.7973p  targ=   5.2475n   trig=   5.1727n
tphl_cout_dcvs= 841.1834p  targ=   6.0138n   trig=   5.1727n
tr_sout_dcvs=   2.0202n  targ=   7.1929n   trig=   5.1727n

         ***** job concluded
******
.title diff_logicfamily_1bit_fa
```

```
******  Circuit Statistics  ******
# nodes       =      30 # elements   =      56
# resistors   =       0 # capacitors =       2 # inductors   =       0
# mutual_inds =       0 # vccs       =       0 # vcvs        =       0
# cccs        =       0 # ccvs       =       0 # volt_srcs   =       4
# curr_srcs   =       0 # diodes     =       0 # bjts        =       0
# jfets       =       0 # mosfets    =      50 # U elements  =       0
# T elements  =       0 # W elements =       0 # B elements  =       0
# S elements  =       0 # P elements =       0 # va device   =       0
# vector_srcs =       0 # N elements =       0
```

	power	Performance (delay)	Area (transistor count)
CMOS	**14.1882 uW**	**74.7991 ps**	**52**
CPL-type	**8.3654 uW**	**187.4632 ps**	**44**
DCVS-type	**5.1702 uW**	**841.1834 ps**	**50**

Exercise 2-3: Design a 4 - Bit Adder

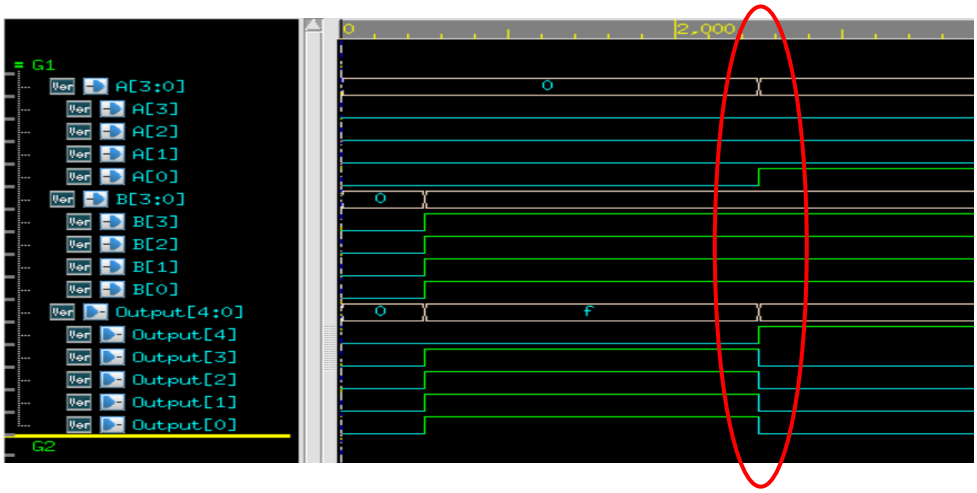
Timing Report:

```
Point                                          Incr       Path
-------------------------------------------------------------
input external delay                           0.00       0.00 r
A[1] (in)                                      0.00       0.00 r
A2/A (Adder_1bit_2)                            0.00       0.00 r
A2/U1/Y (INVx3_ASAP7_75t_R)                    3.37       3.37 f
A2/U4/Y (NAND2x1p5_ASAP7_75t_R)                5.83       9.20 r
A2/U5/Y (NAND2xp5_ASAP7_75t_R)                 8.25      17.45 f
A2/U10/Y (AND2x2_ASAP7_75t_R)                 20.06      37.52 f
A2/U2/Y (NOR2x1p5_ASAP7_75t_R)                14.09      51.61 r
A2/Cout (Adder_1bit_2)                         0.00       51.61 r
A3/Cin (Adder_1bit_1)                          0.00       51.61 r
A3/U2/Y (NOR2x1p5_ASAP7_75t_R)                11.60      63.21 f
A3/U1/Y (NOR2x1p5_ASAP7_75t_R)                11.37      74.57 r
A3/Cout (Adder_1bit_1)                         0.00       74.57 r
A4/Cin (Adder_1bit_0)                          0.00       74.57 r
A4/U1/Y (NOR2xp67_ASAP7_75t_R)                 8.99       83.57 f
A4/U3/Y (NOR2xp33_ASAP7_75t_R)                 6.22       89.79 r
A4/Cout (Adder_1bit_0)                         0.00       89.79 r
Output[4] (out)                                0.00       89.79 r
data arrival time                                         89.79

max_delay                                     90.00       90.00
output external delay                          0.00       90.00
data required time                                        90.00
-------------------------------------------------------------
data required time                                        90.00
data arrival time                                        -89.79
-------------------------------------------------------------
slack (MET)                                               0.21


1
exit
```

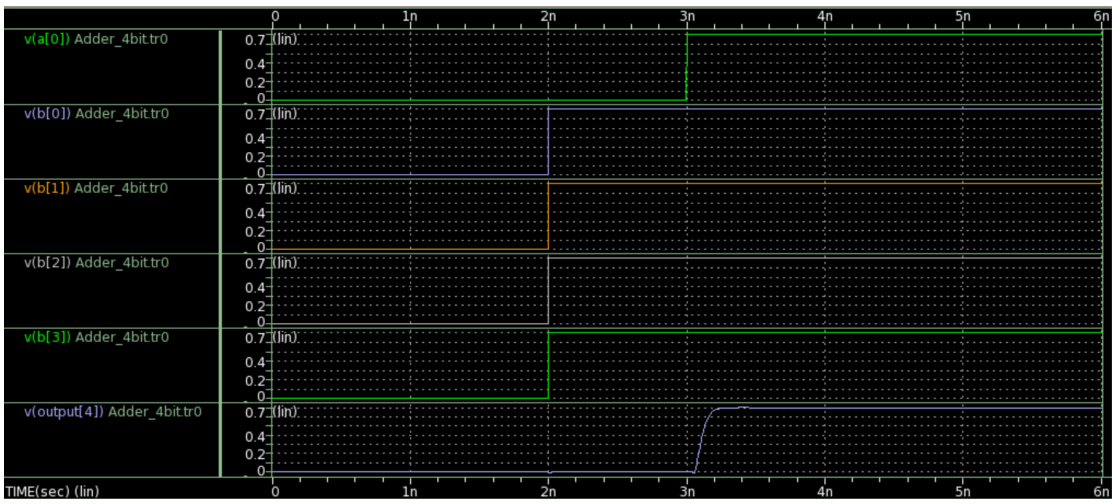
Critical Path: A[0]至 Output[4]

```
NAND2x1p5_ASAP7_75t_R U21 ( .A(A[0]), .B(B[0]), .Y(n15) );
NOR2xp33_ASAP7_75t_R U22 ( .A(n8), .B(n15), .Y(n16) );
NOR3xp33_ASAP7_75t_R U17 ( .A(n16), .B(n9), .C(n17), .Y(n10) );
NOR2xp67_ASAP7_75t_R U13 ( .A(n11), .B(n10), .Y(n21) );
MAJIxp5_ASAP7_75t_R U25 ( .A(n21), .B(A[3]), .C(B[3]), .Y(n12) );
INVxp33_ASAP7_75t_R U26 ( .A(n12), .Y(Output[4]) );
```

Pattern:



Exercise 2-4: CMOS Logics for 4-Bit Adder




```
****** transient analysis tnom=  25.000 temp=  25.000 ******
avg_power_nand=  17.3089u  from=   0.            to=   6.0000n
worst_case_delay= 107.8989p  targ=   3.1079n   trig=   3.0000n
```

Power	17.3089 uW
worst delay	107.8989 ps

```
Radix  1 1 1 1 1 1 1 1
Vname  A[3] A[2] A[1] A[0] B[3] B[2] B[1] B[0]
IO     i i i i i i i i
Tunit  ns
Period 0.2
Trise  0.00
Tfall  0.00
Tdelay 1
Vih    0.7
Vil    0.0

0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 1 1 1 1
0 0 0 0 1 1 1 1
0 0 0 0 1 1 1 1
0 0 0 0 1 1 1 1
0 0 0 1 1 1 1 1
0 0 0 1 1 1 1 1
0 0 0 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
```

Worst delay case

Worst power case

由 2-2 的結果得知 Worst delay case 為 A[0]至 Output[4]；

當 B[3:0]為{1,1,1,1}時，假如 A[0]由 0 變為 1，Output[4]則會由 0 變為 1，此即為 Worst delay case