DIC HW4

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4-1:

PART1: Synthesize the 2x2 convolution kernel provided by TA based on ASAP 7nm standard cells.

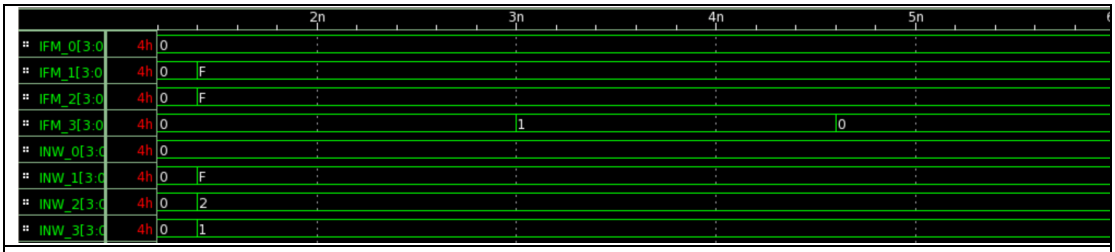
```
Startpoint: INW_3[2] (input port)
Endpoint: Output[8] (output port)
Path Group: default
Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------------
input external delay                                    0.00       0.00 f
INW_3[2] (in)                                           0.00       0.00 f
mult_19_4/b[2] (Convolution_DW_mult_uns_0)              0.00       0.00 f
mult_19_4/U116/Y (NAND2xp33_ASAP7_75t_R)               20.81      20.81 r
mult_19_4/U114/Y (NOR2xp33_ASAP7_75t_R)                30.77      51.58 f
mult_19_4/U39/SN (FAx1_ASAP7_75t_R)                    61.57     113.15 f
mult_19_4/U95/Y (XNOR2xp5_ASAP7_75t_R)                 28.23     141.37 r
mult_19_4/U92/Y (NAND2xp33_ASAP7_75t_R)                12.63     154.01 f
mult_19_4/U91/Y (NAND2xp33_ASAP7_75t_R)                25.12     179.12 r
mult_19_4/U87/Y (NAND2xp33_ASAP7_75t_R)                14.50     193.62 f
mult_19_4/U86/Y (NAND2xp33_ASAP7_75t_R)                25.11     218.74 r
mult_19_4/U82/Y (NAND2xp33_ASAP7_75t_R)                14.50     233.23 f
mult_19_4/U81/Y (NAND2xp33_ASAP7_75t_R)                25.11     258.34 r
mult_19_4/U78/Y (XOR2xp5_ASAP7_75t_R)                  39.48     297.82 r
mult_19_4/product[6] (Convolution_DW_mult_uns_0)        0.00     297.82 r
add_1_root_add_0_root_add_19_3/B[6] (Convolution_DW01_add_2)
                                                        0.00     297.82 r
add_1_root_add_0_root_add_19_3/U1_6/SN (FAx1_ASAP7_75t_R)
                                                       40.86     338.68 r
add_1_root_add_0_root_add_19_3/U11/Y (INVx1_ASAP7_75t_R)
                                                       17.87     356.55 f
add_1_root_add_0_root_add_19_3/SUM[6] (Convolution_DW01_add_2)
                                                        0.00     356.55 f
add_0_root_add_0_root_add_19_3/B[6] (Convolution_DW01_add_0)
                                                        0.00     356.55 f
add_0_root_add_0_root_add_19_3/U1_6/CON (FAx1_ASAP7_75t_R)
                                                       22.90     379.45 r
add_0_root_add_0_root_add_19_3/U4/Y (INVx1_ASAP7_75t_R)
                                                       15.27     394.72 f
add_0_root_add_0_root_add_19_3/U1_7/CON (FAx1_ASAP7_75t_R)
                                                       20.30     415.02 r
add_0_root_add_0_root_add_19_3/U3/Y (INVx1_ASAP7_75t_R)
                                                       15.27     430.29 f
add_0_root_add_0_root_add_19_3/U1_8/SN (FAx1_ASAP7_75t_R)
                                                       37.50     467.79 f
add_0_root_add_0_root_add_19_3/U11/Y (INVx1_ASAP7_75t_R)
                                                        8.03     475.82 r
add_0_root_add_0_root_add_19_3/SUM[8] (Convolution_DW01_add_0)
                                                        0.00     475.82 r
Output[8] (out)                                         0.00     475.82 r
data arrival time                                                475.82

max_delay                                             500.00     500.00
output external delay                                   0.00     500.00
data required time                                               500.00
-----------------------------------------------------------------------------
data required time                                               500.00
data arrival time                                               -475.82
-----------------------------------------------------------------------------
slack (MET)                                                      24.18
```

Critical Path: From IFM_3[0] to Output[8]

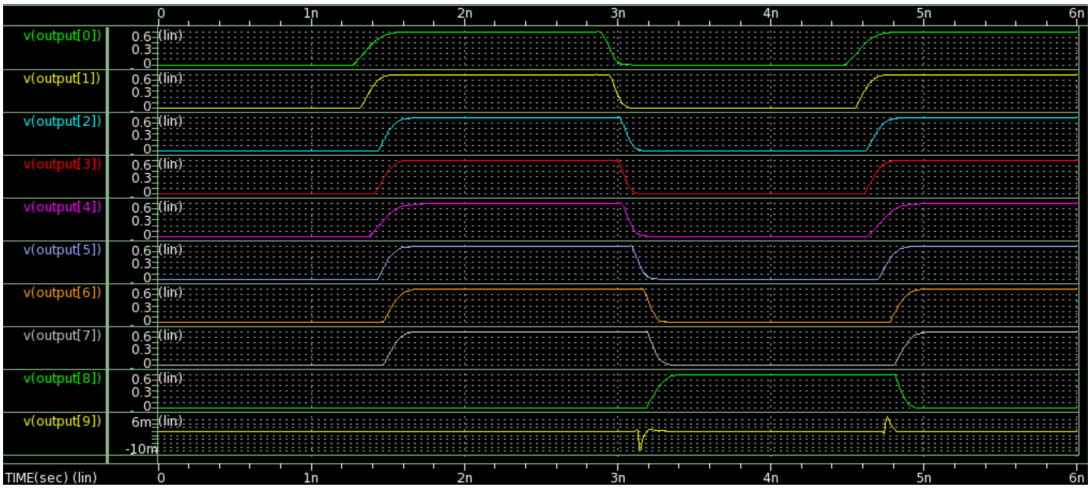
Input Pattern:

Vector num	IFM0	INW0	IFM1	INW1	IFM2	INW2	IFM3	INW3	Output
1	0000	0000	0000	0000	0000	0000	0000	0000	0000000000
	0	0	15	15	15	2	0	1	255
2	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
3	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
4	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
5	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
6	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
7	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
8	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
9	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
	0	0	15	15	15	2	1	1	256
10	0000	0000	1111	1111	1111	0010	0001	0001	0100000000
11	0000	0000	1111	1111	1111	0010	0001	0001	0100000000
12	0000	0000	1111	1111	1111	0010	0001	0001	0100000000
13	0000	0000	1111	1111	1111	0010	0001	0001	0100000000
14	0000	0000	1111	1111	1111	0010	0001	0001	0100000000
15	0000	0000	1111	1111	1111	0010	0001	0001	0100000000
16	0000	0000	1111	1111	1111	0010	0001	0001	0100000000
17	0000	0000	1111	1111	1111	0010	0001	0001	0100000000
	0	0	15	15	15	2	0	1	255
18	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
19	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
20	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
21	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
22	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
23	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
24	0000	0000	1111	1111	1111	0010	0000	0001	0011111111
25	0000	0000	1111	1111	1111	0010	0000	0001	0100000011

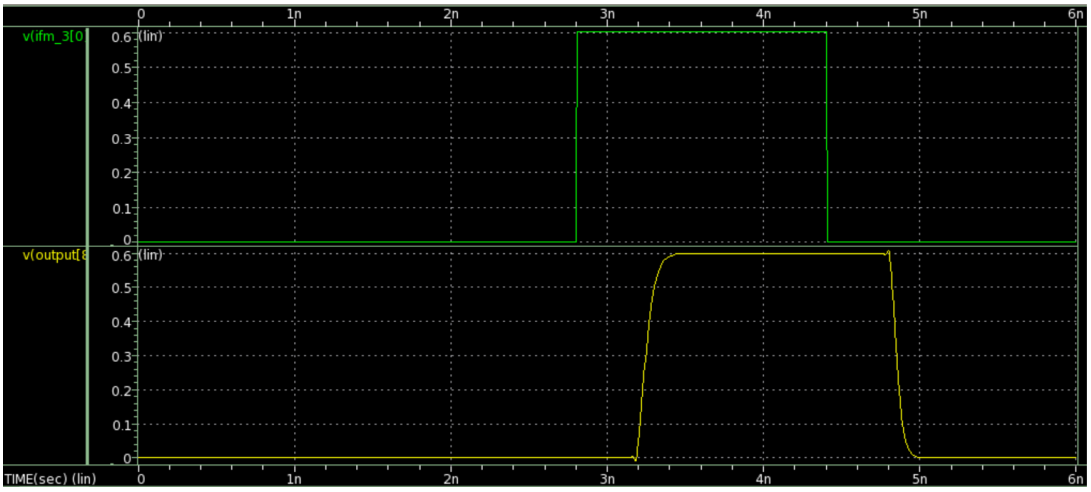
Input Data Wave



Output Data Wave



Critical Path Wave

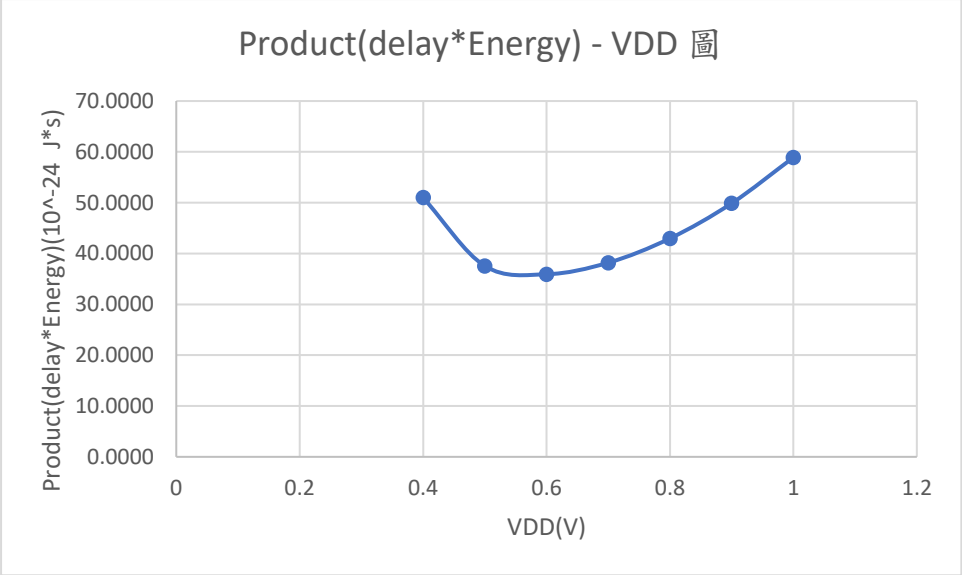


PART2: Analyze and Plot EDP-voltage figure.

VDD (V)	Power (uW)	Energy (fJ)	Delay (ps)	Product (J·s)
1.0	43.2955	259.7730	226.7129	58.8942 e^{-24}
0.9	33.7150	202.2900	246.6001	49.8846 e^{-24}
0.8	25.6047	153.6282	279.7146	42.9720 e^{-24}
0.7	18.8691	113.2146	337.3468	38.1924 e^{-24}
0.6	13.4108	80.4648	446.4564	35.9241 e^{-24}
0.5	8.9527	53.7162	699.0870	37.5522 e^{-24}
0.4	5.4503	32.7018	1559.0	50.9982 e^{-24}

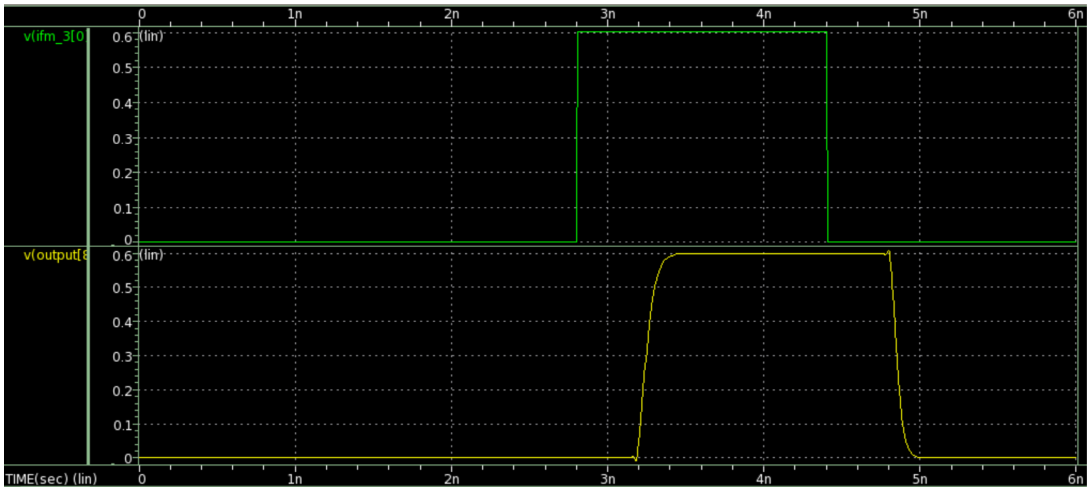
如何得到 Energy？

Step1: **測量 power**	.meas tran AVG_Power_Convolution AVG power power_delay_product= 5.9873f
Step2: **乘 transition time**	.tran 0.1ps 6ns energy_delay_product= 3.5924e-23



PART3:Find out the minimal energy-delay product of the 2x2 convolution kernel by voltage scaling

在 VDD=0.6V，可得到最小的 product (最佳解)；波形及 delay、power 等資訊如下圖所示：




```
****** transient analysis tnom=  25.000 temp=  25.000 ******
avg_power_convolution=  13.4108u  from=   0.             to=   6.0000n
worst_case_delay_rise= 453.4589p  targ=   3.2593n   trig=   2.8058n
worst_case_delay_fall= 439.4539p  targ=   4.8436n   trig=   4.4042n
worst_case_delay= 446.4564p
power_delay_product=   5.9873f
energy_delay_product= 3.5924e-23

         ***** job concluded
******
```

4-2:

PART1: Synthesize the comparator provided by TA based on ASAP 7nm standard cells then convert the .v to .sp for measurement.

```
****************************************

Operating Conditions: PVT_0P7V_25C   Library: asap7sc7p5t_INVBUF_RVT_TT_08302018
Wire Load Model Mode: top

  Startpoint: B[47] (input port)
  Endpoint: Out (output port)
  Path Group: default
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  B[47] (in)                               0.00       0.00 r
  U79/Y (XNOR2xp5_ASAP7_75t_R)            14.28      14.28 r
  U87/Y (NAND4xp25_ASAP7_75t_R)           18.47      32.74 f
  U74/Y (NOR5xp2_ASAP7_75t_R)             26.10      58.84 r
  U83/Y (NAND4xp25_ASAP7_75t_R)           21.97      80.81 f
  U10/Y (NOR5xp2_ASAP7_75t_R)             17.38      98.19 r
  Out (out)                                0.00      98.19 r
  data arrival time                                  98.19

  max_delay                              280.00     280.00
  output external delay                    0.00     280.00
  data required time                                280.00
  -----------------------------------------------------------
  data required time                                280.00
  data arrival time                                 -98.19
  -----------------------------------------------------------
  slack (MET)                                       181.81
```

.sp 檔模擬成功結果:

```
 Command Line Threads Count :     1
 Available CPU Count        :   256
 Actual Threads Count       :     1


 ******  Circuit Statistics  ******
 # nodes       =    9422 # elements   =   20922
 # resistors   =    8502 # capacitors =   11488 # inductors   =       0
 # mutual_inds =       0 # vccs       =       0 # vcvs        =       0
 # cccs        =       0 # ccvs       =       0 # volt_srcs   =       2
 # curr_srcs   =       0 # diodes     =       0 # bjts        =       0
 # jfets       =       0 # mosfets    =     802 # U elements  =       0
 # T elements  =       0 # W elements =       0 # B elements  =       0
 # S elements  =       0 # P elements =       0 # va device   =       0
 # vector_srcs =     128 # N elements =       0


 ******  Runtime Statistics (seconds)  ******

 analysis           time    # points   tot. iter  conv.iter
 op point           0.44           1          91
 transient          0.05       60001          62          31 rev=         0
 readin             0.18
 errchk             0.10
 setup              0.20
 output             0.00


          peak memory used        435.73 megabytes
          total cpu time            0.98 seconds
          total elapsed time        1.21 seconds
          job started at     20:02:47 12/04/2023
          job ended   at     20:02:48 12/04/2023

>info:         ***** hspice job concluded
          job total runtime         1.21 seconds


lic: Release hspice token(s)
lic: total license checkout elapse time:        0.22(s)
```

透過增加 INVBUF_RVT datasheet 中的 buffer 來降低 delay:

```
XU93 VSS VDD  n44_t n44 BUFx2_ASAP7_75T_R

XU56 VSS VDD  n55 n56 n57 n58 n59 n44_t NOR5xp2_ASAP7_75t_R
XU57 VSS VDD  B[56] A[56] n59 XOR2xp5_ASAP7_75t_R
XU58 VSS VDD  B[57] A[57] n58 XOR2xp5_ASAP7_75t_R
```

由圖可以發現，out 的 Tr 及 Tf 都小於 100ps，且 minimum delay 小於 1.5ns:

```
******
.title ex_4.2

****** transient analysis tnom=  25.000 temp=  25.000 ******
avg_power_convolution=   5.9525u  from=   0.            to=  60.0000n
worst_case_delay_rise=   1.4996n  targ=   5.5333n   trig=   4.0337n
tr_out=  51.4509p  targ=  13.5125n   trig=  13.4611n
tf_out=  48.1663p  targ=   8.6440n   trig=   8.5959n

         ***** job concluded
******
.title ex_4.2

****** job statistics summary tnom=  25.000 temp=  25.000 ******
```

PART2: Measure the PPA at 0.4v and 0.7v of minimized and synthesized comparator, and analyze

Under 0.4V:

```
******
.title ex_4.2

****** transient analysis tnom=  25.000 temp=  25.000 ******
avg_power_convolution=   5.9525u  from=   0.            to=  60.0000n
worst_case_delay_rise=   1.4996n  targ=   5.5333n   trig=   4.0337n
tr_out=  51.4509p  targ=  13.5125n   trig=  13.4611n
tf_out=  48.1663p  targ=   8.6440n   trig=   8.5959n

         ***** job concluded
******
.title ex_4.2

****** job statistics summary tnom=  25.000 temp=  25.000 ******
```

Under 0.7V:

```
******
.title ex_4.2

****** transient analysis tnom=  25.000 temp=  25.000 ******
avg_power_convolution=  10.6244u  from=   0.            to=  20.0000n
worst_case_delay_rise= 279.8368p  targ=   4.3125n   trig=   4.0327n
tr_out=  12.2597p  targ=   4.3110n   trig=   4.2988n
tf_out=  14.3784p  targ=   8.1634n   trig=   8.1490n

        ***** job concluded
******
.title ex_4.2

****** job statistics summary tnom=  25.000 temp=  25.000 ******

****** Machine Information ******
```

V	Worst_delay	power	Area counts
0.4v	1499.6ps	5.9525uW	9114
0.7v	279.8368ps	10.6244uW	9114

由此可知，當 0.7V 時，雖功率增加約一倍，但 minimum worst delay 縮小 5 倍之多，為 ECO 的效用。