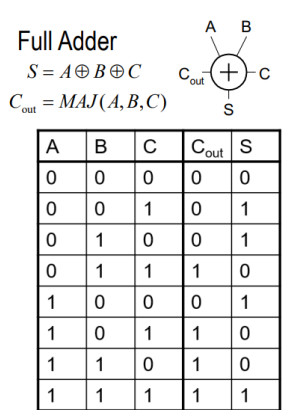
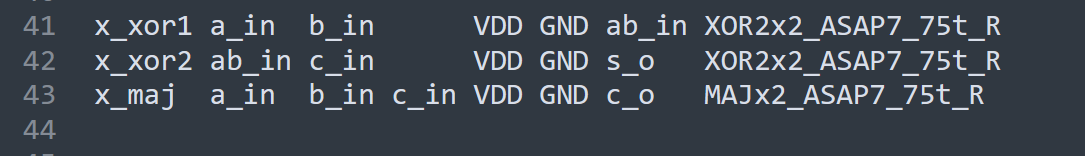
**DIC HW2**

312510190 張家瑋

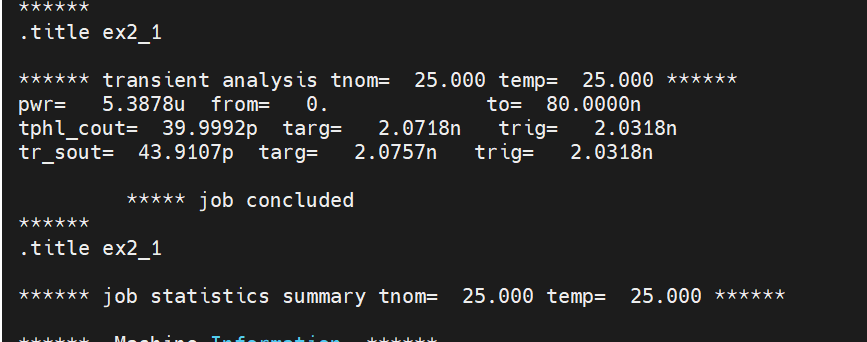
**Exercise 2-1:** **1-bit Full Adder standard cell**

****

Implement 1-bit FA by XOR and MAJ gates in the cell library，實作結果如下:

****

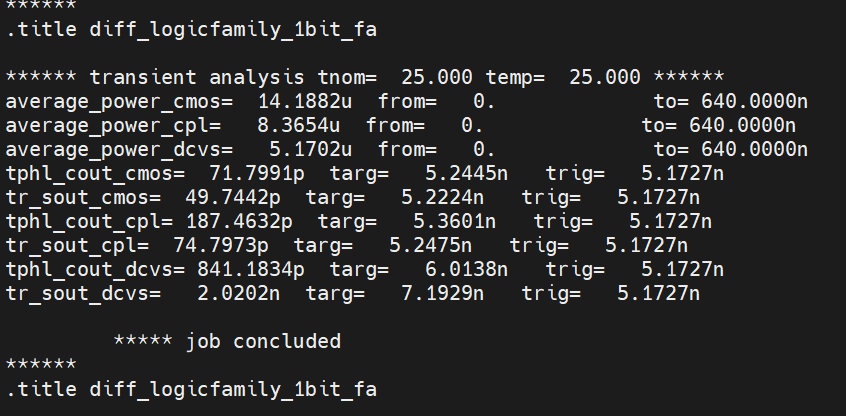
測出結果如下圖:

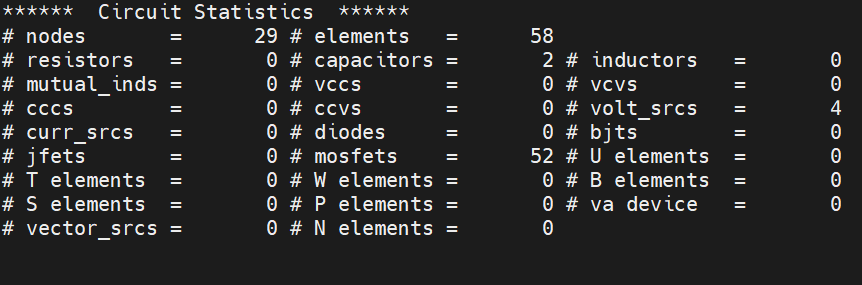
****

|  |  |
| --- | --- |
| power | Delay = tphl\_cout |
| **5.3878 uW** | **39.9992 ps** |

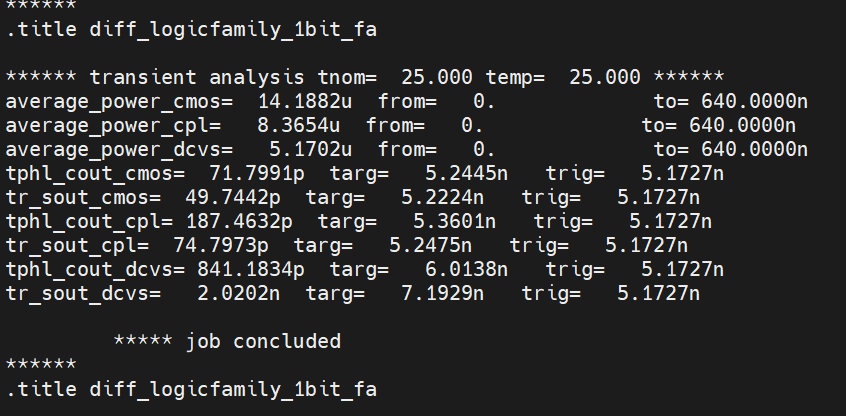
**Exercise 2-2: Different logic family of 1-bit Full Adders**

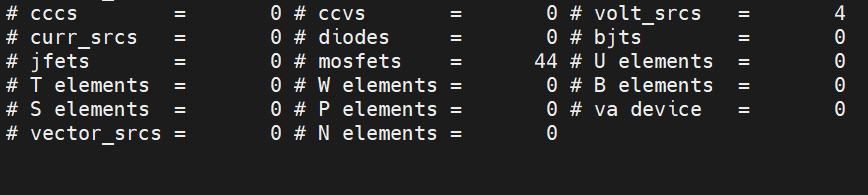
CMOS:



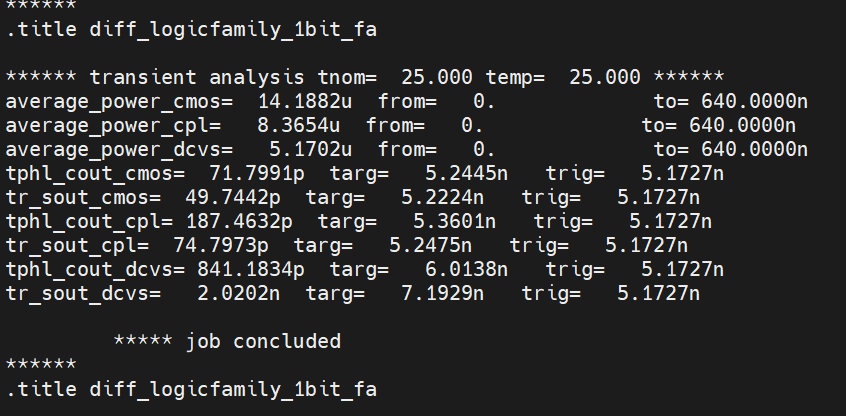


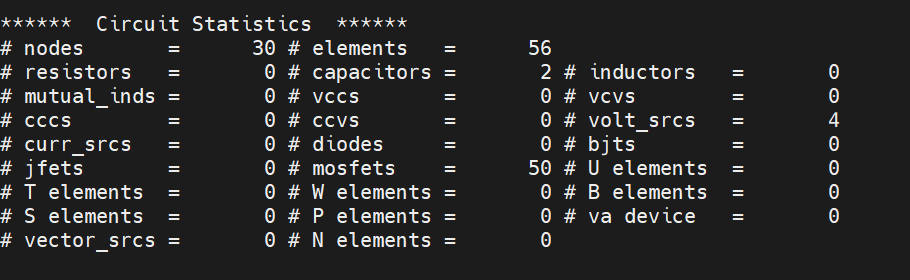
CPL\_type:





DCVS-type:

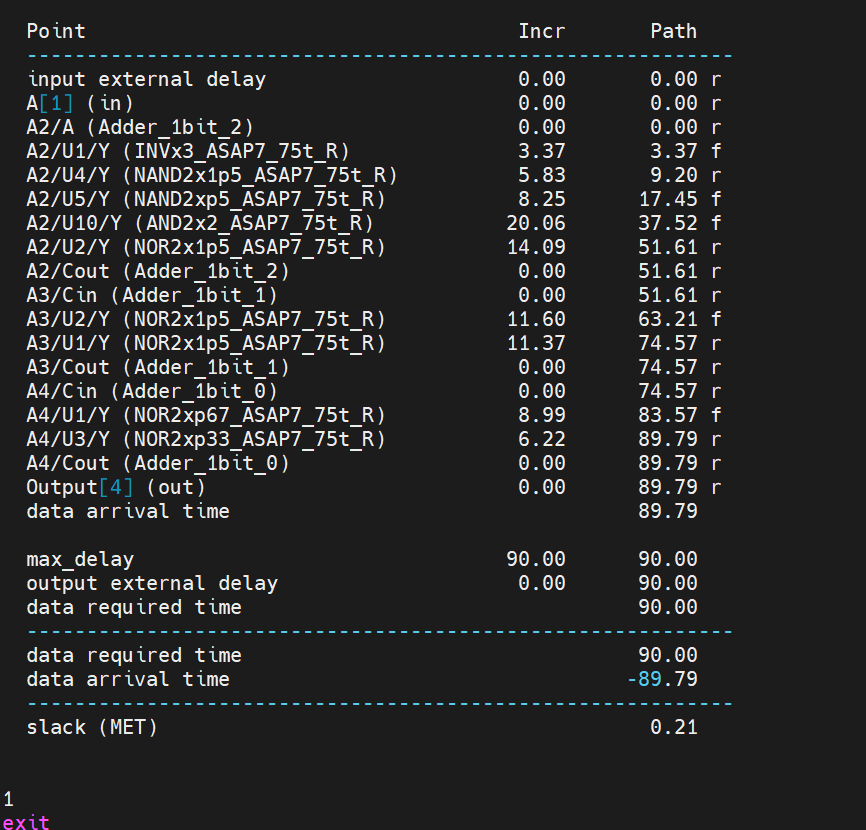




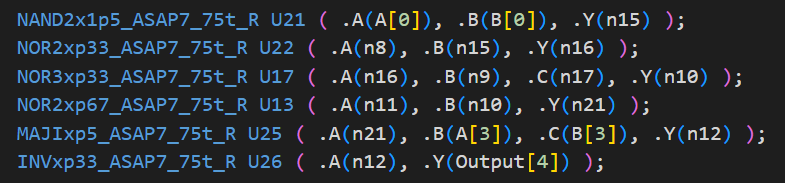
|  |  |  |  |
| --- | --- | --- | --- |
|  | power | Performance  (delay) | Area  (transistor count) |
| CMOS | **14.1882 uW** | **74.7991 ps** | **52** |
| CPL-type | **8.3654 uW** | **187.4632 ps** | **44** |
| DCVS-type | **5.1702 uW** | **841.1834 ps** | **50** |

**Exercise 2-3: Design a 4 - Bit Adder**

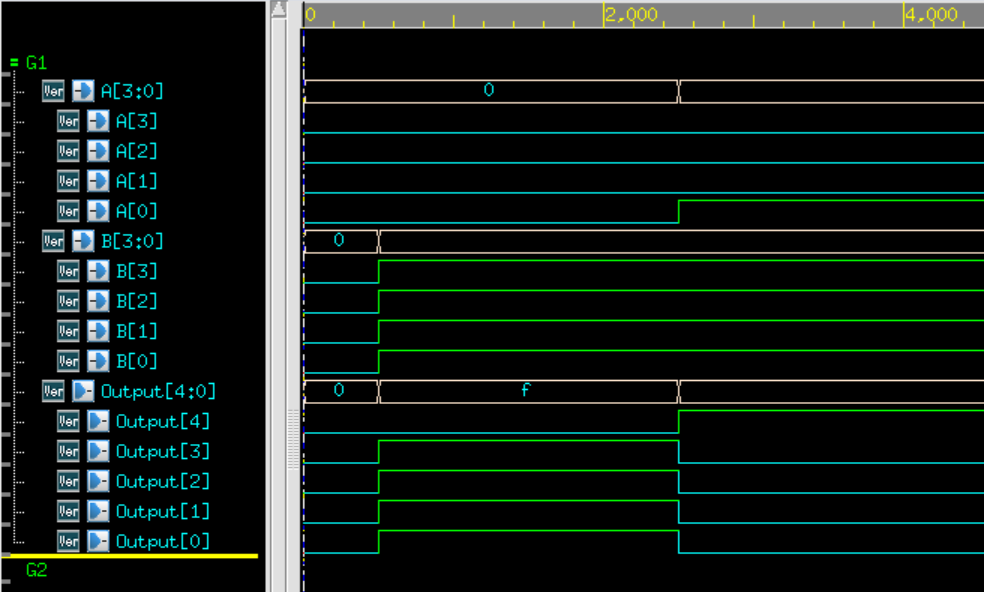
Timing Report:



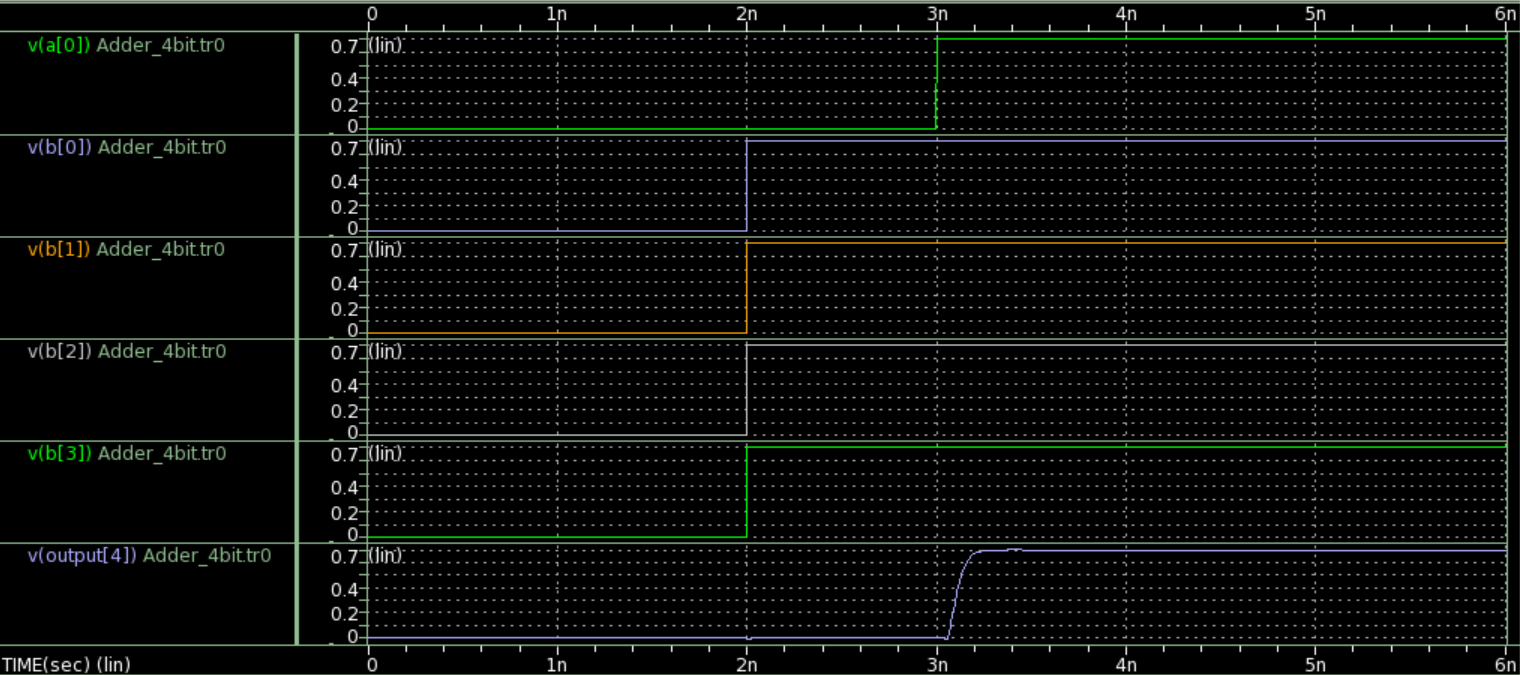
Critical Path: A[0]至Output[4]

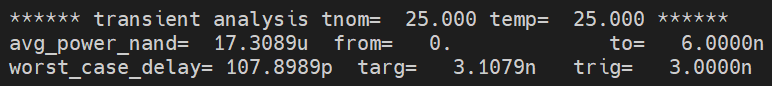


Pattern:

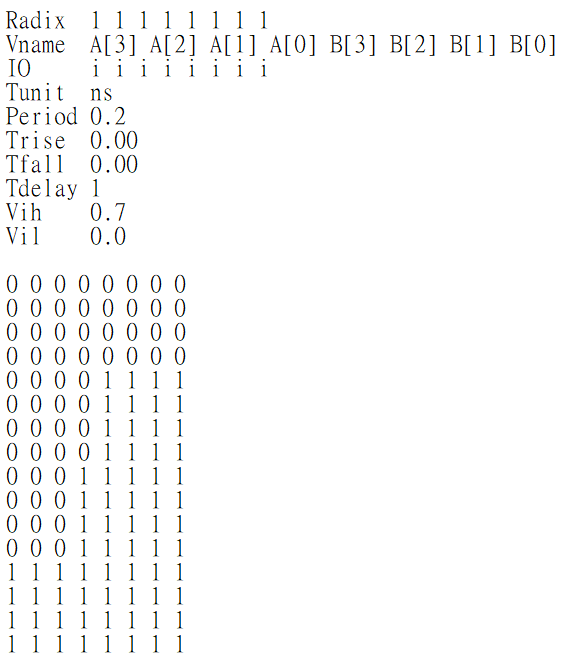


**Exercise 2-4: CMOS Logics for 4-Bit Adder**





|  |  |
| --- | --- |
| Power | 17.3089 uW |
| worst delay | 107.8989 ps |



Worst power case

Worst delay case

由2-2的結果得知Worst delay case為A[0]至Output[4]；

當B[3:0]為{1,1,1,1}時，假如A[0]由0變為1，Output[4]則會由0變為1，此即為Worst delay case