## **HW1 Report**

Simulation results demonstrate the predicted output for the provided input data:

```
SystemC 2.3.3-Accellera --- Mar 2 2024 23:27:20
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       ALL RIGHTS RESERVED
    idx |
             value | class name
    207
             15.407
                              golden retriever
             14.8607
                             Sussex spaniel
    220
    163
             14.6819
                             bloodhound
             14.5163
    175
                             otterhound
    219
             14.3564
                            cocker spaniel
Info: /OSCI/SystemC: Simulation stopped by user.
22:53 mlchip004@ee21[~/hw1]$ make
g++ -I . -I /RAID2/COURSE/mlchip/mlchipTA01/systemc-2.3.3/include -L
COURSE/mlchip/mlchipTA01/systemc-2.3.3/lib-linux64
./run
       SystemC 2.3.3-Accellera --- Mar 2 2024 23:27:20
       Copyright (c) 1996-2018 by all Contributors,
       ALL RIGHTS RESERVED
             value | class name
             19.9741
    285
                              Egyptian cat
             16.3325
    281
                              tabby
    282
             15.9074
                              tiger cat
    287
             15.0163
                              lynx
    728
             14.3206
                              plastic bag
Info: /OSCI/SystemC: Simulation stopped by user.
23:04 mlchip004@ee21[~/hw1]$
```

## implementation approach:

I construct one module called alexnet to include all convolutions layers and fclayers:

```
SC_MODULE(alexnet){
11
        sc_out <float> output_final[1000];
12
        float input[3][224][224];
13
        float weight_1st[3][11][11];
        float output_1st[64][27][27];
        float weight_2st[64][5][5];
17
        float output_2st[192][13][13];
18
        float weight_3st[192][3][3];
        float output_3st[384][13][13];
        float weight_4st[384][3][3];
21
        float output_4st[256][13][13];
22
        float weight_5st[256][3][3];
        float output_5st[256][13][13];
        float fc_6st[4096];
        float fc_7st[4096];
        float fc_8st[1000];
```

In the module, all the layers are written as functions, separately:

```
732 SC_CTOR(alexnet) {
733 SC_METHOD(conv1);
734 SC_METHOD(conv2);
735 SC_METHOD(conv3);
736 SC_METHOD(conv4);
737 SC_METHOD(conv5);
738 SC_METHOD(fc6);
739 SC_METHOD(fc7);
740 SC_METHOD(fc8);
741 }
742
743 };
```

One function complete all the calculate operations, including padding, convolution, bias addition, activation function, max-pooling:

```
int INPUT_CHANNELS = 3;
int INPUT_HEIGHT = 224;
int INPUT_WIDTH = 224;
int OUTPUT_CHANNELS = 64;
int OUTPUT_HEIGHT = 55;
int OUTPUT_WIDTH = 55;
int KERNEL_SIZE = 11;
int ZERO_PADDING = 1;
int STRIDE_SIZE = 4;
int pool_size = 3;
int pool_stride = 2;
int pool_output_height = 27;
int pool_output_width = 27;
float output[OUTPUT_CHANNELS][OUTPUT_HEIGHT][OUTPUT_WIDTH];
float bias[OUTPUT_CHANNELS];
std::ifstream input_file("dog.txt");
if (input_file.is_open()) {
     float temp;
     for (int ic = 0; ic < INPUT_CHANNELS; ic++) {
   for (int ih = 0; ih < INPUT_HEIGHT; ih++) {
     for (int iw = 0; iw < INPUT_WIDTH; iw++) {</pre>
                  input_file >> temp;
                   input[ic][ih][iw] = temp;
     input_file.close();
```

After the computations, I construct a monitor module to print out the outputs from alexnet:

## challenges faced:

At first, I use lots of float-type arrays to store values of weights, bias, and the output results, it comes out a "core dump" problem:

Then I start to deal with the weight arrays, trying not to identify the OUTPUT\_CHANNEL index in the weight arrays, it means: take the weight value from .txt file only when the computations need it, so it becomes:

## other observations or insights gained:

I've learned some in creating modules in systemC. In SystemC, a module represents the smallest container of functionality with state, behavior, and structure for hierarchical connectivity. Understanding the concept and usage of modules in SystemC is fundamental for building complex hardware and software systems.

Modules in SystemC facilitate hierarchical design, allowing designers to break down complex systems into smaller, more manageable components. This modular approach promotes reusability, scalability, and maintainability of designs.

While port communication is the preferred mechanism for inter-module communication, SystemC allows other communication mechanisms for debugging or diagnostic purposes. For example, direct method calls between modules or accessing internal module variables may be used temporarily for debugging, but such practices should be limited to diagnostic purposes and avoided in production designs.