Name:_____

Honor Pledge: I am adhering to the Honor Code while taking this test.

Signature:_____ Date:_____

25 points total. Don’t miss the binary arithmetic on the back of the last page!

1. The trustees of Karnaugh University (Alice, Bob, Carol, and David) are voting on whether they should bother to vote in the presidential election. They build a digital circuit to help them decide.

If at least three trustees vote 1, they will vote in the presidential election.

If Alice and Bob vote 0 while Carol and David vote 1, or if Alice and Bob vote 1 while Carol and David vote 0, they are frozen in indecision and will not vote in the presidential election.

In all other cases, the trustees don't care how their circuit responds (though they will follow its output regardless).

A. Complete this truth table, where 1 as an output represents the decision to vote. X as an output represents "don't care."

A	B	C	D	VOTE
0	0	0	0	X
0	0	0	1	X
0	0	1	0	X
0	0	1	1	0
0	1	0	0	X
0	1	0	1	X
0	1	1	0	X
0	1	1	1	1
1	0	0	0	X
1	0	0	1	X
1	0	1	0	X
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

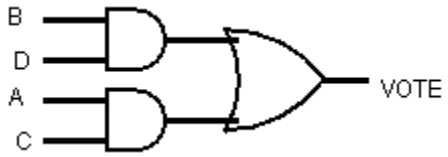
B. Write out a K map equivalent to the truth table.

		CD			
		00	01	11	10
AB	00	**X**	**X**	**0**	**X**
	01	**X**	**X**	**1**	**X**
	11	**0**	**1**	**1**	**1**
	10	**X**	**X**	**1**	**X**

C. Write out any logic equation that implements the truth table. You may use as many gates as you like.

B&D|A&C. Alternatively, B&C|A&D.

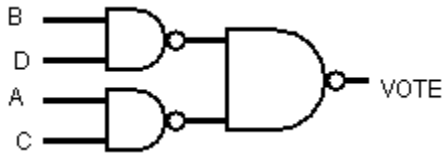
D. Write out the circuit diagram equivalent to the logic equation.



E. Write out a minimized logic equation. (Hint: Only three gates are required. A NOT "bubble" at an output does not count as a separate gate because NOR gates and NAND gates are standard, commercially available gates. A NOT "bubble" at an input **does** count as a separate gate.) Your responses to C and E may be identical.

B&D|A&C

F. Write an equivalent circuit diagram using only NAND gates. Your responses to D and F may be identical.



2. Edward, Carlisle, Esme, Alice, Emmett, Rosalie, and Jasper are voting on whether to turn Bella into a vampire. Edward votes NO. Emmett votes the same way as Alice, and Jasper votes the same way as Rosalie.

A. Complete this truth table, where 1 as an input represents a YES vote, and 1 as an output represents that a majority of the seven vampires voted YES.

Carlisle	Esme	Alice	Rosalie	Vampire
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

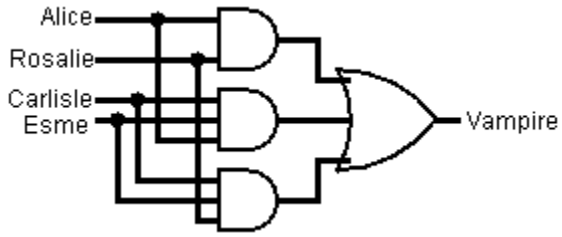
B. Write out a K map equivalent to the truth table.

		AliceRosalie			
		00	01	11	10
CarlisleEsme	00	**0**	**0**	**1**	**0**
	01	**0**	**0**	**1**	**0**
	11	**0**	**1**	**1**	**1**
	10	**0**	**0**	**1**	**0**

C. Write out minimized logic equation (using as few gates as possible) equivalent to the K map. (Hint: Four gates are required.)

Alice&Rosalie | Carlisle&Esme&Alice | Carlisle&Esme&Rosalie

D. Draw the circuit diagram equivalent to your response to part C.



E. (Seven points.) Write a Verilog module that computes a sum and uses an **if** statement to determine whether Bella is turned into a vampire. There should be four input variables: Carlisle, Esme, Alice, and Rosalie.

```
module partF (input Carlisle, input Esme, input Alice, input Rosalie, output reg Vampire);

wire [2:0] sum;

assign sum = Carlisle + Esme + 2*Alice + 2*Rosalie;

always @ (*)

if (sum < 4) Vampire = 0;

else Vampire = 1;

endmodule
```

3. Consider the following module:

```
module main(
        input [7:0] sw,
        output [3:0] sum,
        output carry,
        output reg overflow
   );
assign {carry,sum} = sw[7:4] + sw[3:0];
always@(*)
        if (sum[3]==1&sw[7]==0&sw[3]==0|sum[3]==0&sw[7]==1&sw[3]==1)
                overflow=1;
        else
                overflow=0;
endmodule
```

A. Explain in words what this module does. Specifically, why is sum only four bits, while the input is 8 bits?
This module divides sw into two 4-bit numbers and sums them. The sum is only four bits, so there's a separate carry bit, as well as a two's complement overflow bit.

B. (Three points.) Determine sum (as a four bit number), carry, and overflow if the input is 01101011.
sum = 0001, carry = 1, overflow = 0

C. (Three points.) Determine sum (as a four bit number), carry, and overflow if the input is 01100011.
sum = 1001, carry = 0, overflow = 1

D. Suppose the always block is deleted, and overflow is changed from type reg to type wire. Write an assign statement that assigns the correct value to overflow.

```
assign overflow = sum[3]&~sw[7]&~sw[3]|~sum[3]&sw[7]&sw[3];
```