積體電路設計導論

PEX & post-simulation tutorial

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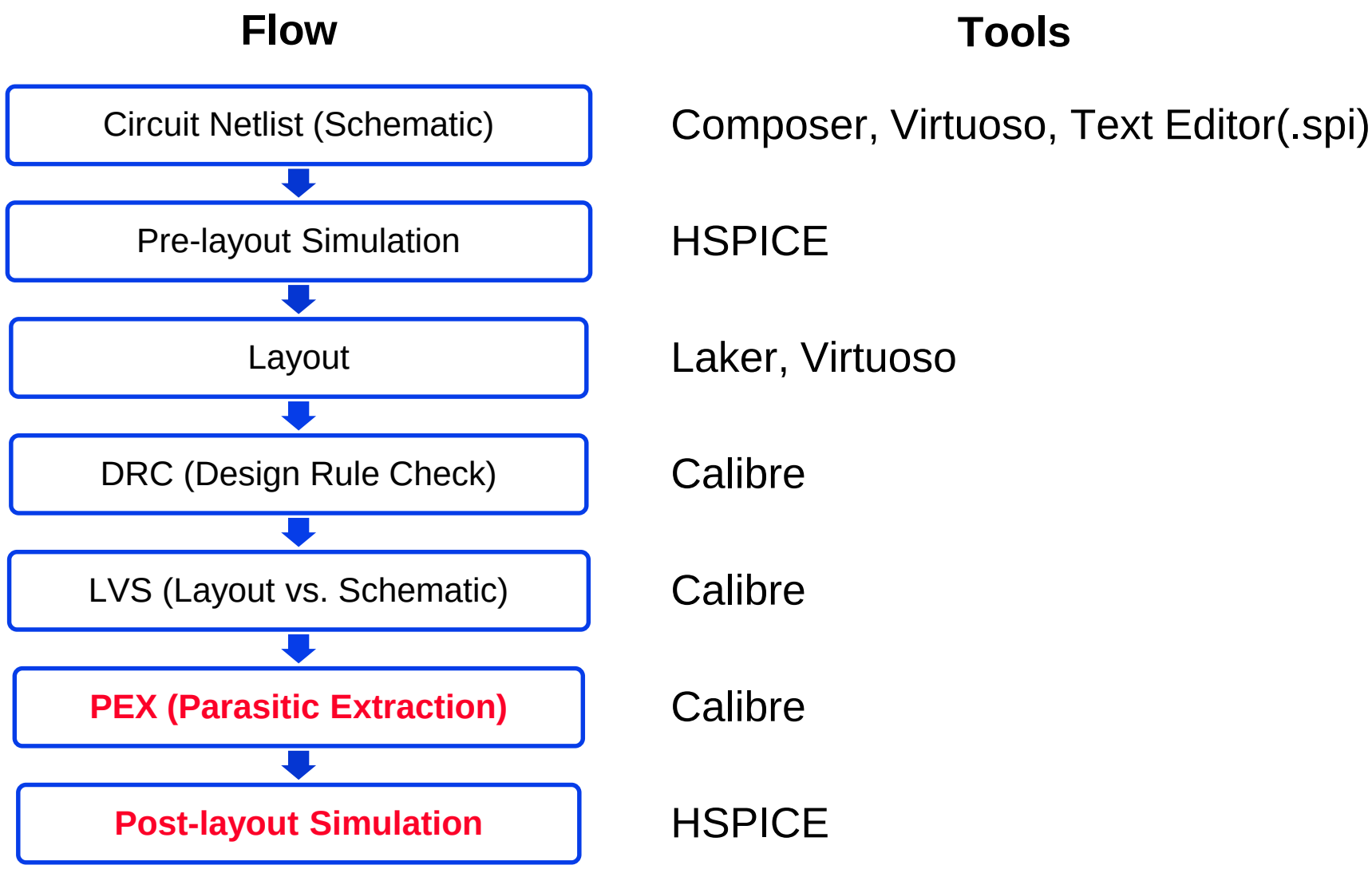
Outline

- Circuit Design Flow
- What is PEX?
- Parasitic Effects
- Calibre PEX Flow
- Post-simulation

Circuit Design Flow



What is PEX?

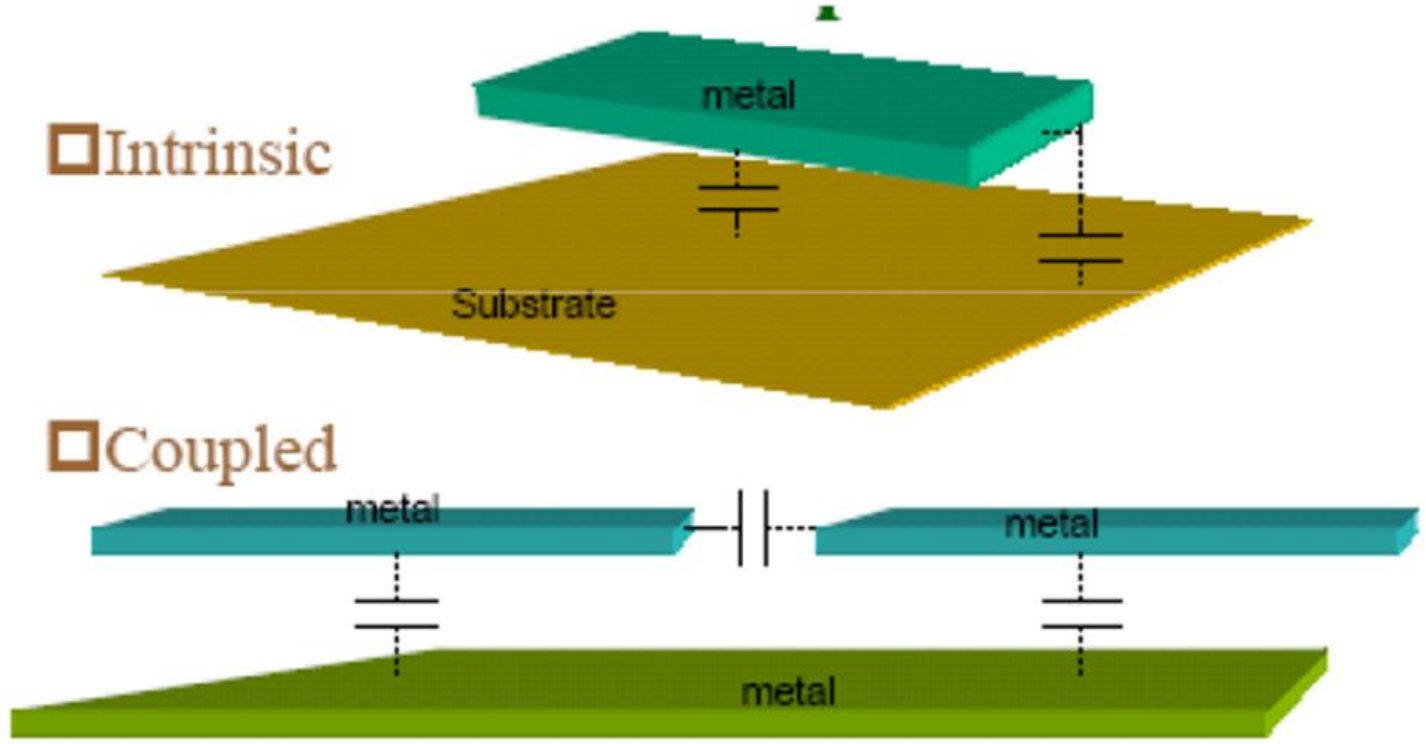
What is PEX?

- PEX means Parasitic Extraction
  - Extracts the parasitic effect resulted from the interconnection of layout design
  - Capacitance and Resistance are added to the new netlist file(.spi) for post simulation

Parasitic Effects

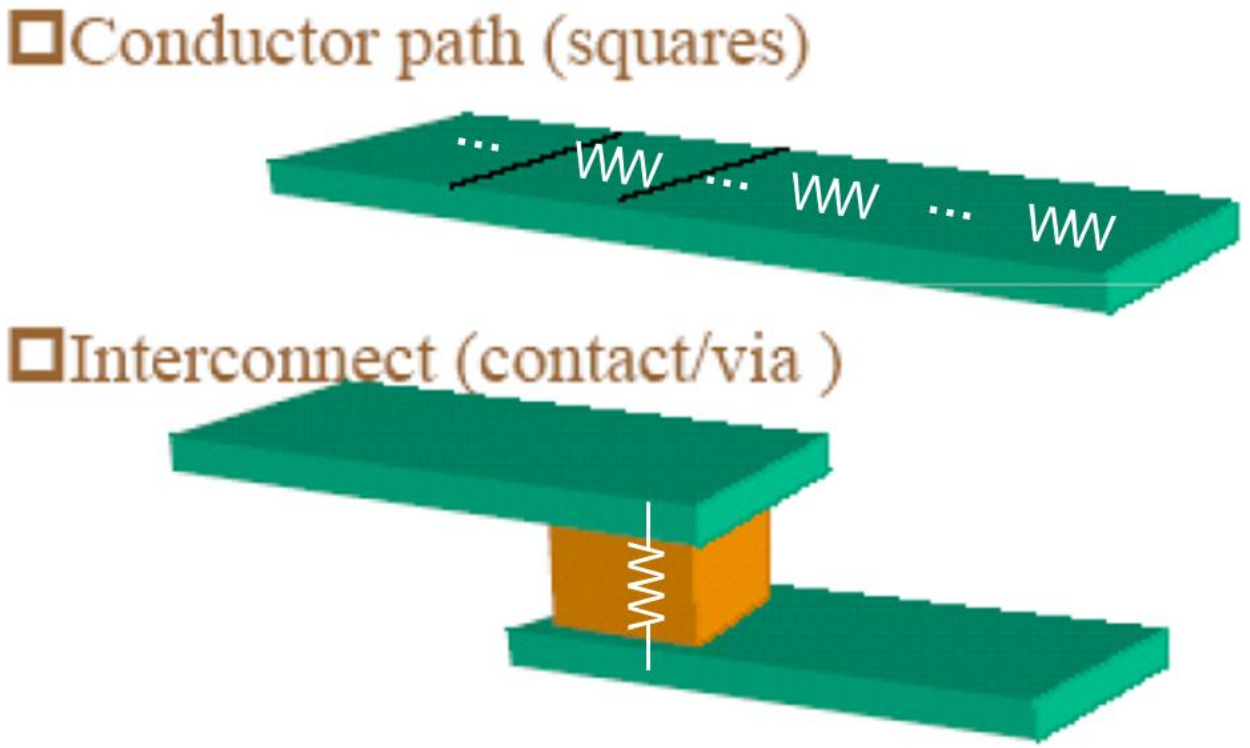
Parasitic Effects - Capacitance

- Parasitic Capacitance



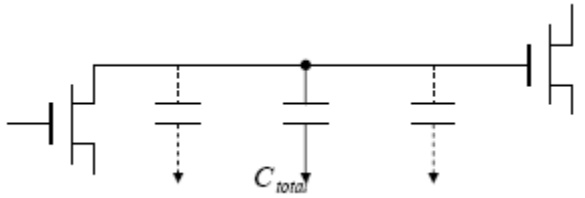
Parasitic Effects - Resistance

- Parasitic Resistance

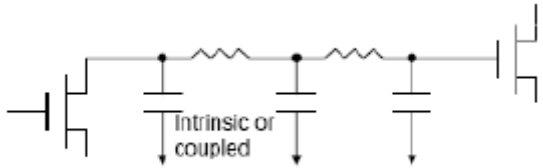


Parasitic Effects - (R+C)

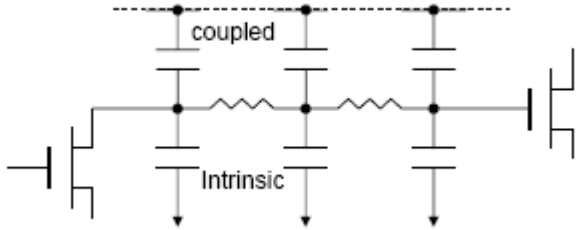
- Extraction option
  - Lumped Capacitance (C)



  - Distributed Resistance/Capacitance (RC)



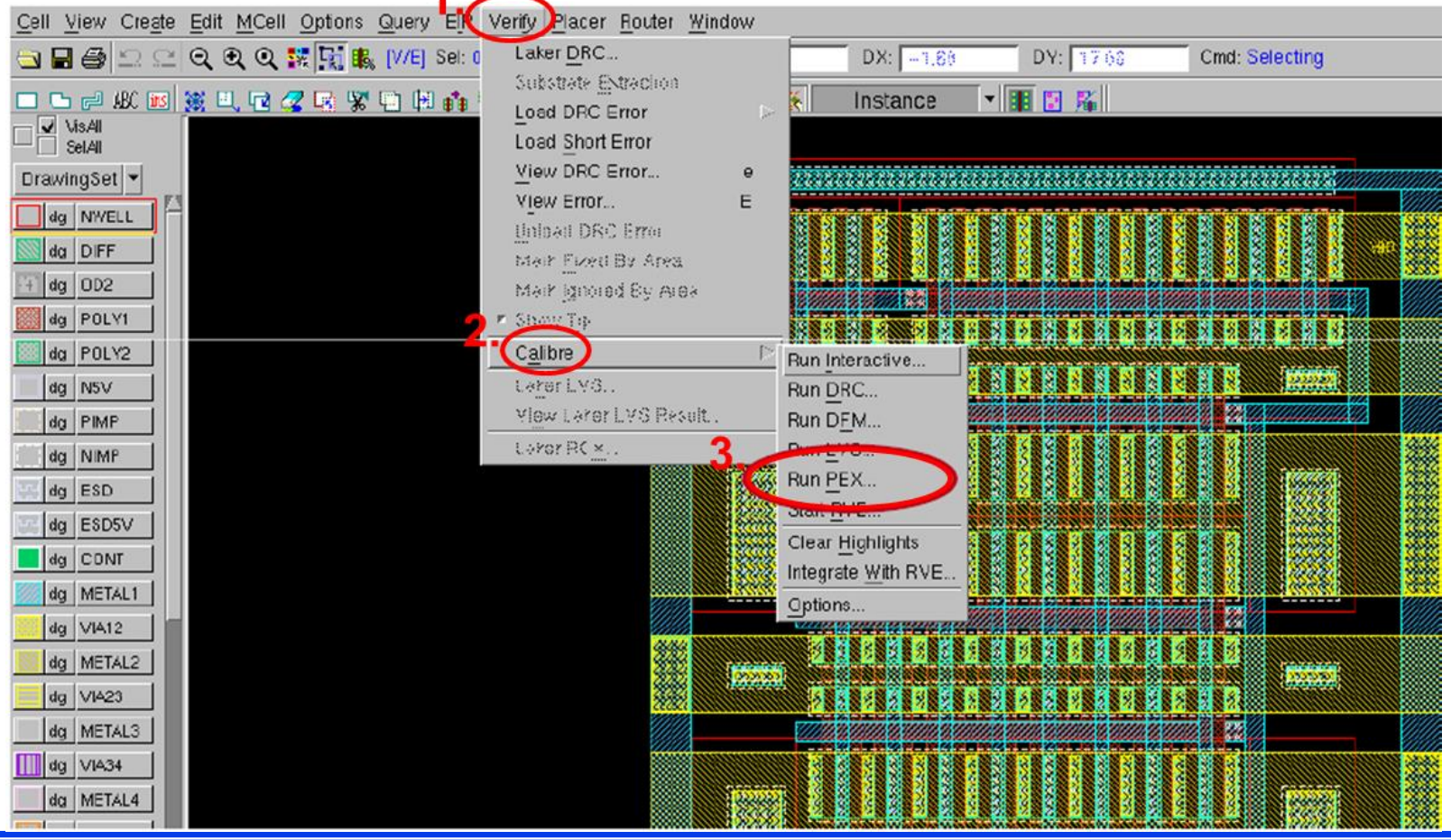
  - Distributed Resistance/Coupled Capacitance (RC+C)



Calibre PEX Flow

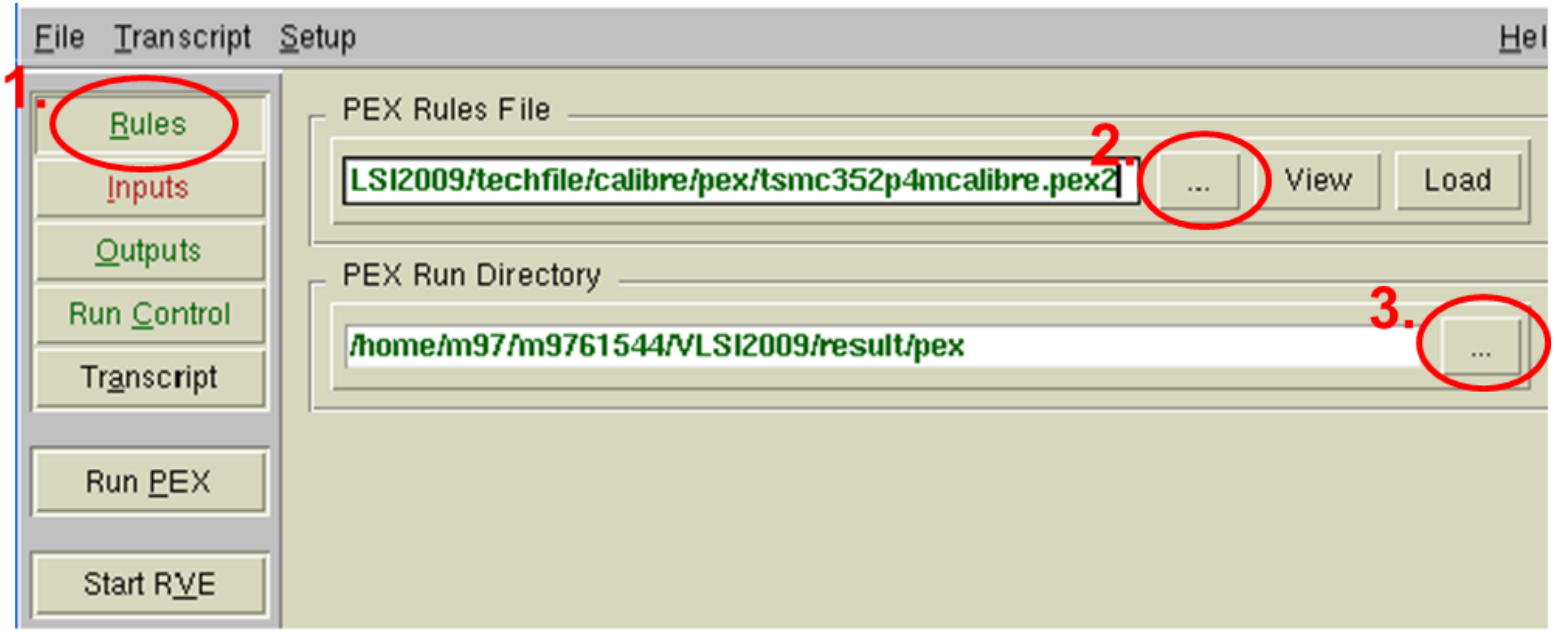
PEX STEP 1 – Run Calibre PEX

- After finished DRC, LVS check => Run PEX check
- Verify -> Calibre -> Run PEX



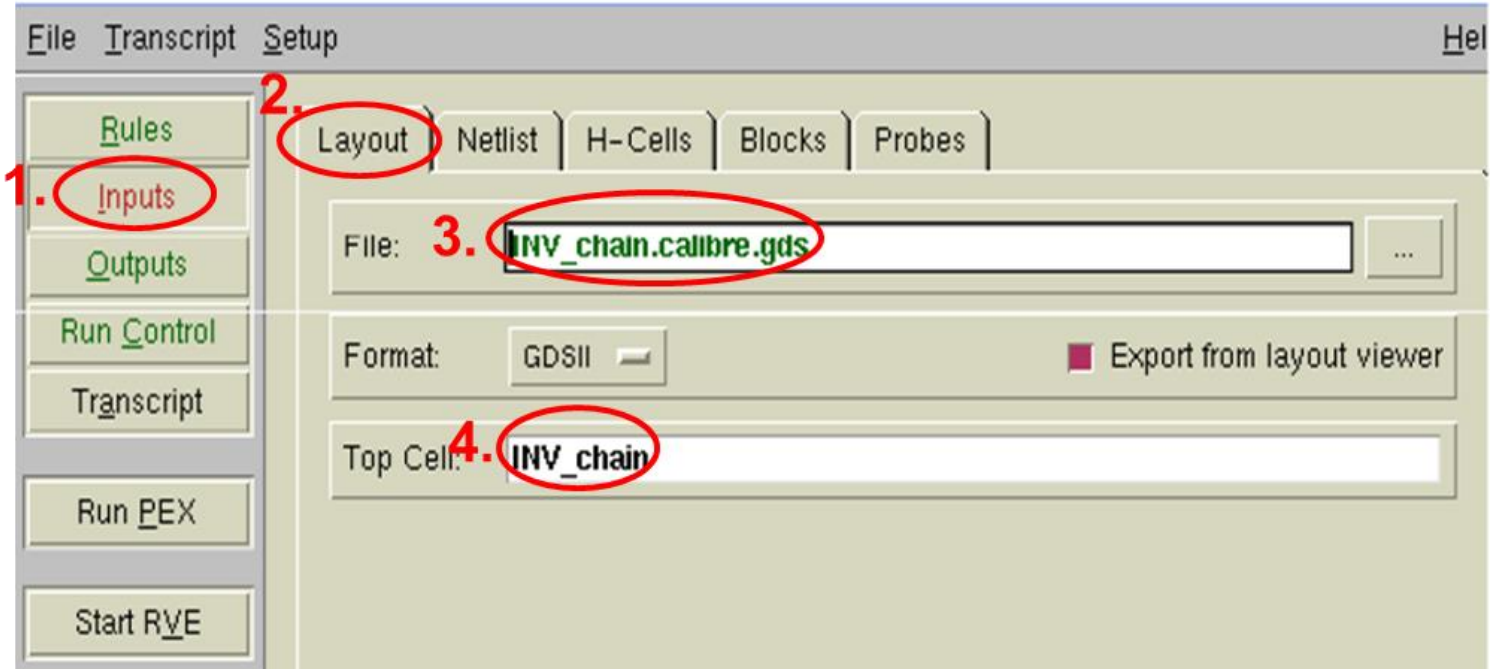
PEX STEP 2 – Choose Tech. file

- Rule -> PEX Rules file -> choose PEX command tech-file path
  - tsmc352p4mcalibre.pex2
- Rule -> PEX Run directory -> choose directory which extracted file which will be stored in
  - **XXX.spi, XXX.pxi, XXX.pex** will be generated after PEX



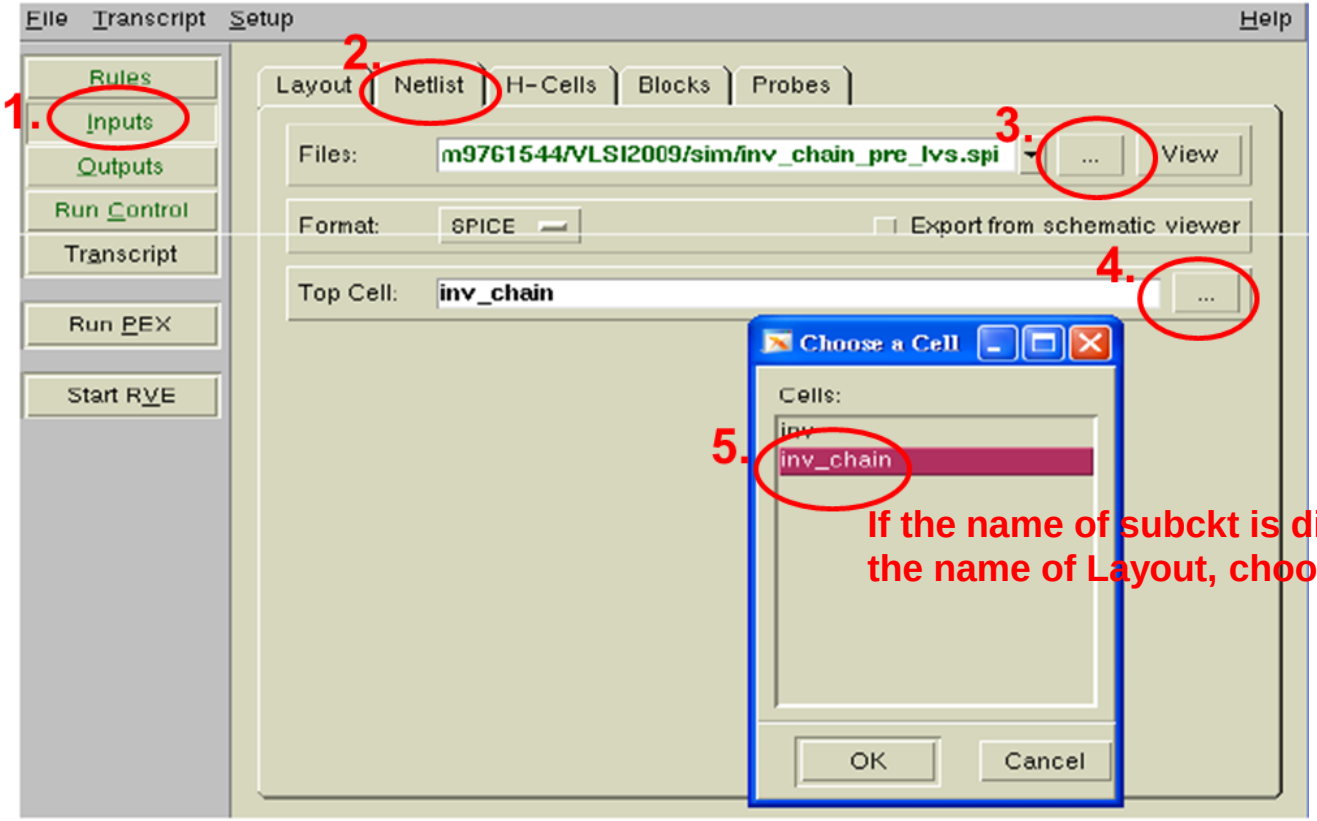
PEX STEP 3 – Input Layout setting

- Inputs -> Layout -> file
  - Choose layout file(.gds) (which is already passed DRC/LVS)
  - Choose Top Cell name



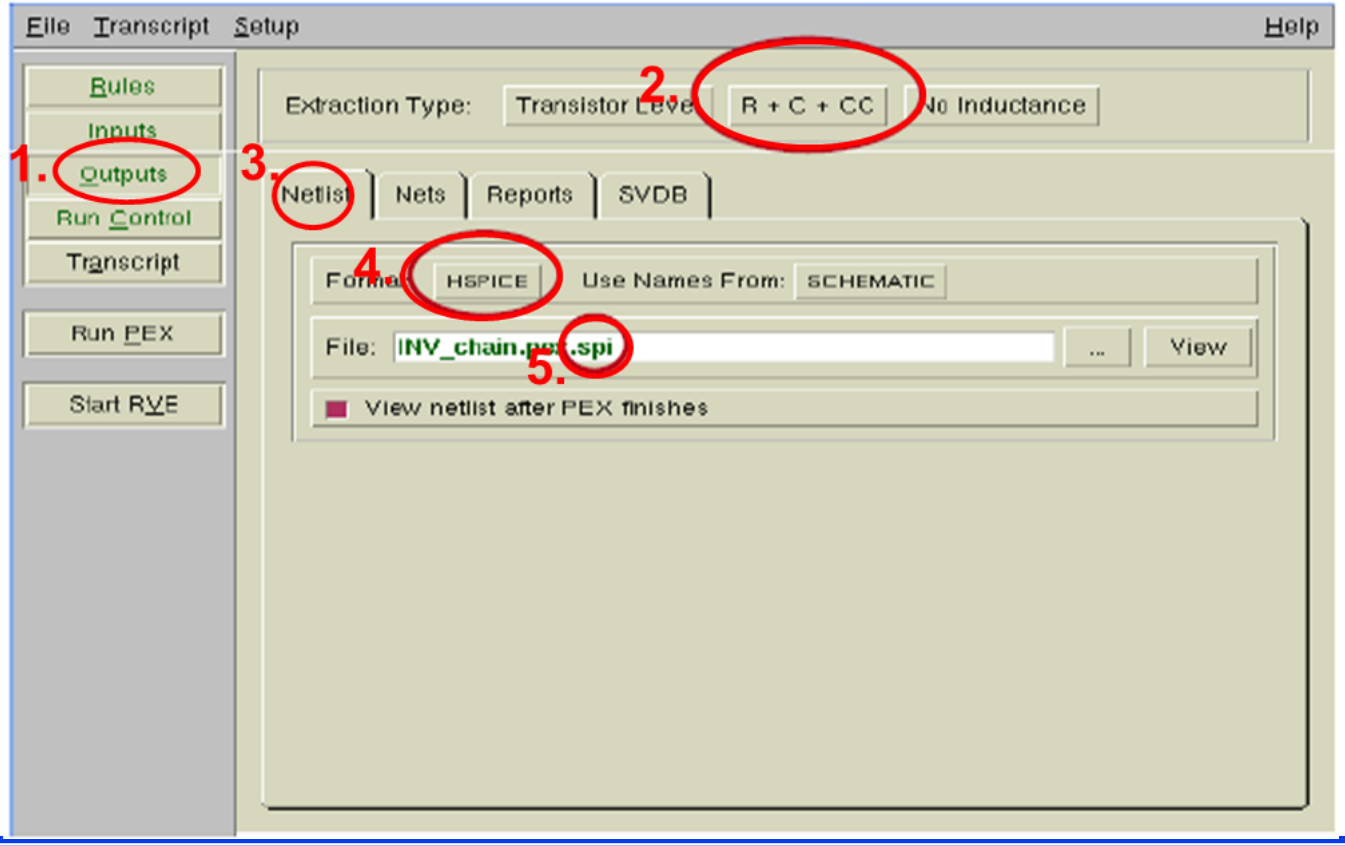
PEX STEP 4 – Input Netlist setting

- Inputs -> Netlist -> File
  - Choose Netlist file(.spi) (the same file using for LVS check)
  - Choose Top Cell name



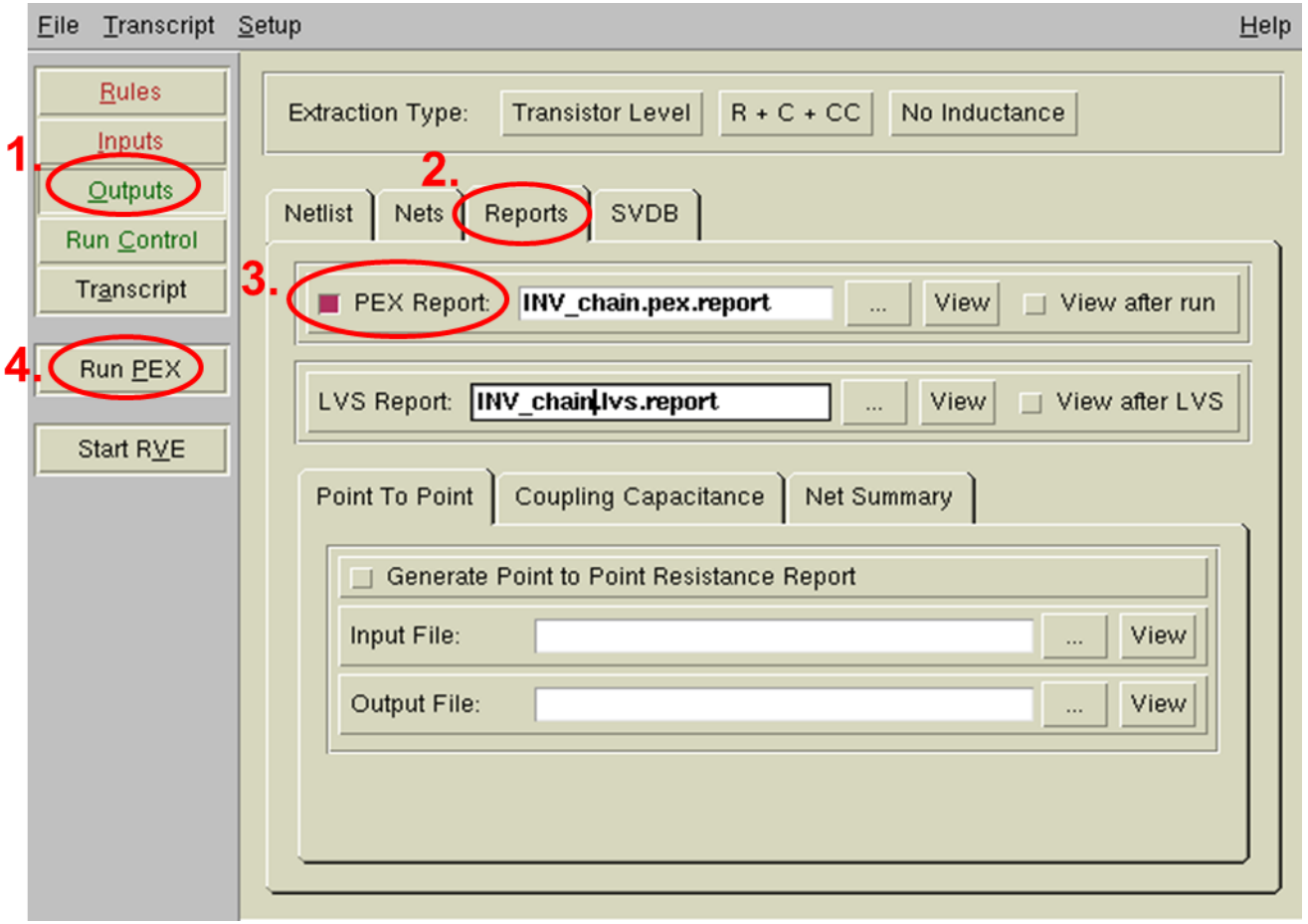
PEX STEP 5 – Output setting

- Outputs -> Extraction Type -> Choose **R+C+CC**
- Outputs -> Netlist -> Format -> Choose **HSPICE**
- Outputs -> Netlist -> File -> Change **XXX.pex.netlist** to **XXX.pex.spi**



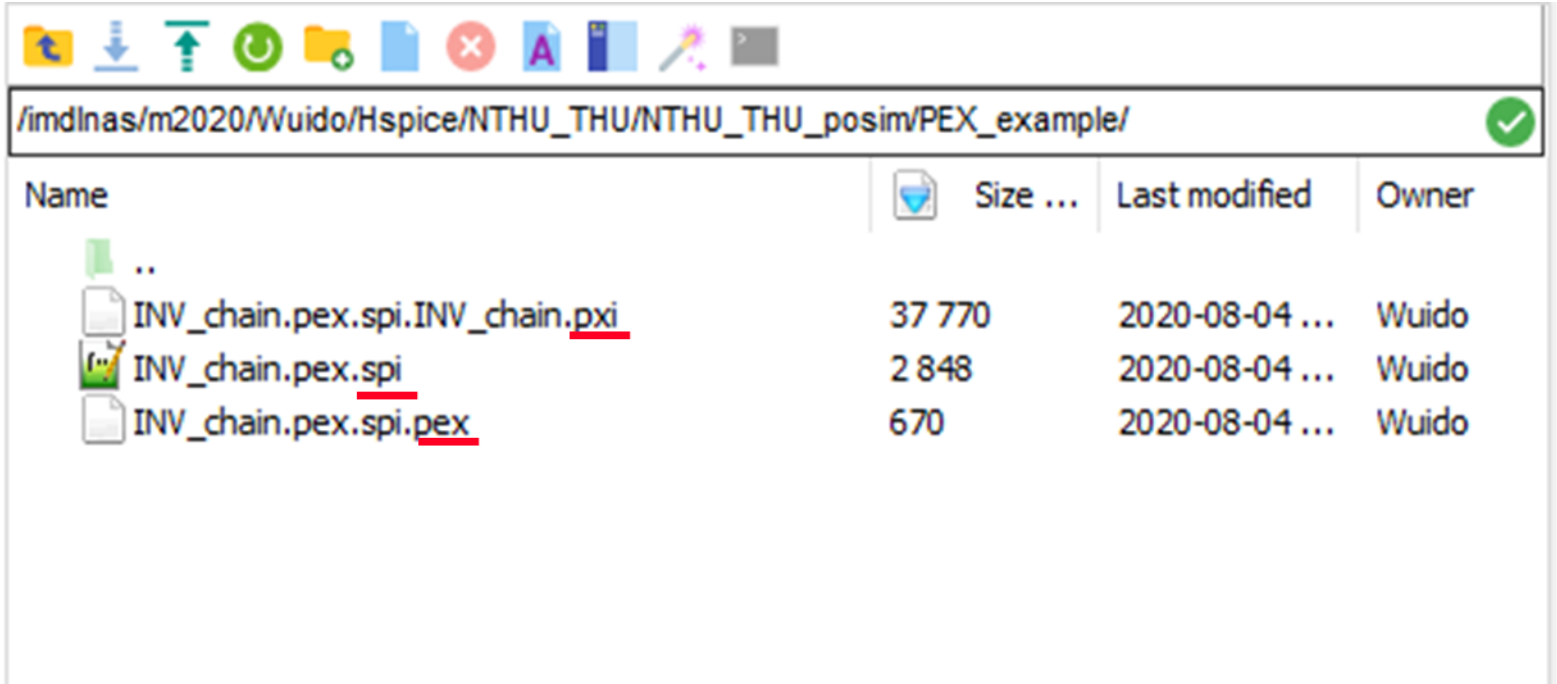
PEX STEP 6 – Output Report

- Outputs -> Reports -> PEX Report (Choice)



PEX STEP 7 – Output File

- PEX Finished -> three files will be generated after PEX
  - spi file: the new Netlist file consider parasitic effect
  - pex file: the file indicates the parasitic R+C between internode
  - pxi file: the file indicates the detail parasitic R+C of the circuit



Post-simulation

Post-sim

- Include .spi, .pxi, .pex file into Simulation File(.sp)
  - Change **original .spi file** to **extracted .spi file**

[without consider R+C]

```
.prot
.lib “cic018.l” TT
.temp 25
.unprot
.inc “INV_chain.spi”
.option post
x1 IN OUT VDD GND INV_chain
v1 VDD 0 1.8
v2 GND 0 0
.dc v3 0 1.8 0.01
.end
```

Simulation file (.sp) for **pre-sim**

[consider R+C]

```
.prot
.lib “cic018.l” TT
.temp 25
.unprot
.inc “INV_chain.pex.spi”
.option post
x1 IN OUT VDD GND INV_chain
v1 VDD 0 1.8
v2 GND 0 0
.dc v3 0 1.8 0.01
.end
```

Simulation file (.sp) for **po-sim**

Post-sim

- Sub-circuit ports order
  - Copy extracted .spi file sub-circuit **new** ports order to .sp file
  - Run HSPICE simulation

```
.prot
.lib “cic018.l” TT
.temp 25
.unprot
.inc “INV_chain.spi”
.option post
x1 IN OUT VDD GND INV_chain
v1 VDD 0 1.8
v2 GND 0 0
.dc v3 0 1.8 0.01
.end
```

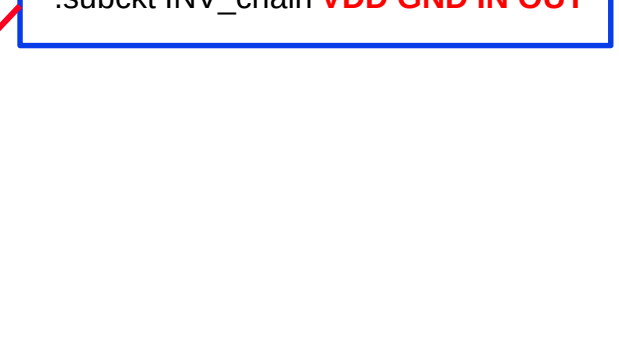
Simulation file (.sp) for **pre-sim**

```
.prot
.lib “cic018.l” TT
.temp 25
.unprot
.inc “INV_chain.pex.spi”
.option post
x1 VDD GND IN OUT INV_chain
v1 VDD 0 1.8
v2 GND 0 0
.dc v3 0 1.8 0.01
.end
```

Simulation file (.sp) for **po-sim**

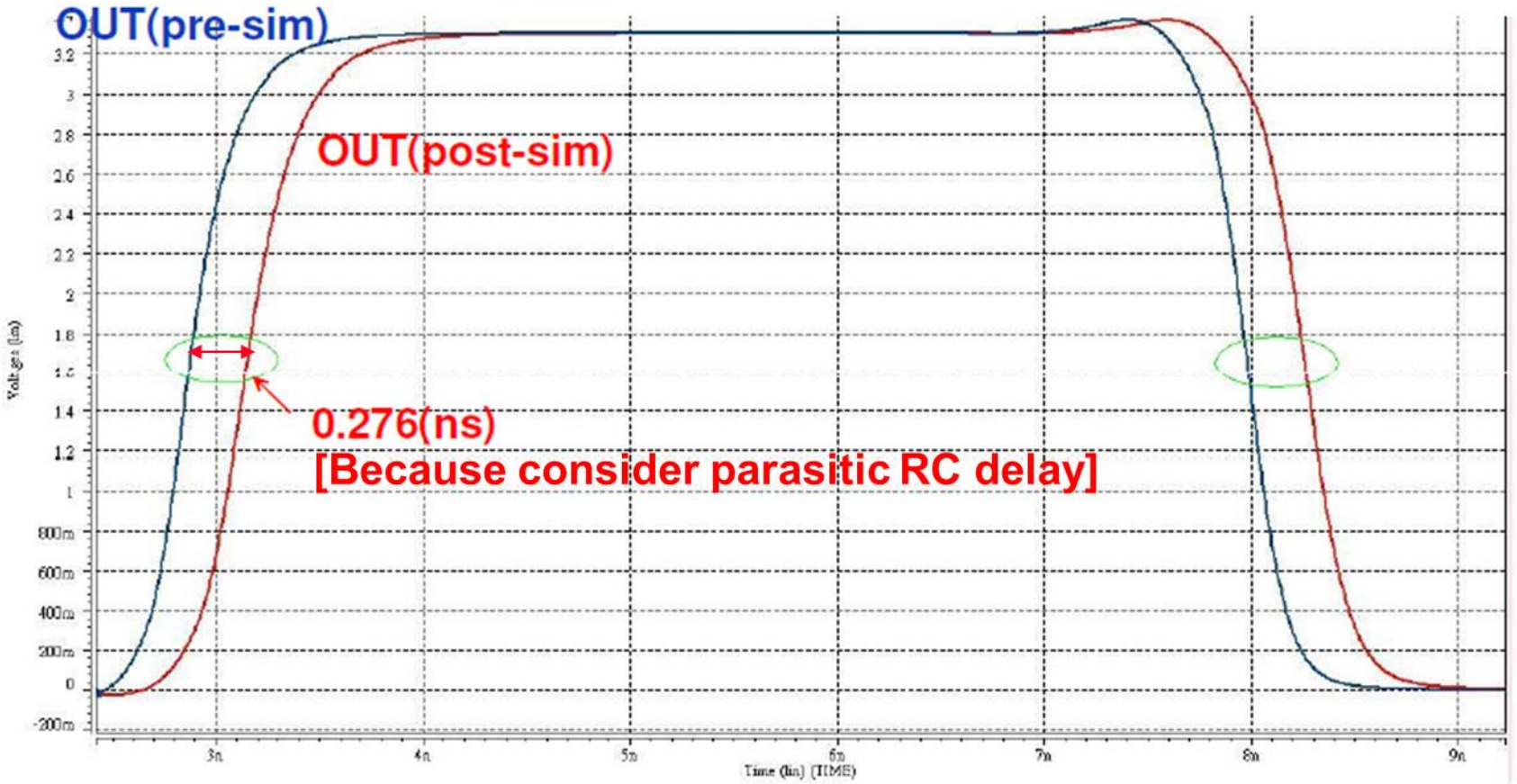
INV_chain.pex.spi

```
.include "INV_chain.pex.spi.pex“
.subckt INV_chain VDD GND IN OUT
```



Post-sim result

- slew_rate from 5.000e-10 to 5.658e-10
- delay_time from 1.824e-09 to 2.100e-09 **Δdelay_time = 0.276(ns)**



Have a nice job!