積體電路設計導論

Laker Tutorial

Date: 2022/10/04

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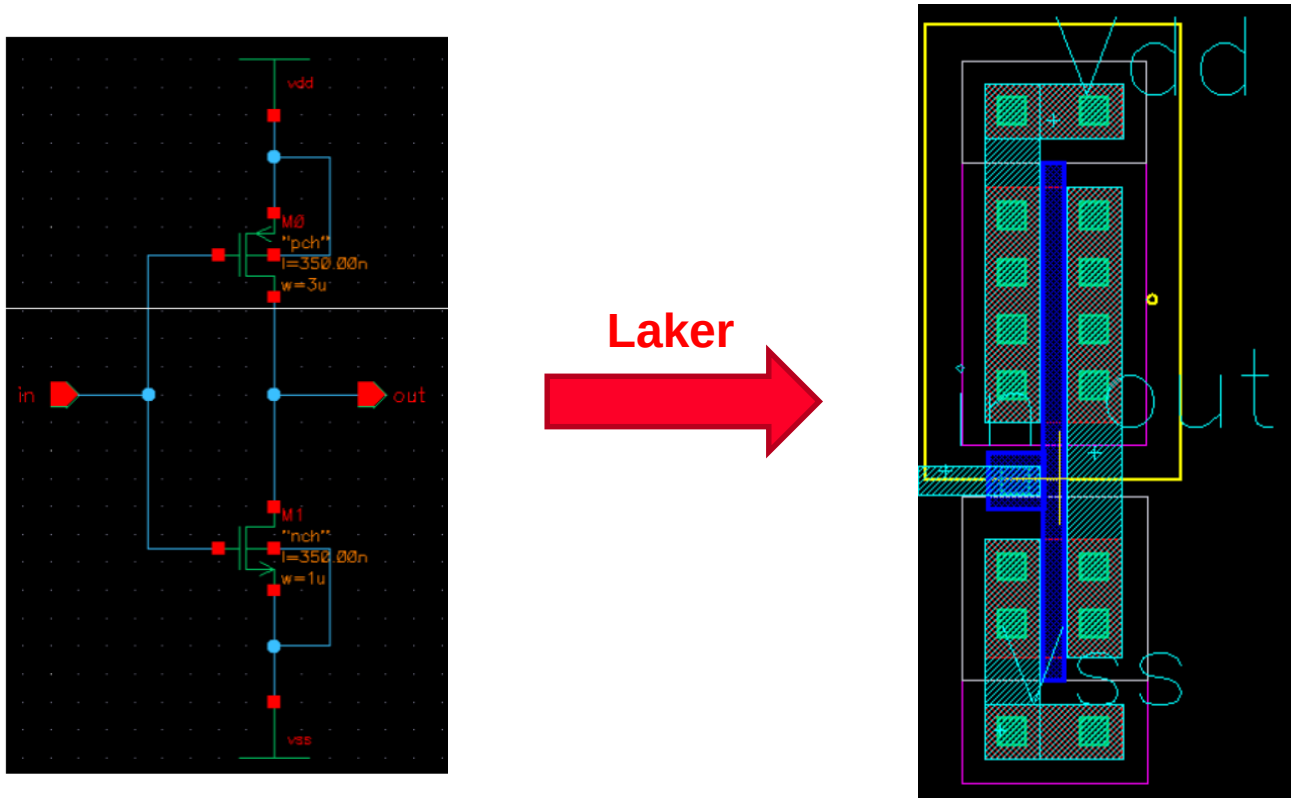
Outline

- What is Laker?
- File Requirement
- Environment Setting
- Hot Key
- Process v.s. Layout
- Multiply the Width
- Calibre DRC Flow
- Calibre LVS Flow
- Export / Import Design

What is Laker?

- **Laker** is a tool which enable user to generate layout results so that we can ask the Fab (Ex: TSMC) to make a Custom IC.



File Requirement

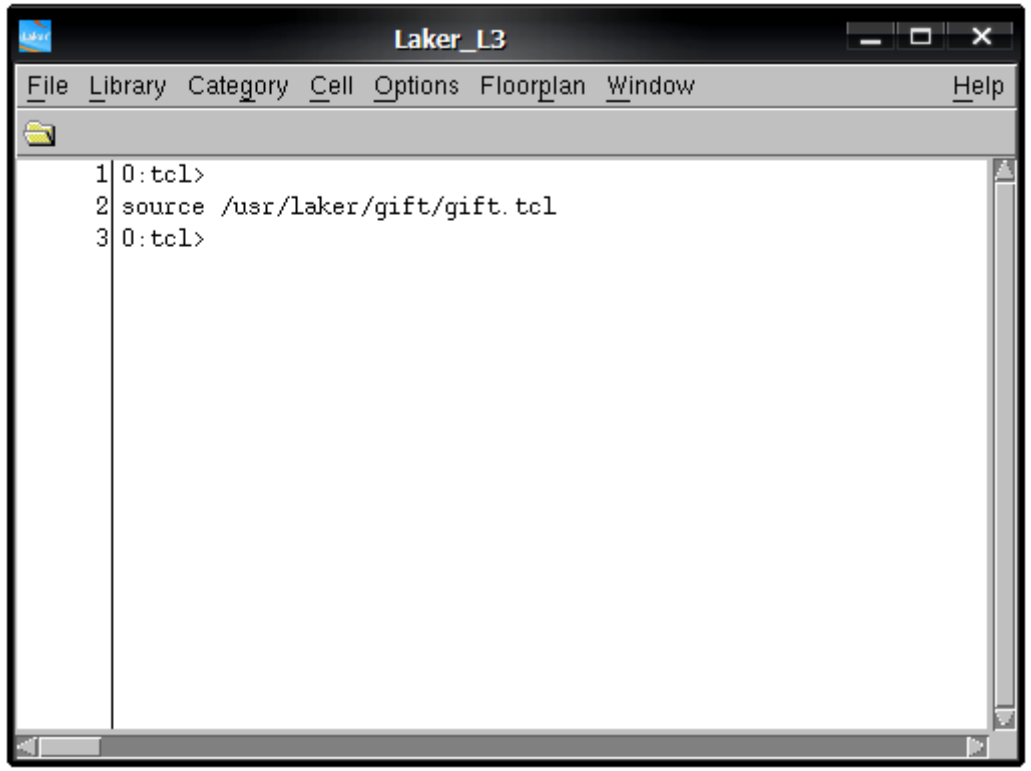
File Requirement

- Netlist : *.spi
  - The *.spi file you want to transfer to layout
- Technology file : laker.tf
  - The process information (EX: 0.18u, 65nm, 28nm …)
- DRC file : rule.drc
  - To check if the layout violates fabrication rule
- LVS file : Rule.lvs
  - To check whether layout and schematic are the same

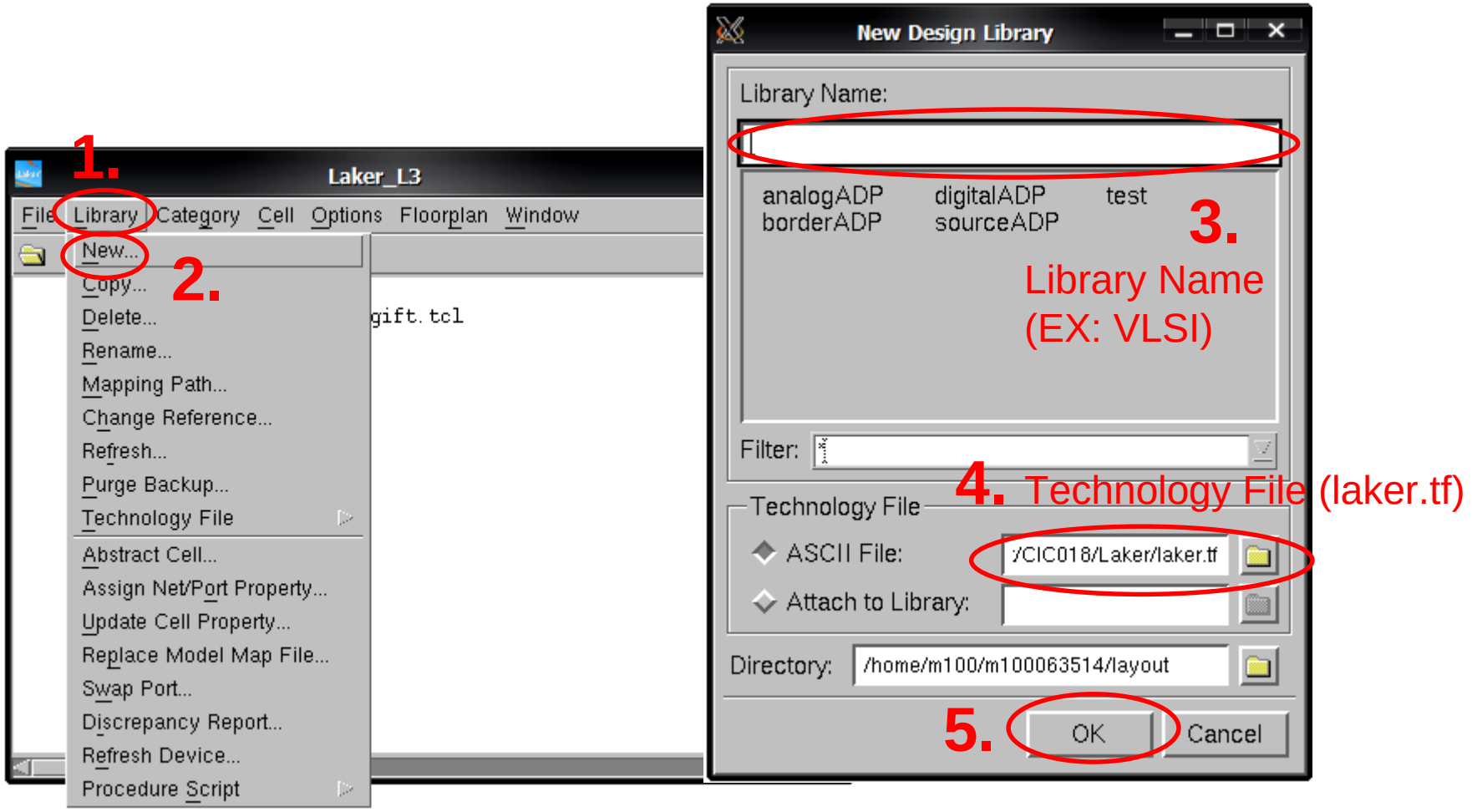
Environment Setting

Laker - Initialize

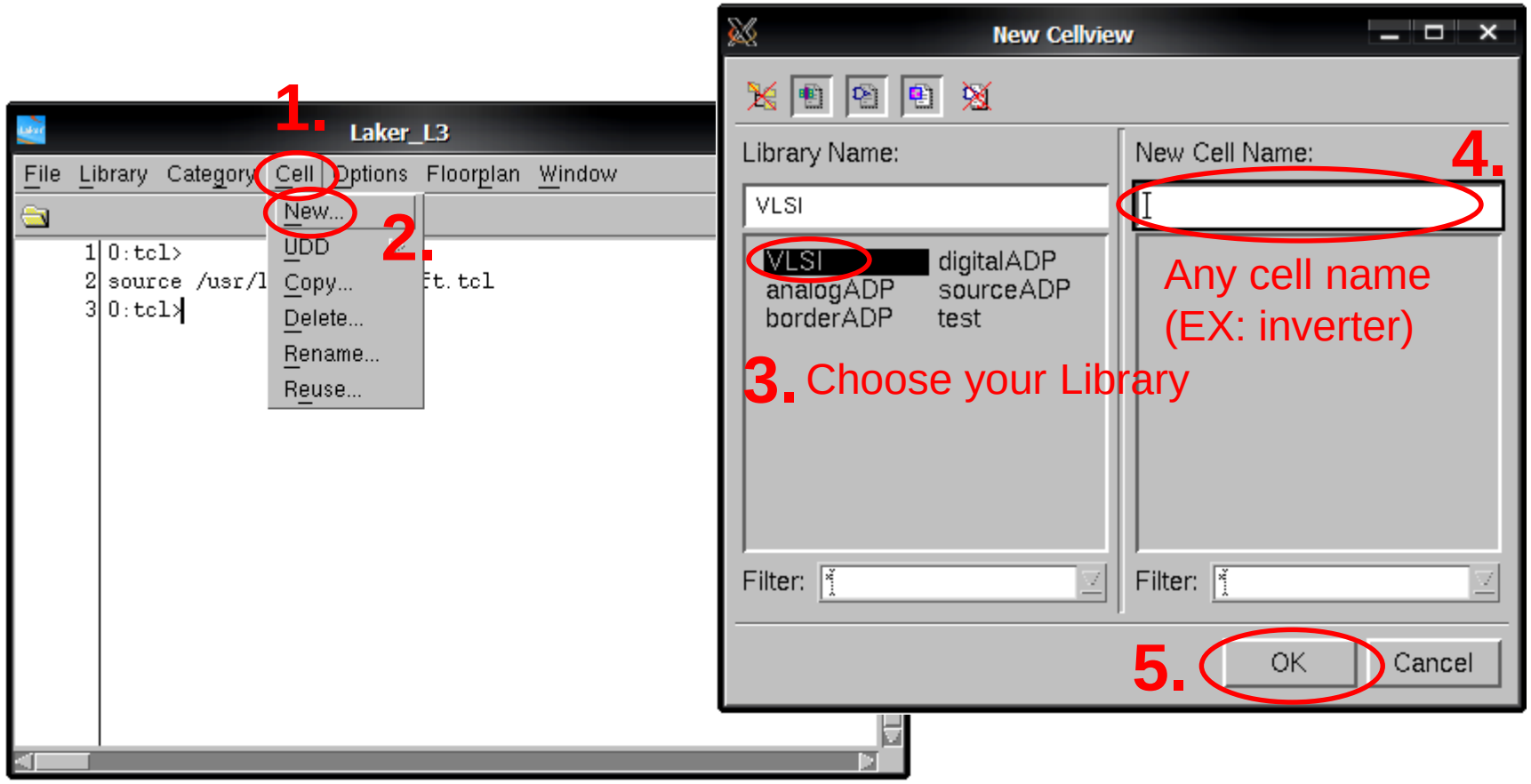
- source /usr/cadtool/user_setup/08-laker.csh
- Create a layout directory by “mkdir ”
- Type the command “laker &” in terminal
- Main Window



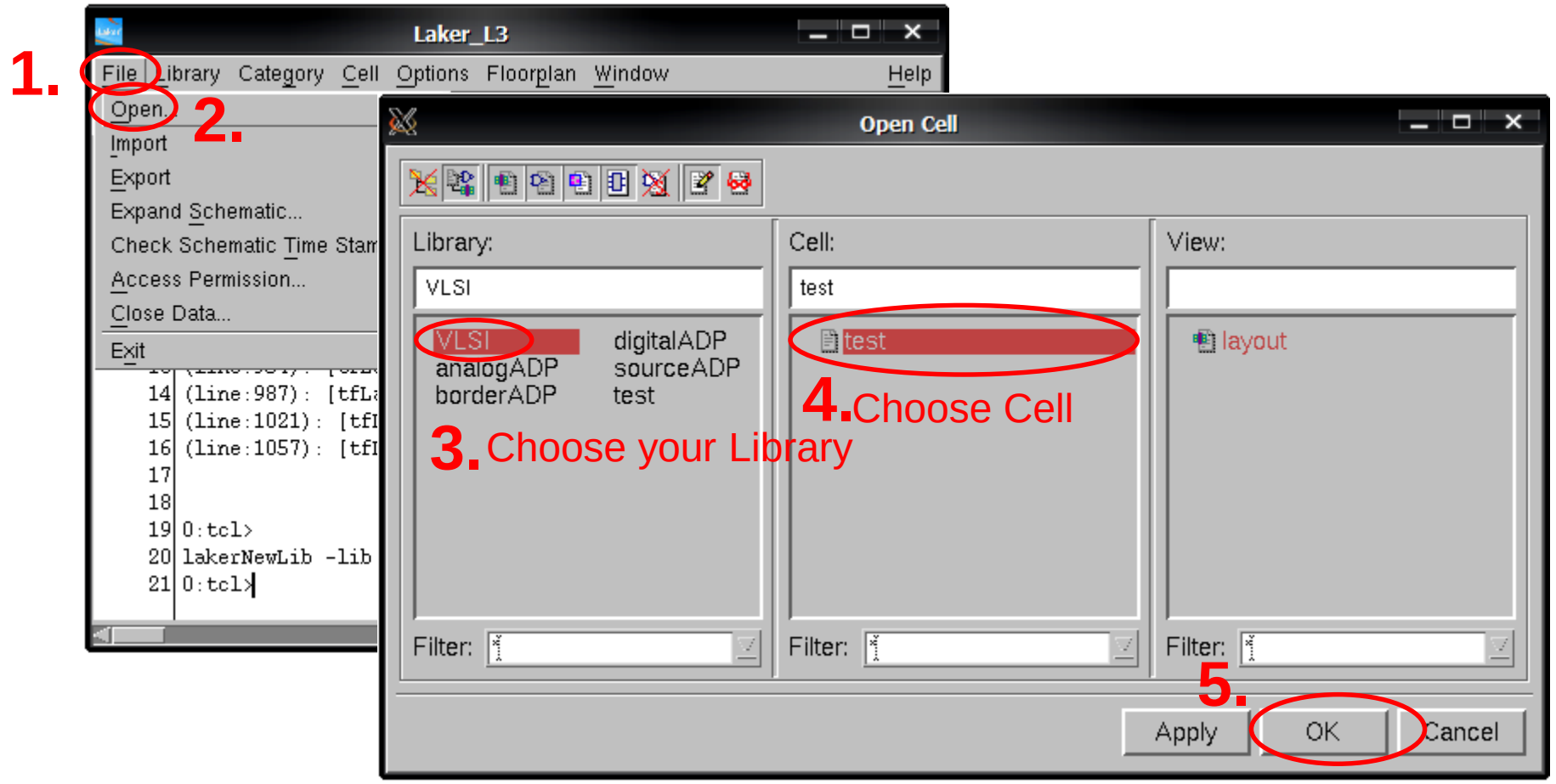
Laker – Create New Library



Laker – Create New Cell

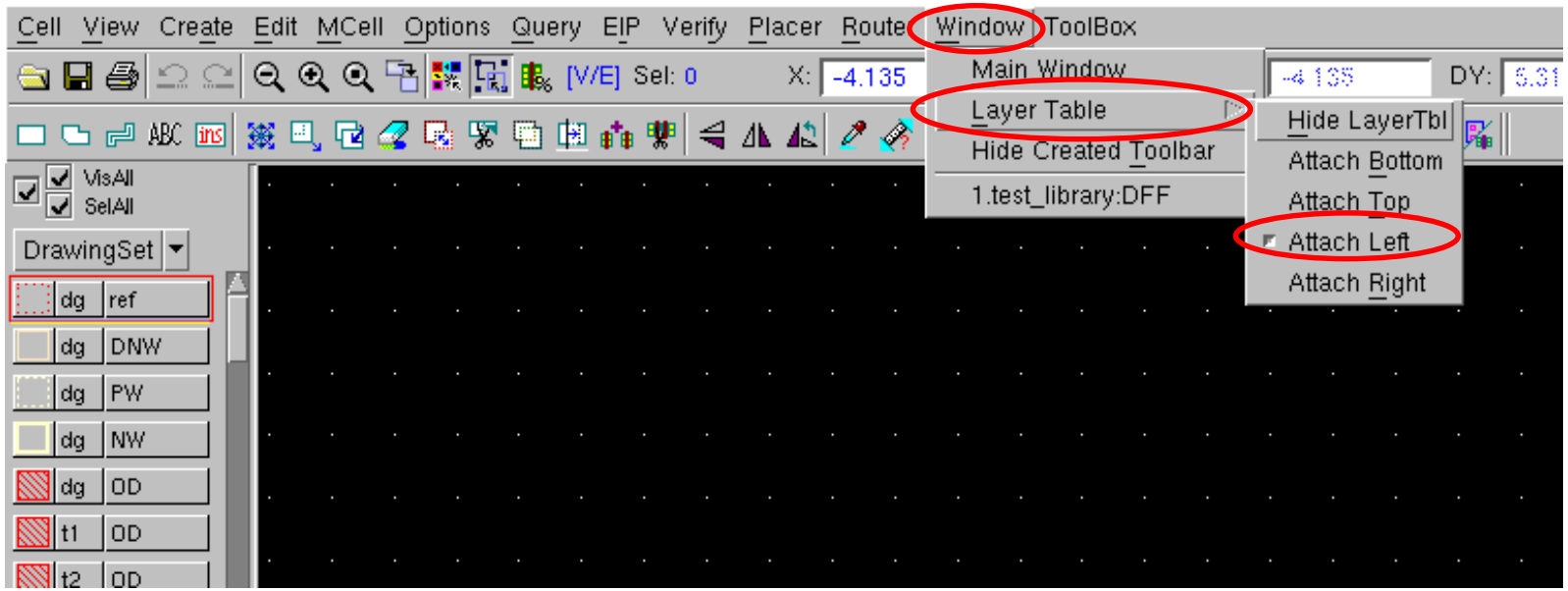


Laker – Open Cell



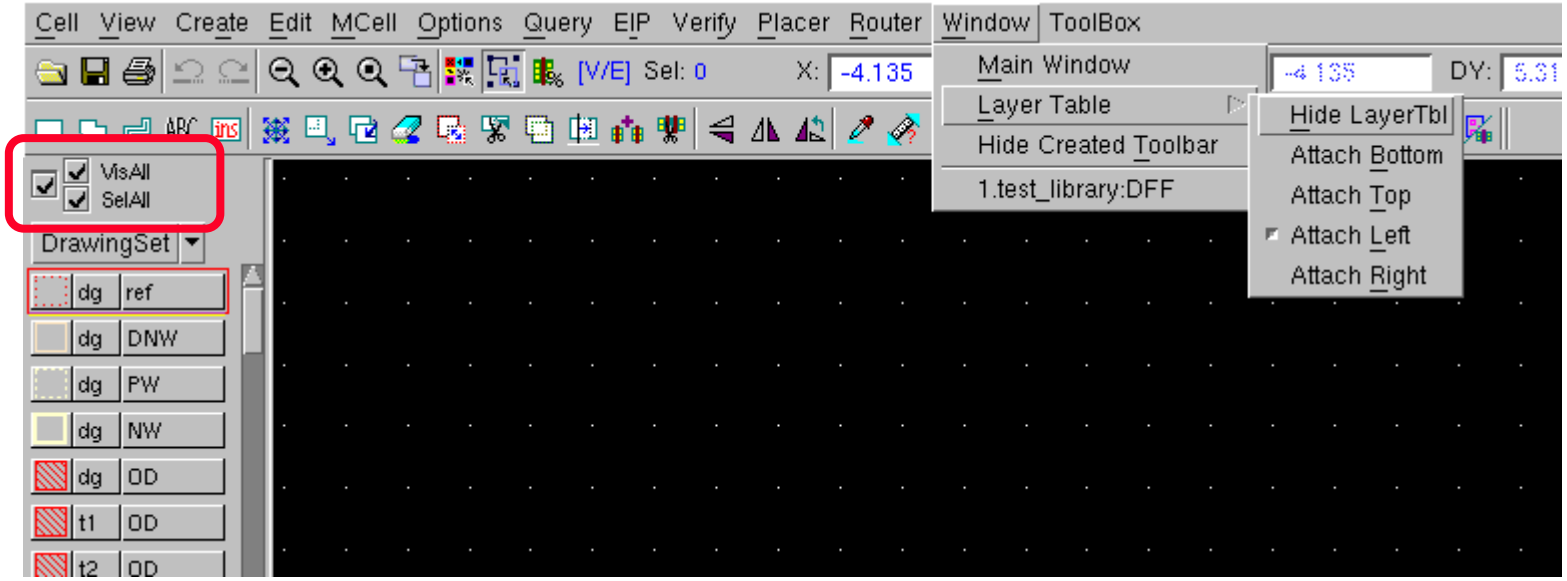
Laker – Editor

- Window → Layer Table → Attach Left
  - Don’t select “Hide Created ToolBar”



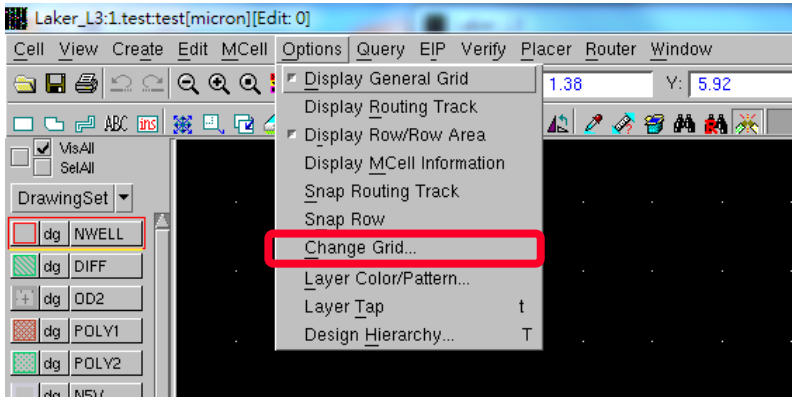
Laker – Editor

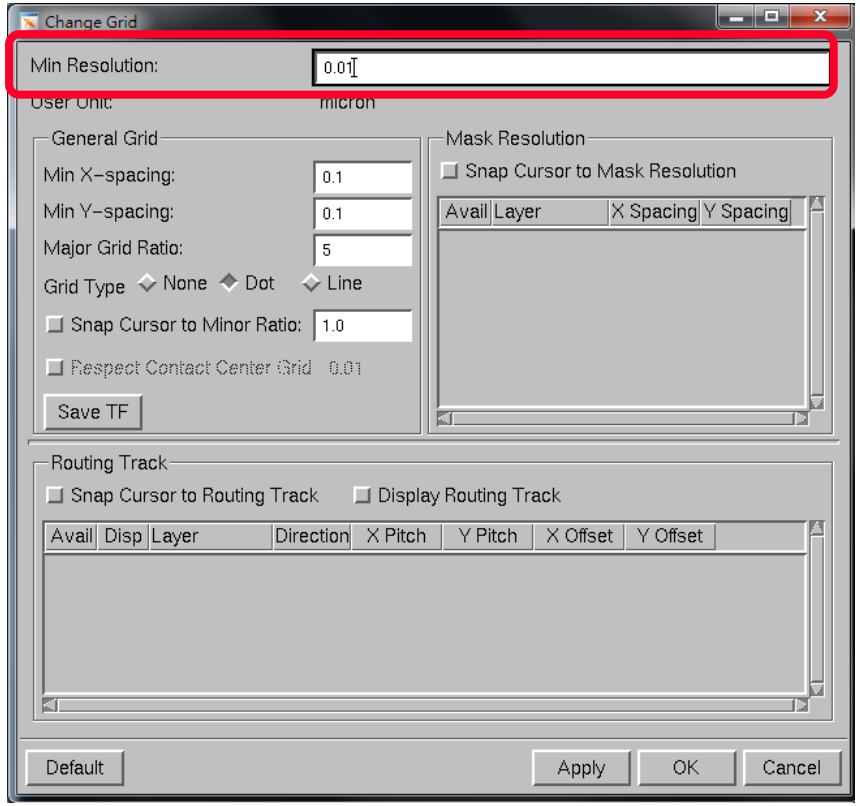
- Selectable and Visible
  - Visible : You can see those materials
  - Selectable : You can use those materials



Laker – Grid

- Change Resolution
  - Check at “Option → Change Grid”
  - Min Resolution = 0.01





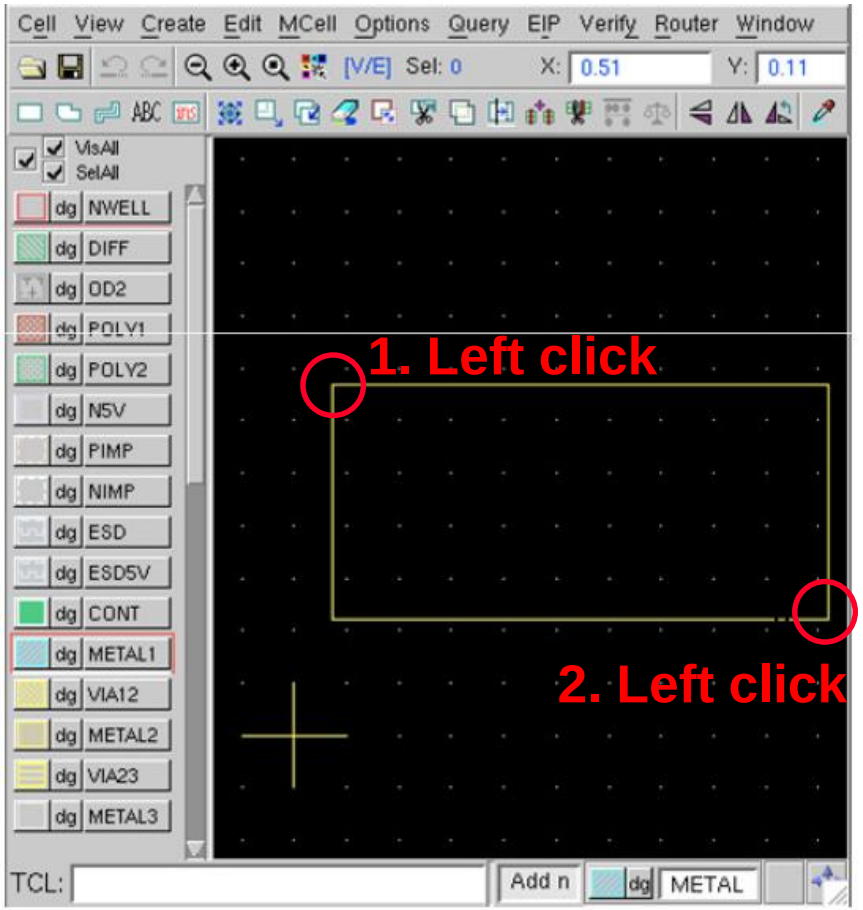
Hot Key

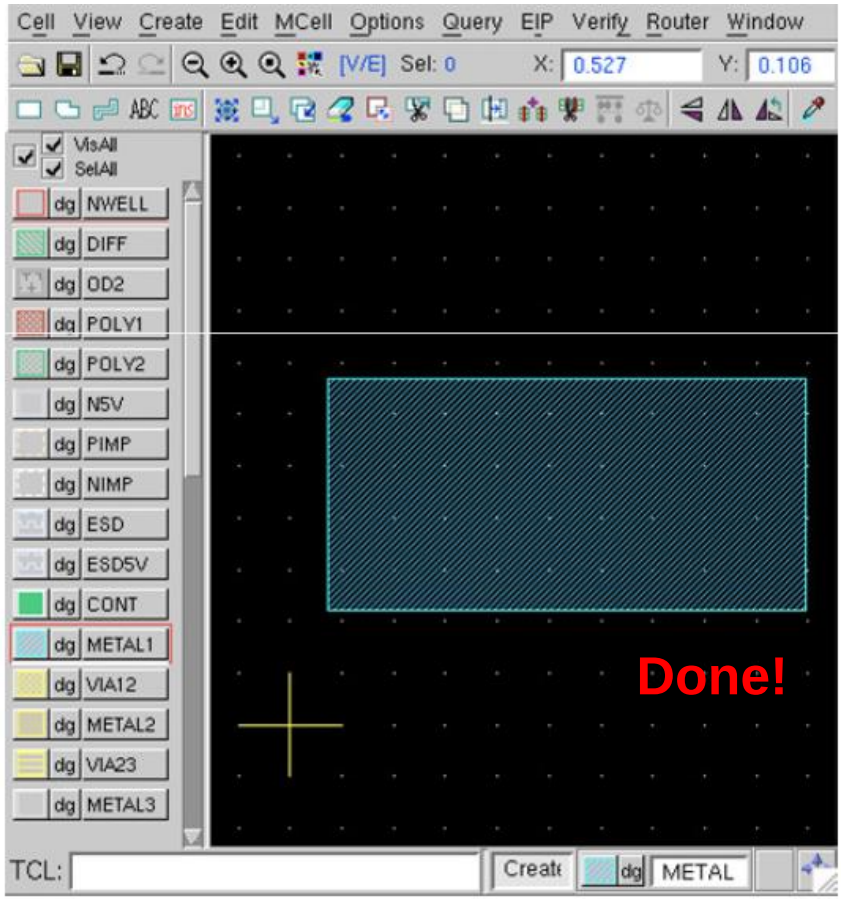
Laker – Hot Key Table

Hot Keys	Attitude	Hot Keys	Attitude
R	Rectangular	**P**	Path
S	Stretch	**Z**	Zoom area
M	Move	**ctrl/shift+z**	zoom in/out
C	Copy	**D**	Distance
Del	Delete	**K/shift+K**	Marker / Remove all Markers
Q	Quality	**I**	Instance
Esc	Release attitudes	**A**	Align
u/shift+u	Undo / redo		

Laker – (R)ectangular

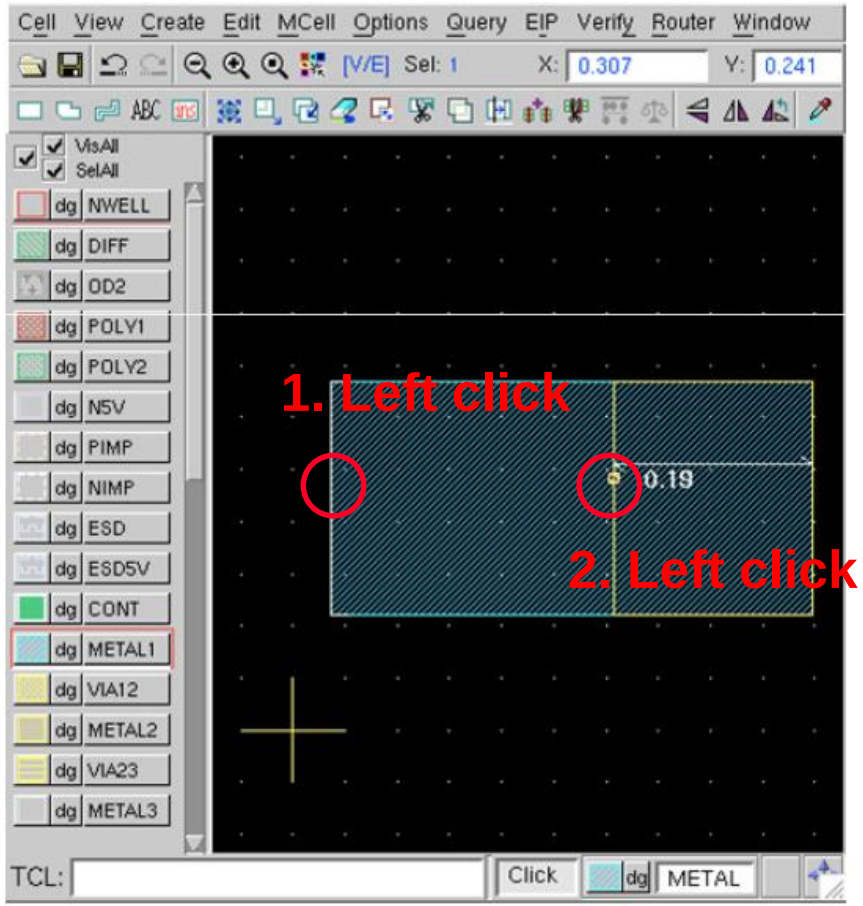
- Draw Rectangular (R)
  - Choose a material → Press r → point ref. → point dest.

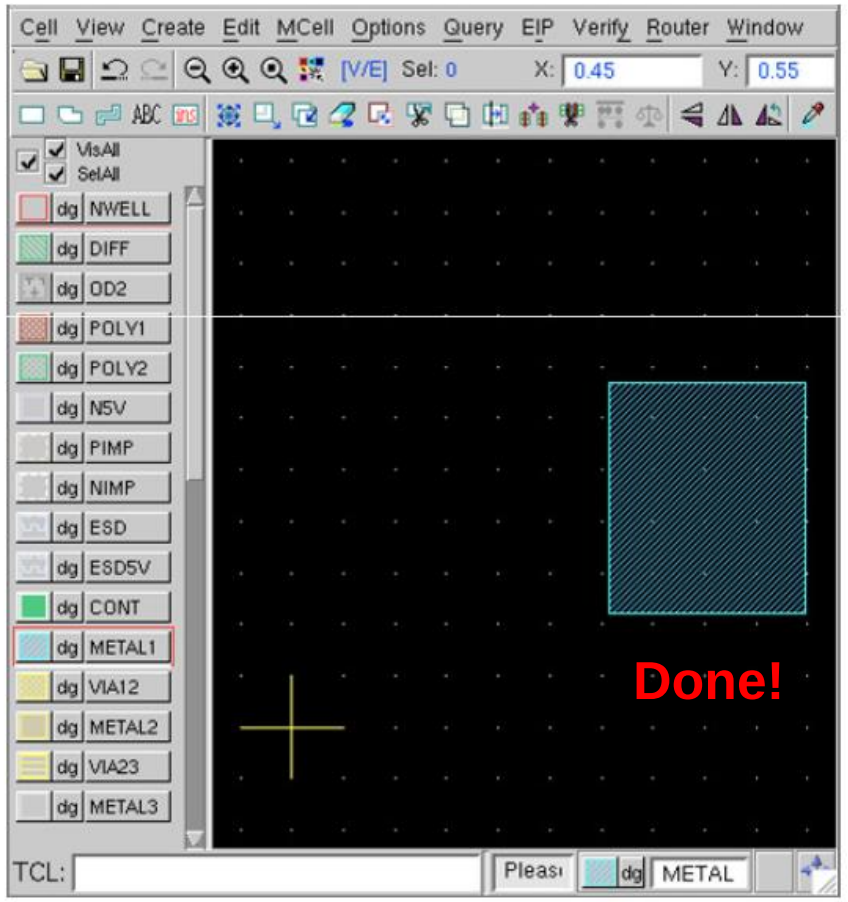




Laker – (S)tretch

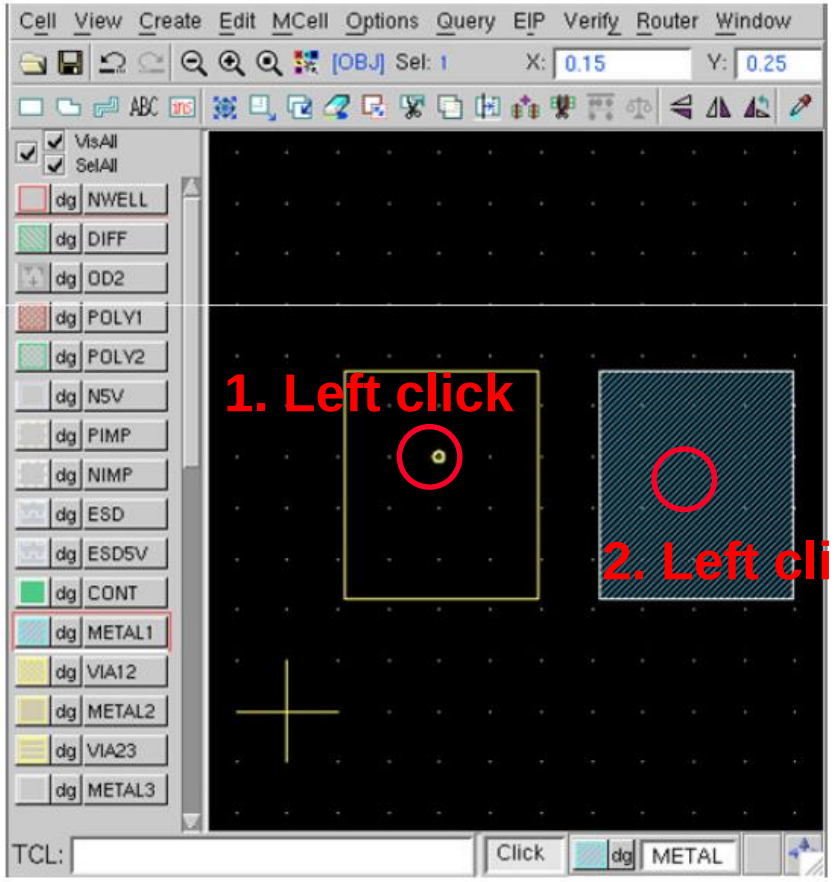
- Stretch (s)
  - Press s → select edge → point ref. → point dest.

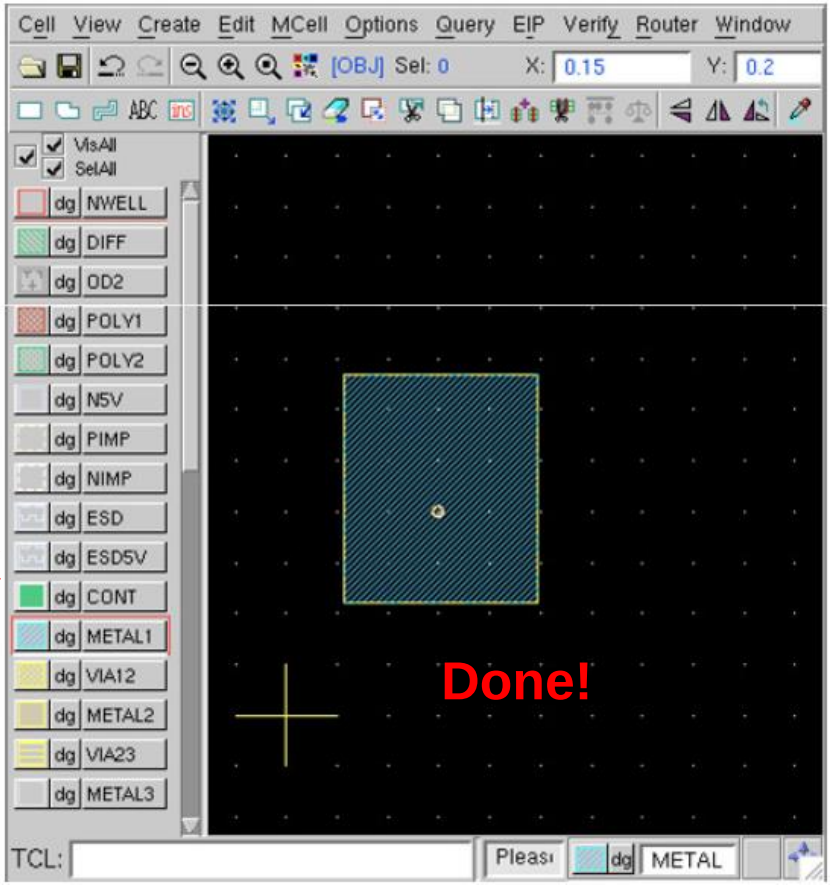




Laker – (M)ove

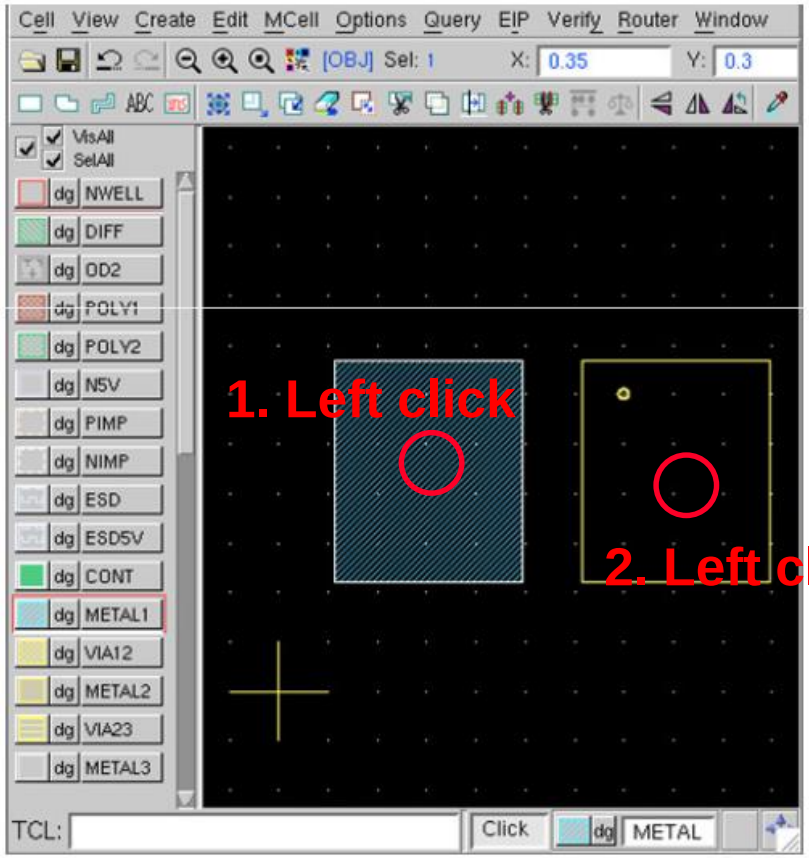
- Move (m)
  - Press m → select figure → point ref. → point dest.

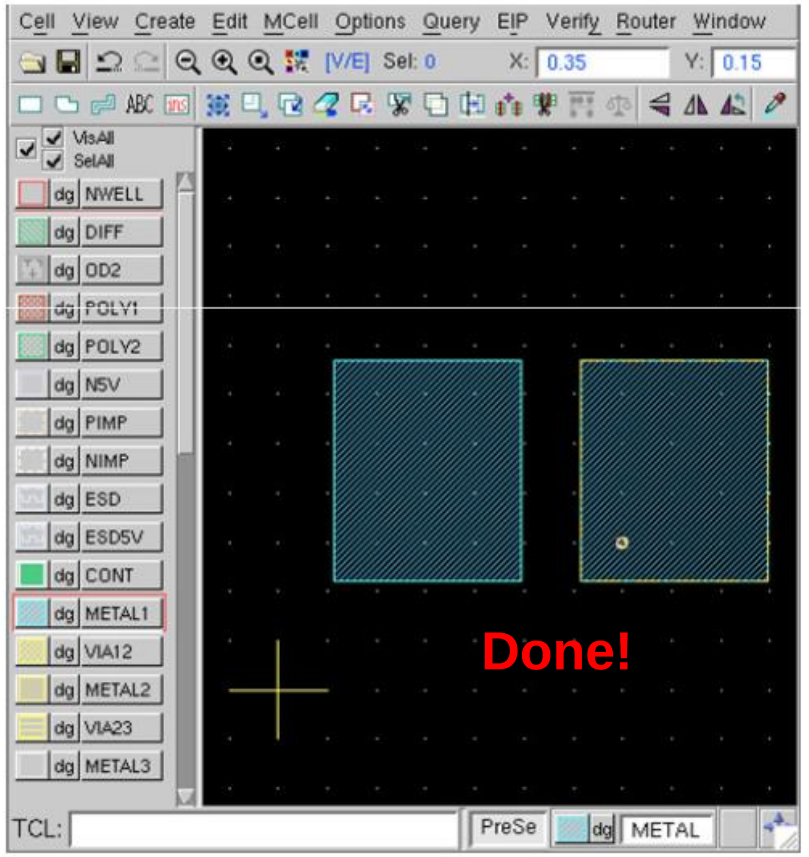




Laker – (C)opy

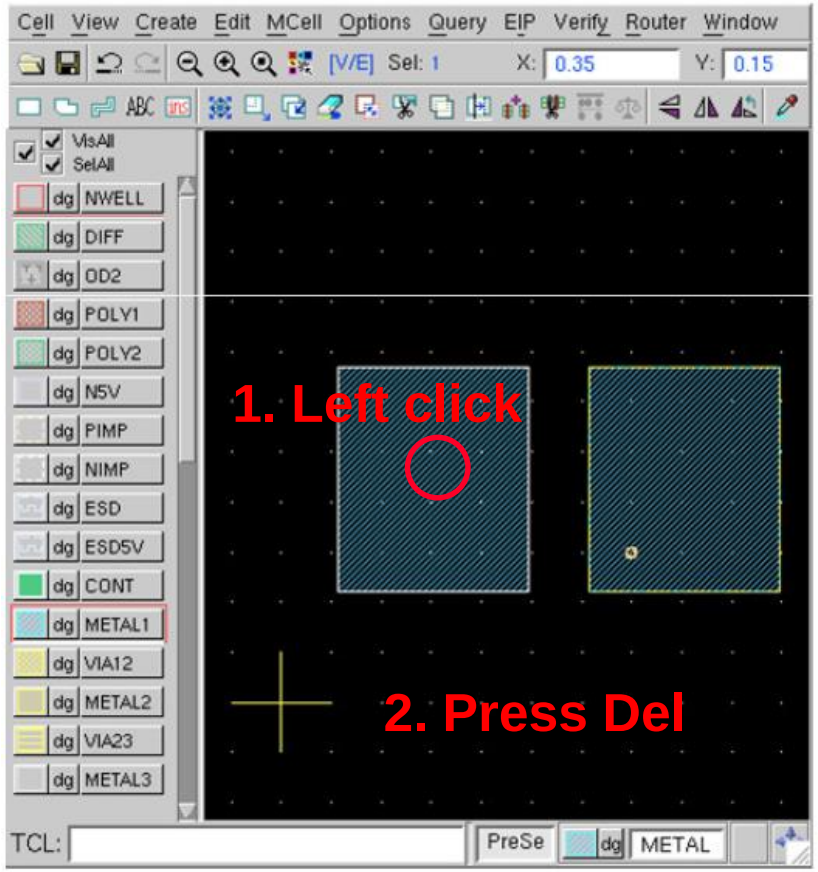
- Copy (c)
  - Press c → select figure → point ref. → point dest.

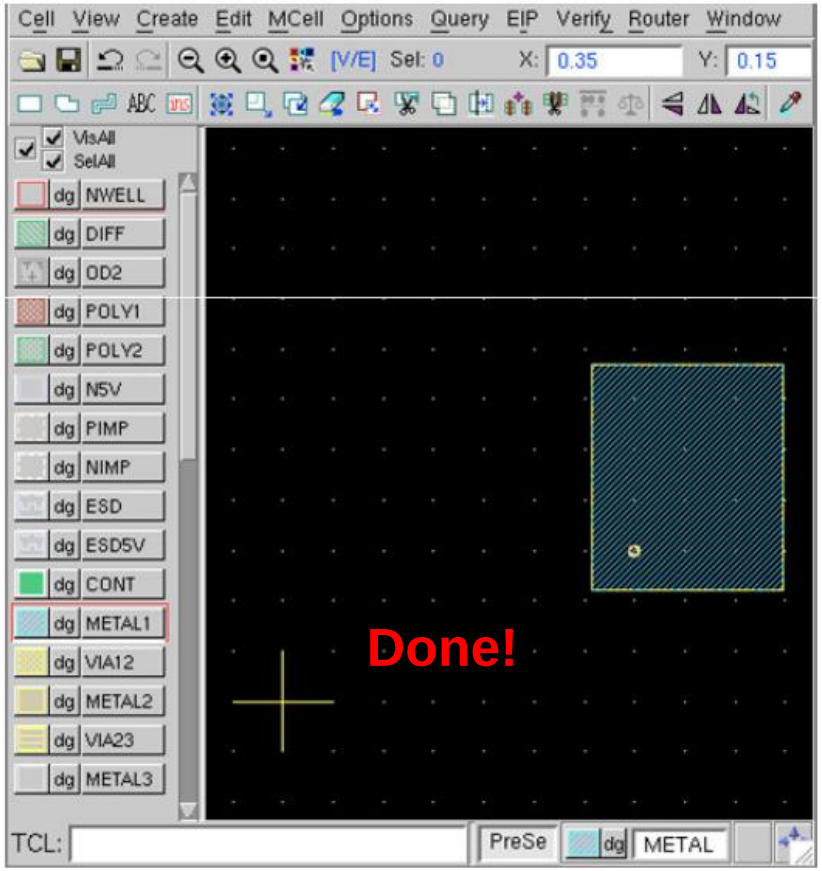




Laker – (Del)ete

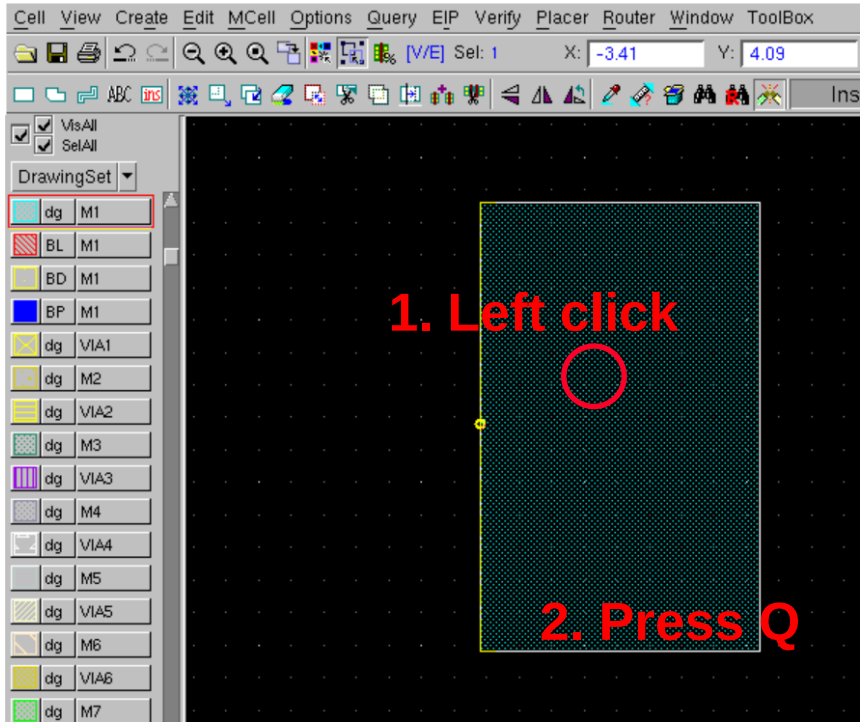
- Delete (Del)
  - Select figure → press Del

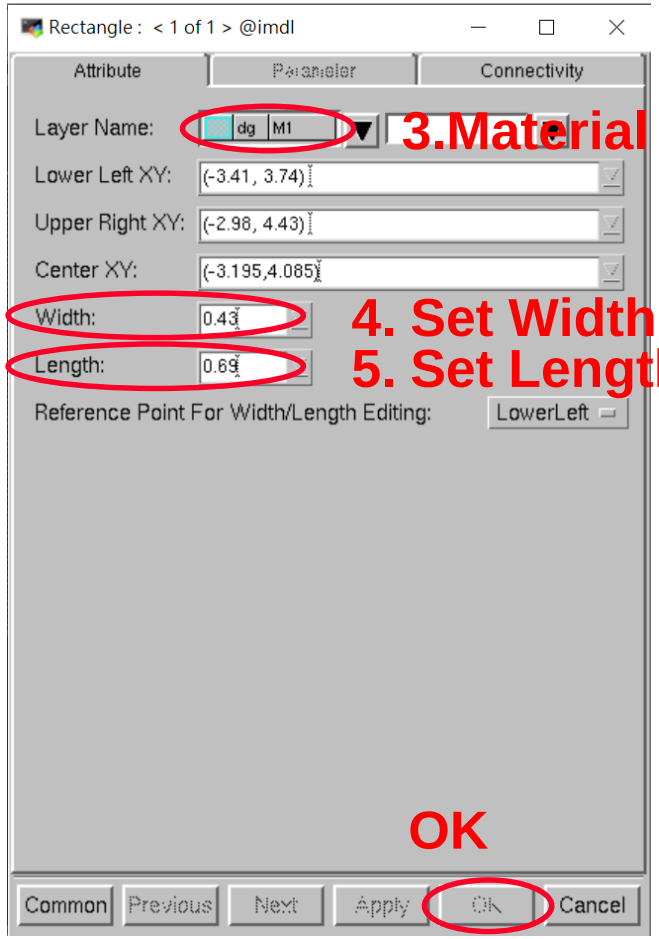




Laker – (Q)uality

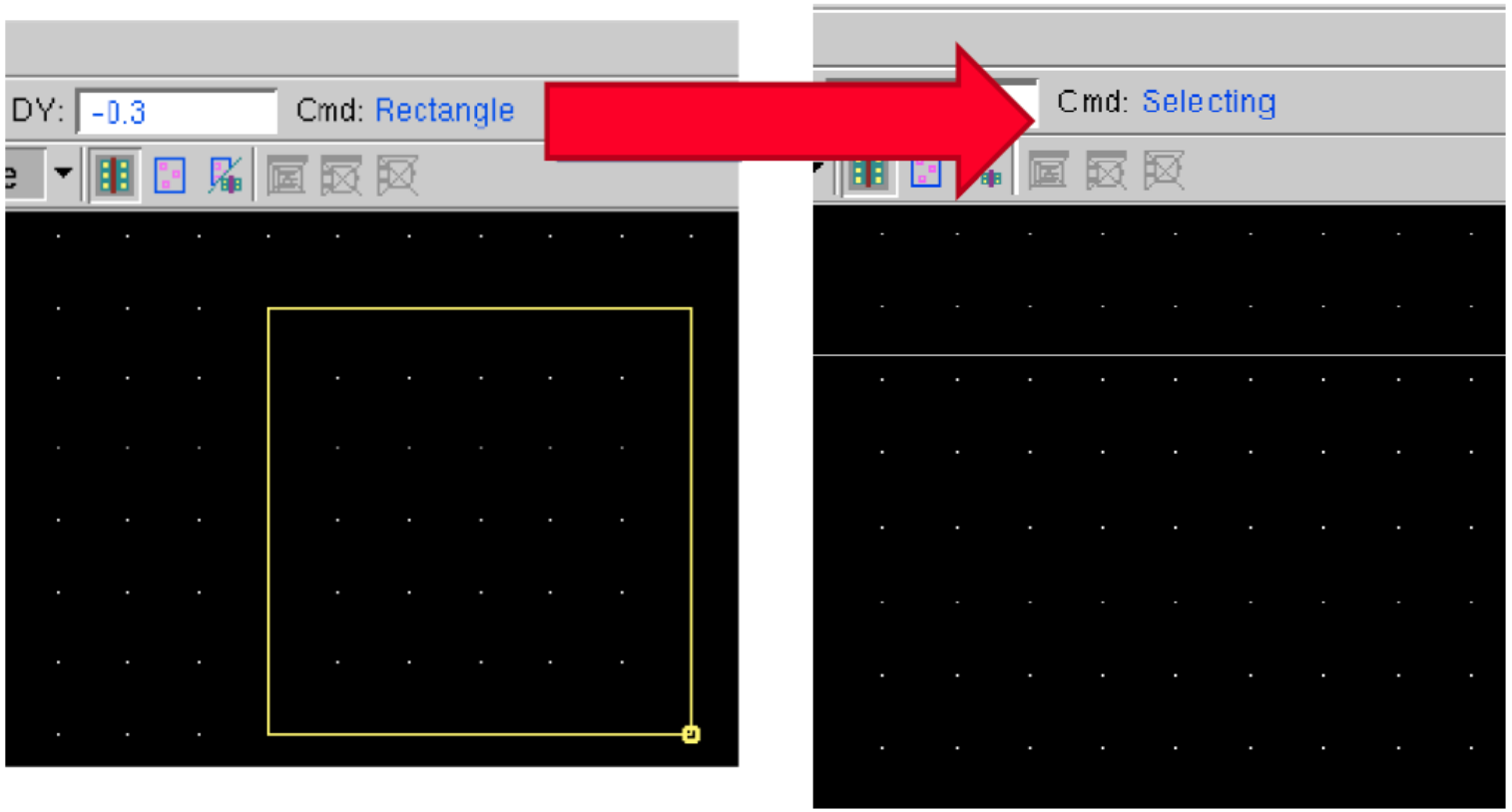
- Quality (Q)
  - Select figure → press Q → Edit



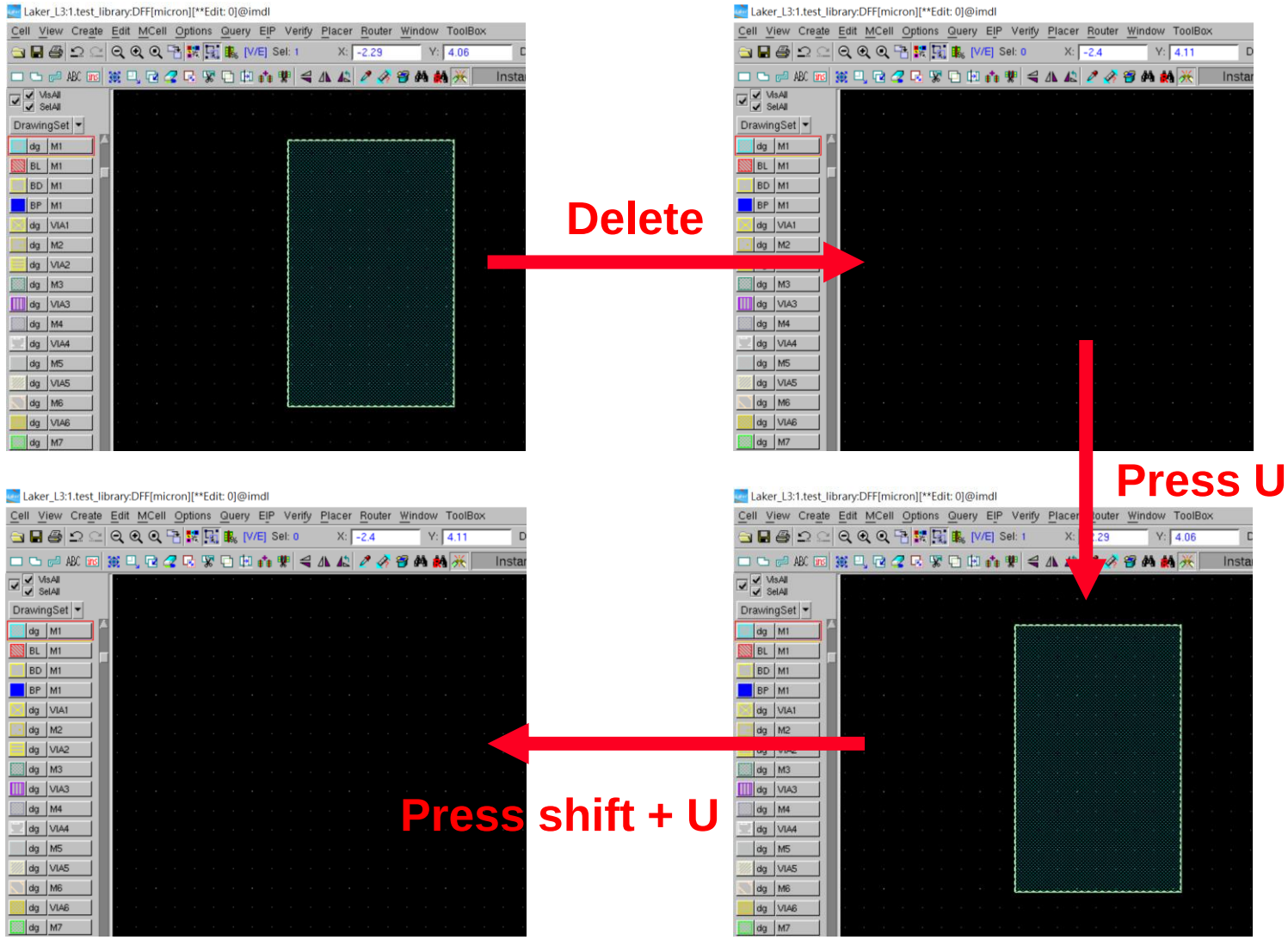


Laker – (Esc)ape

- Release from Attitude (Esc)
  - Press after every operation (Good habit)

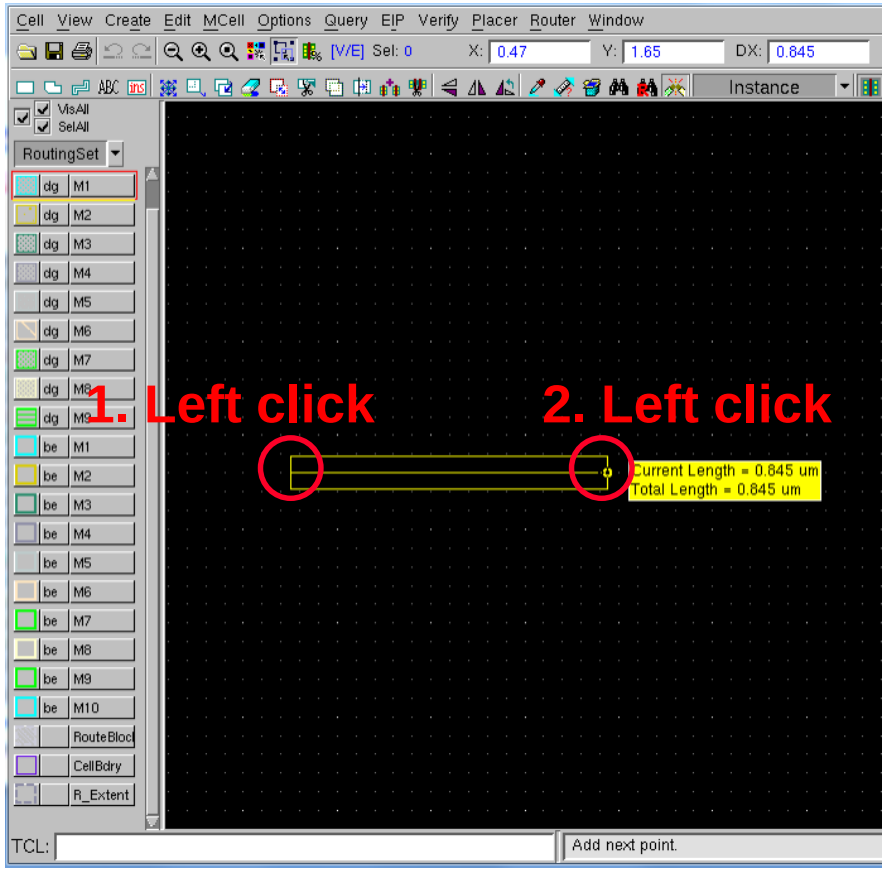


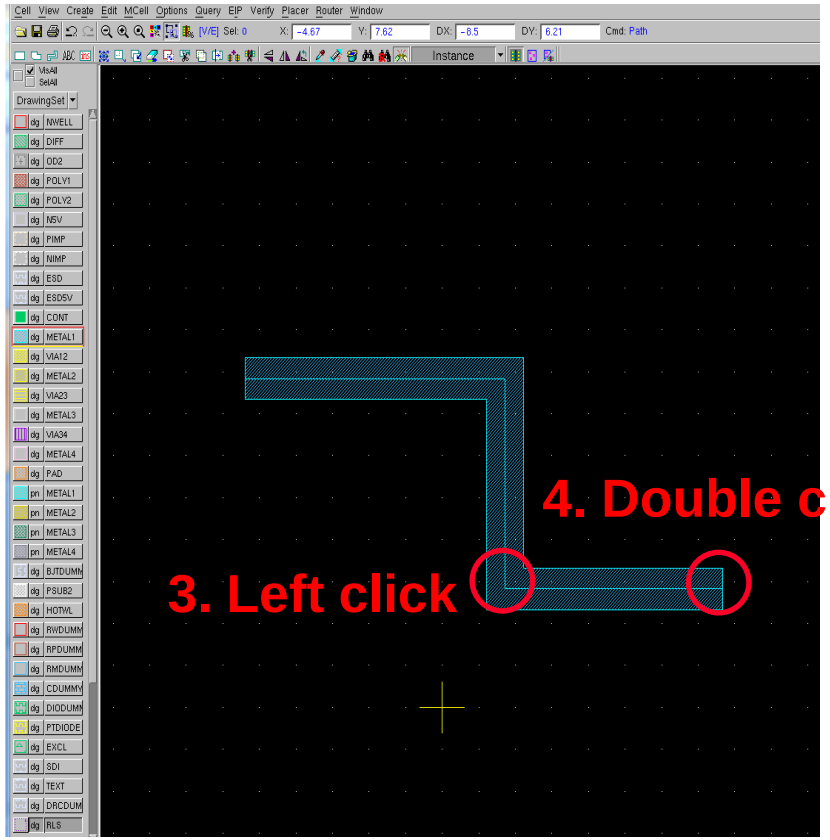
Laker – (U)ndo



Laker – (P)ath

- Path(p)
  - Choose a material → Press p → point to turn → double click to dest.



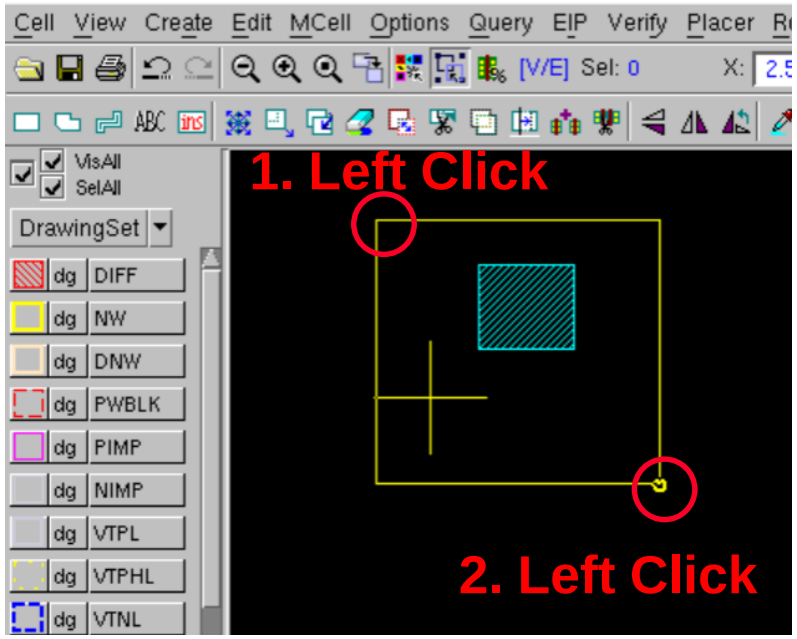


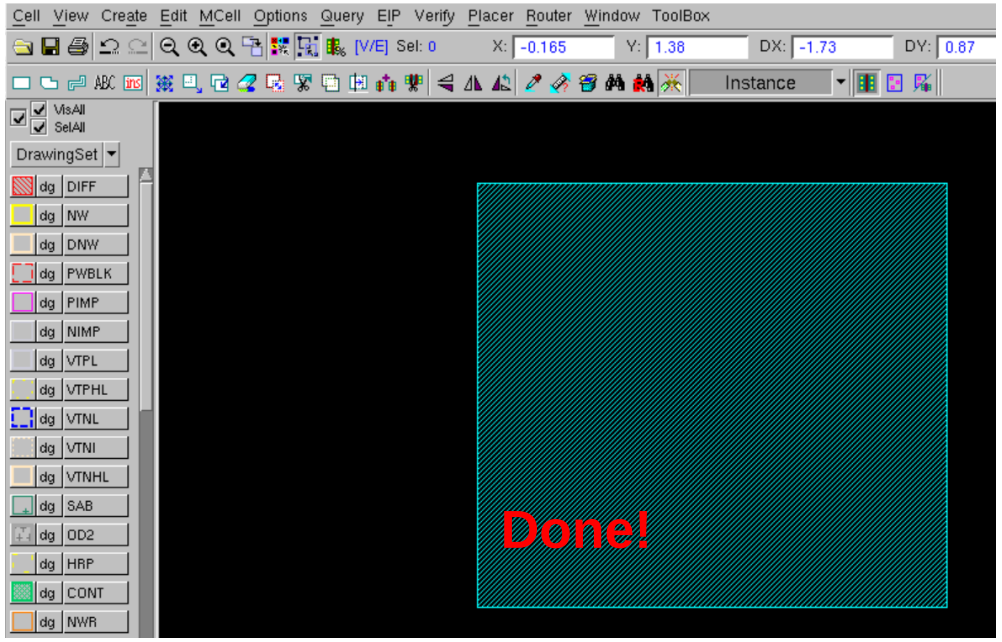
Laker – (Z)oom (1/3)

- Zoom in (ctrl + z)
- Zoom out (shift + z)
- Fit to screen (f)
- Zoom to area (z + mouse left click)
  - Press z → point ref. → point dest.
- Zoom to area (mouse right drag)
  - Right click at ref. → drag to dest.

Laker – (Z)oom (2/3)

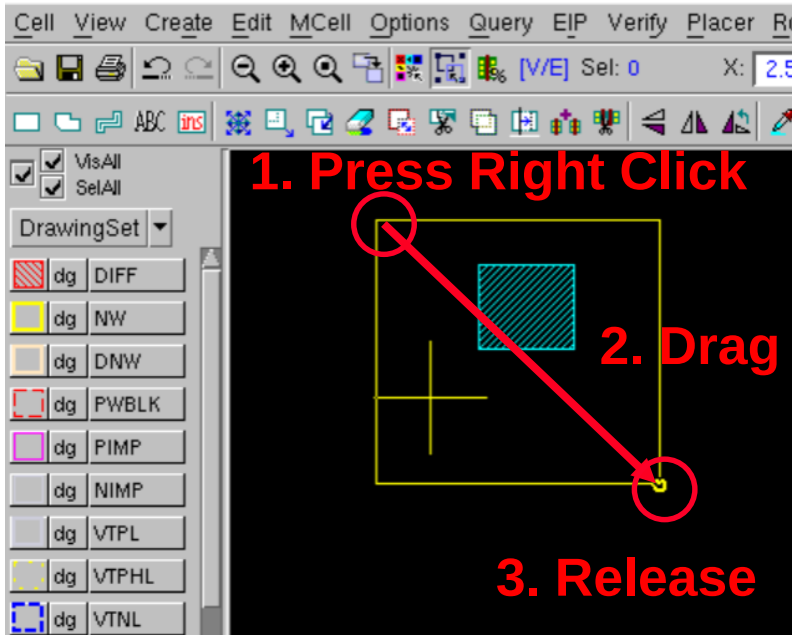
- Zoom to area (z + mouse left click)
  - Press z → point ref. → point dest.

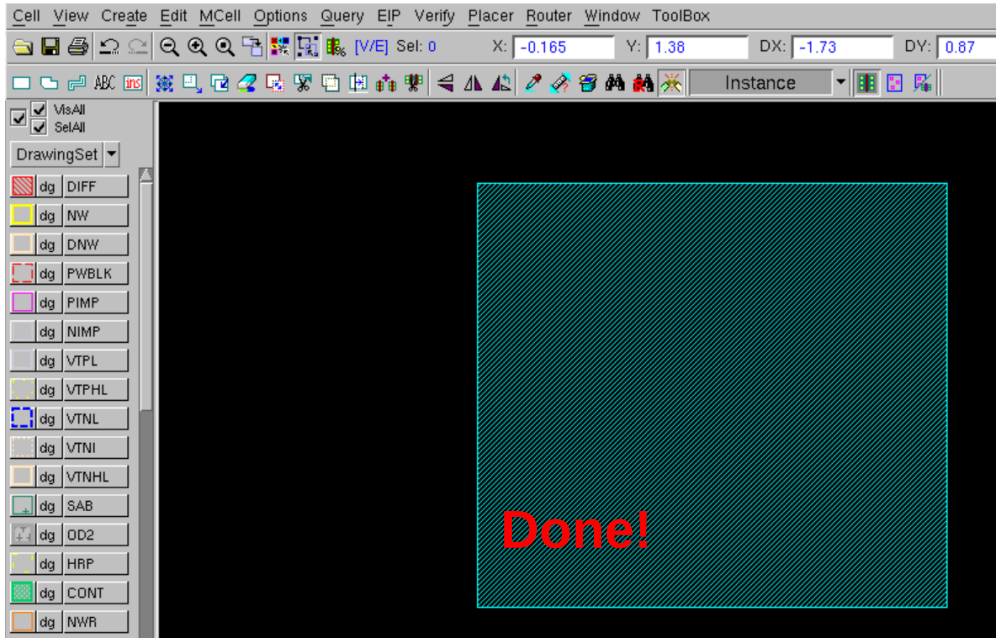




Laker – (Z)oom (3/3)

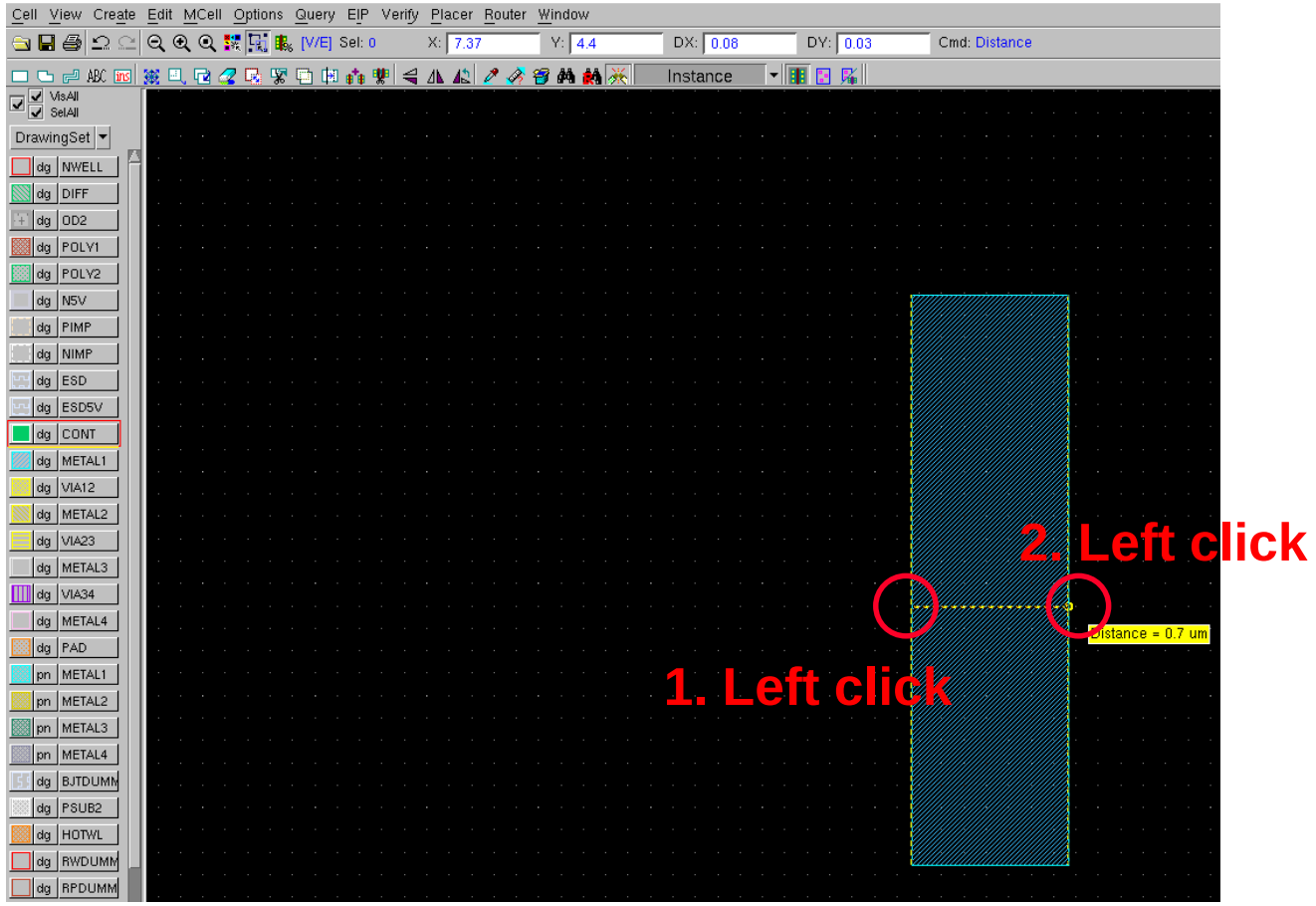
- Zoom to area (mouse right drag)
  - Right click at ref. → drag to dest.





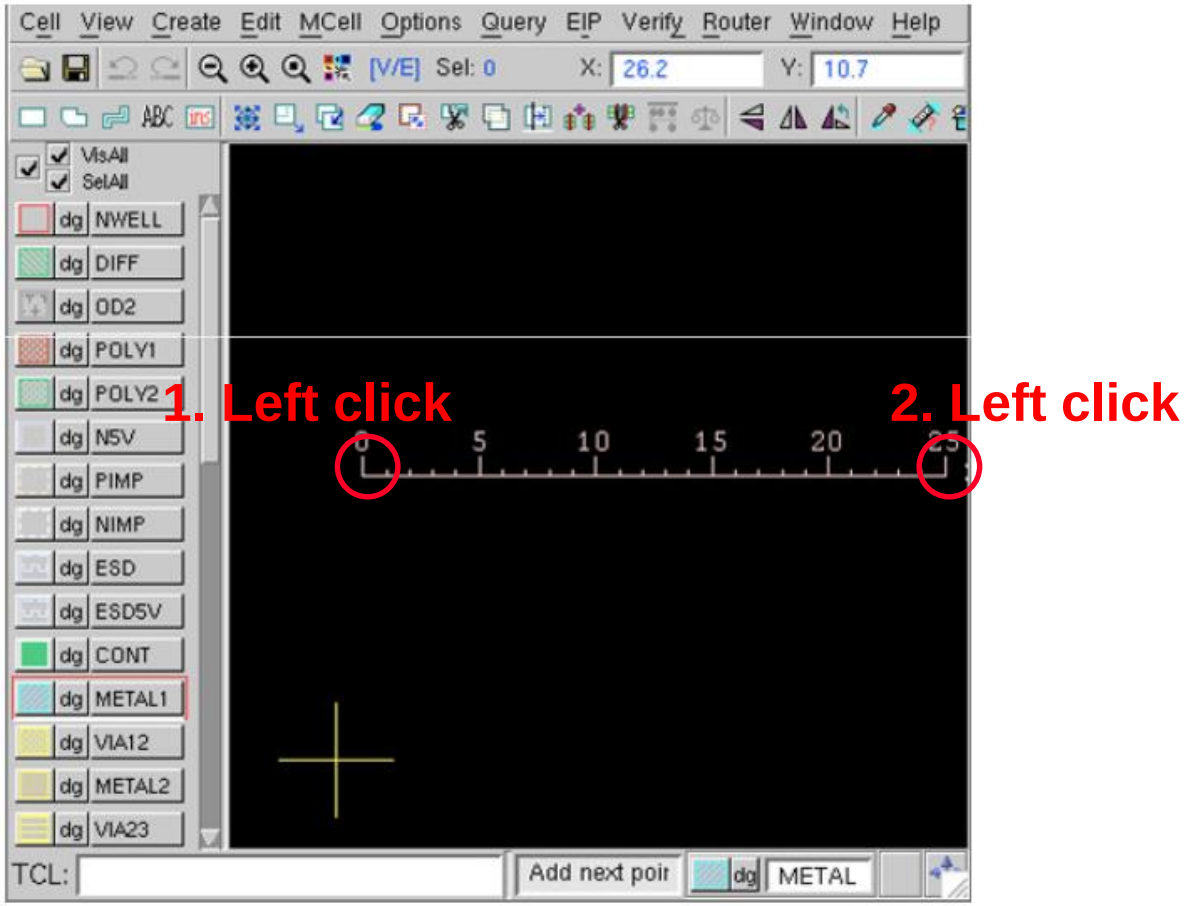
Laker – (D)istance

- Measure Distance (d)
  - Press d → point ref. → stop the mouse at dest.



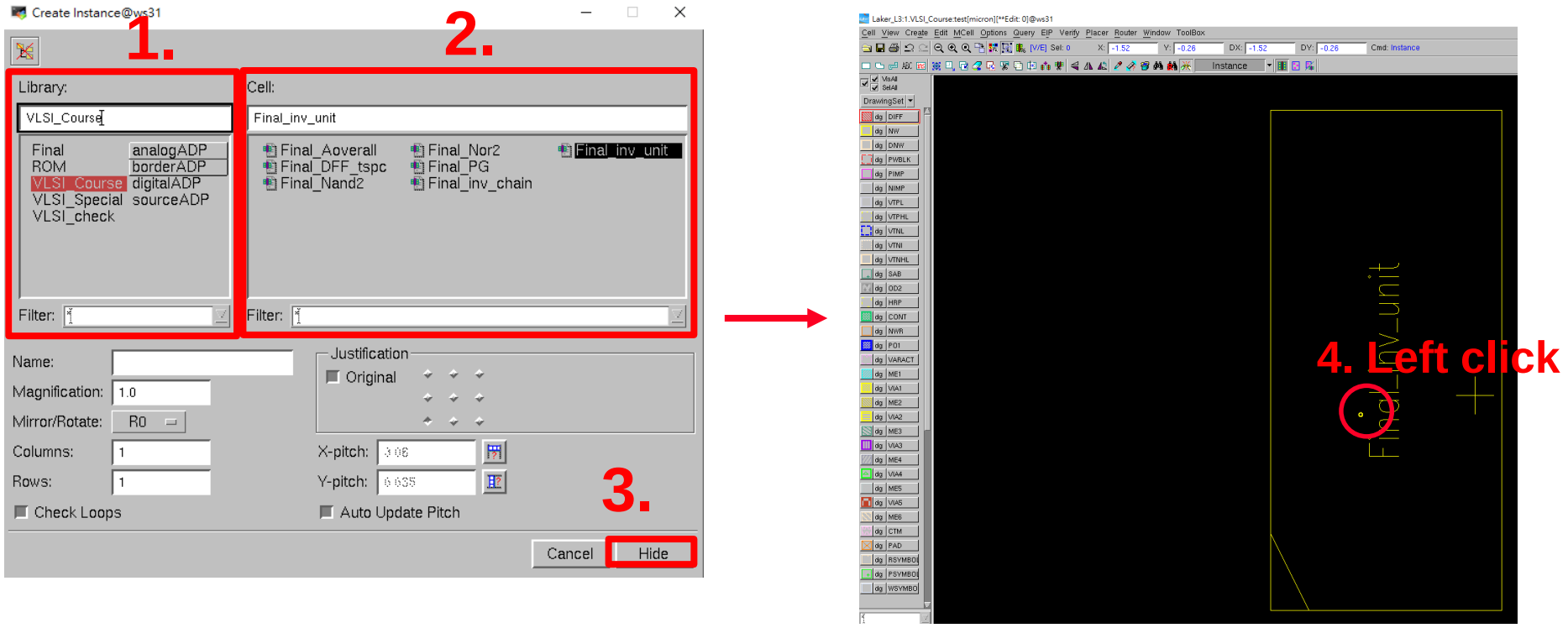
Laker – Mar(K)er

- Marker (k) /Remove all Markers(shift + k)
  - Press k → point ref. → point dest.



Laker – (I)nstance (1/2)

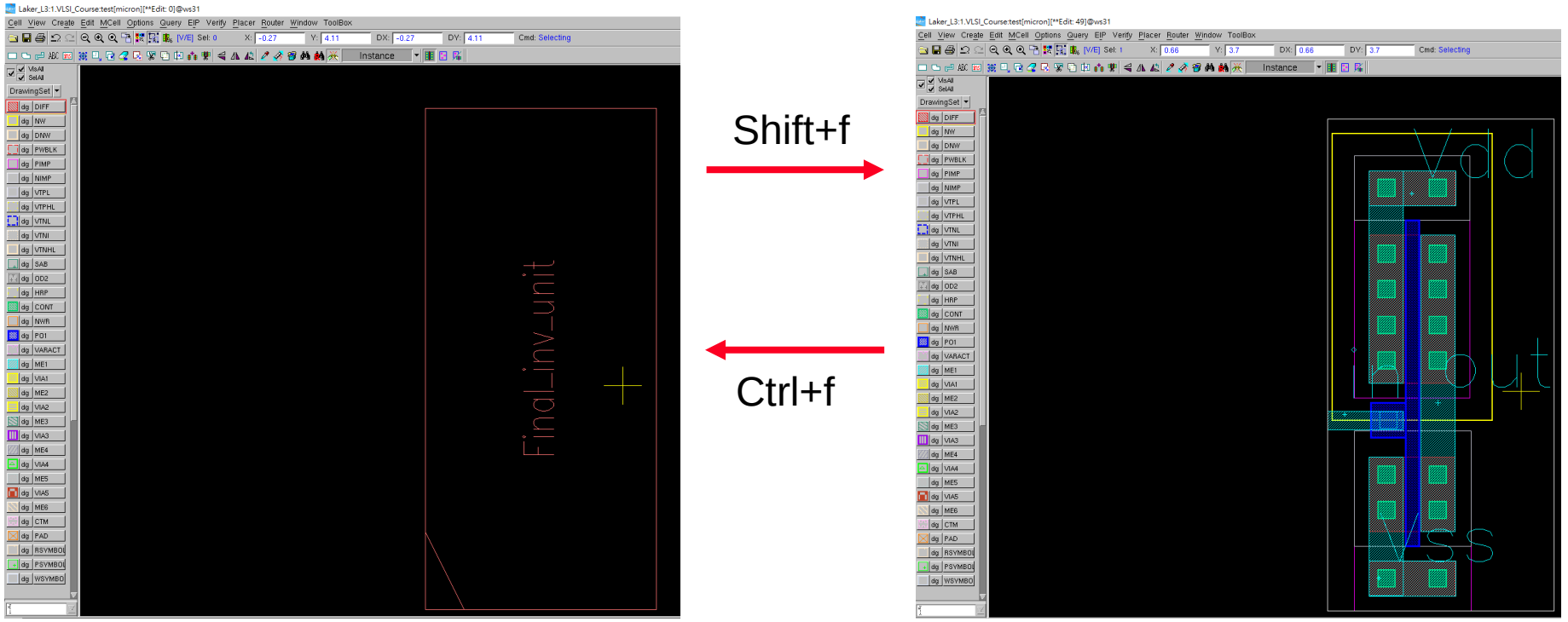
- Call an Instance (I)
  - Press I → select the cell → place the cell



Laker – (I)nstance (2/2)

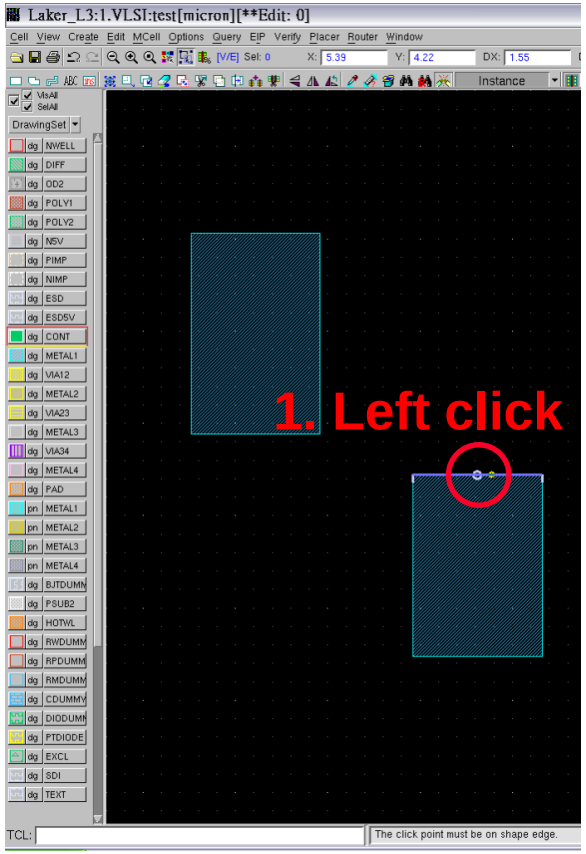
- Min/Max View Level (ctrl/shift+f)

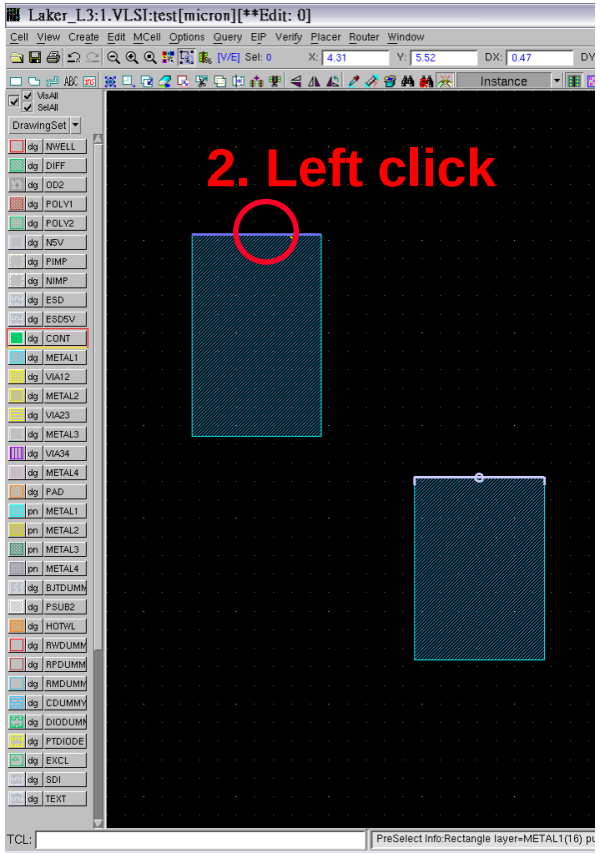
→ After add an instance, we can choose the view level we want.

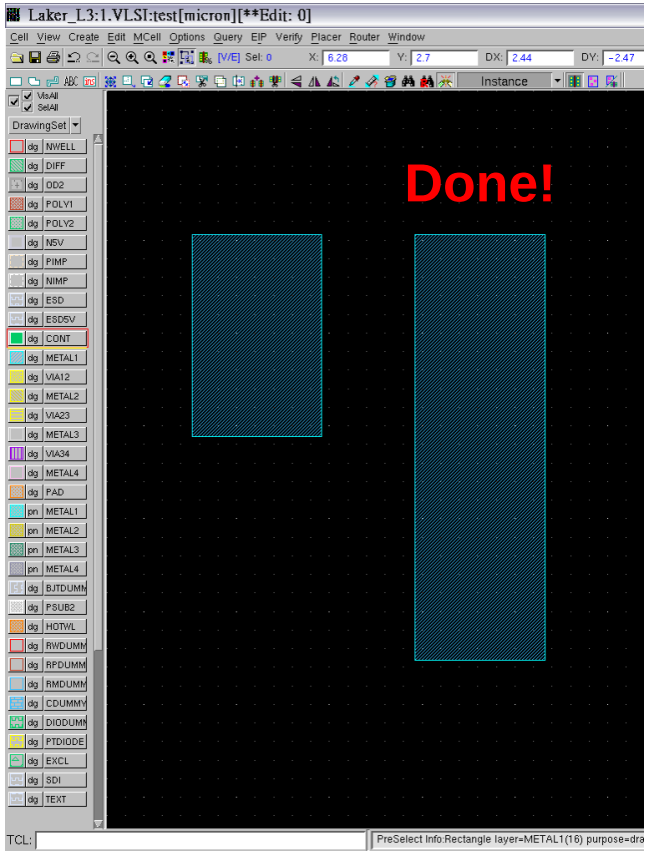


Laker – (A)lign

- Align (a)
  - Press a → point ref. → point dest.







Practice – Align (Part A)

- Part A: Please try the Align function with different ref. and dest. position, and write down the results :

Reference point	Destination point
1. Middle point of edge 2. Vertex	1. Middle point of edge 2. Edge 3. Vertex

Practice – Align (Part B)

- Part B: Please try the Align function with **only select the edge**, and repeat part A.

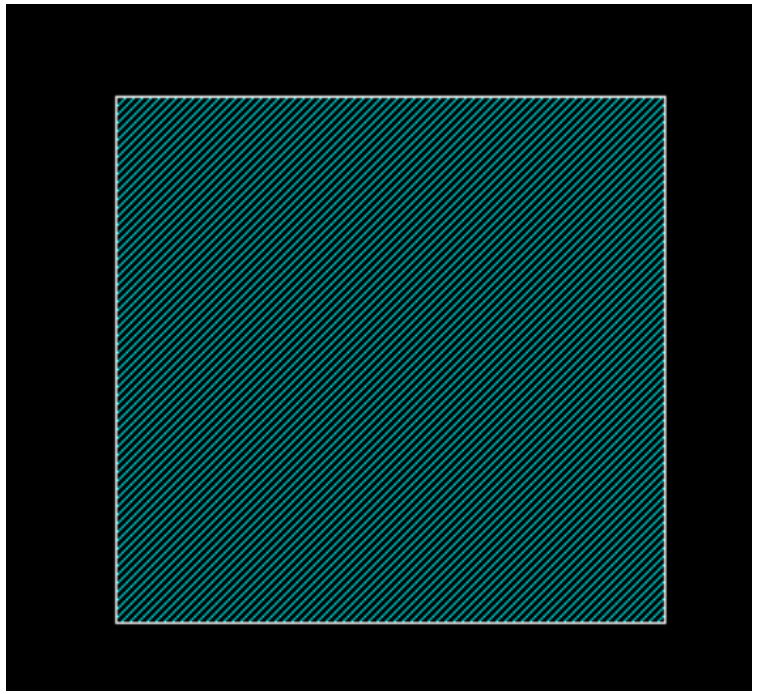


Fig1. Select the whole block

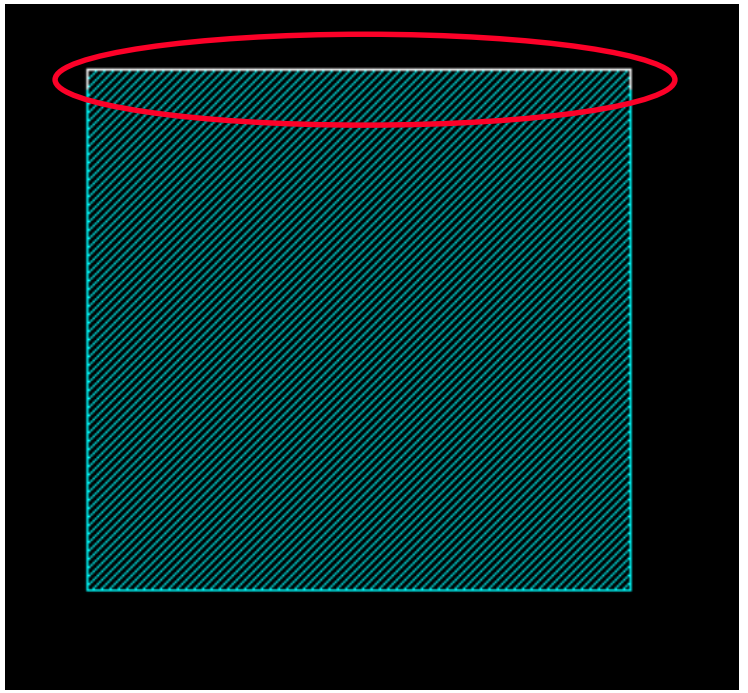
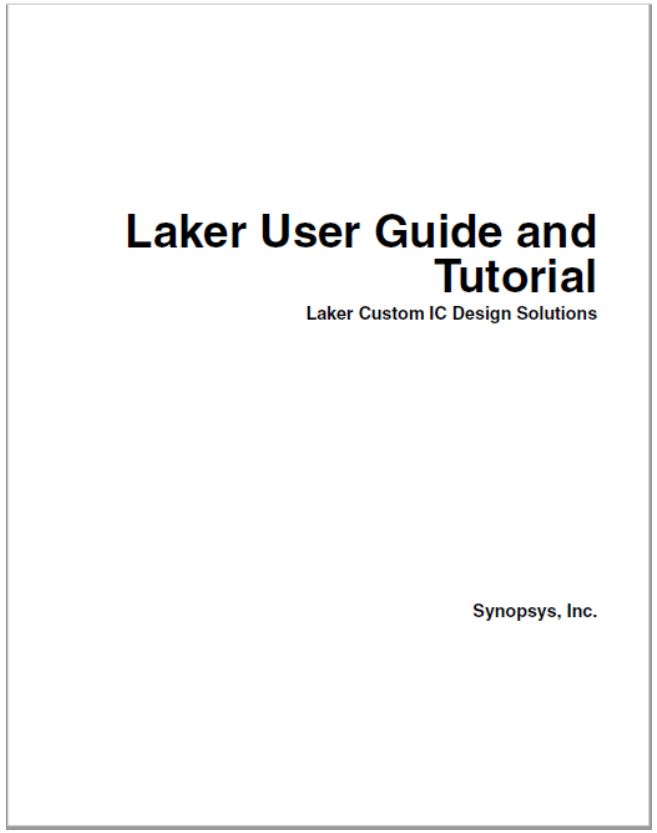


Fig2. Only select the edge

Advanced hot key

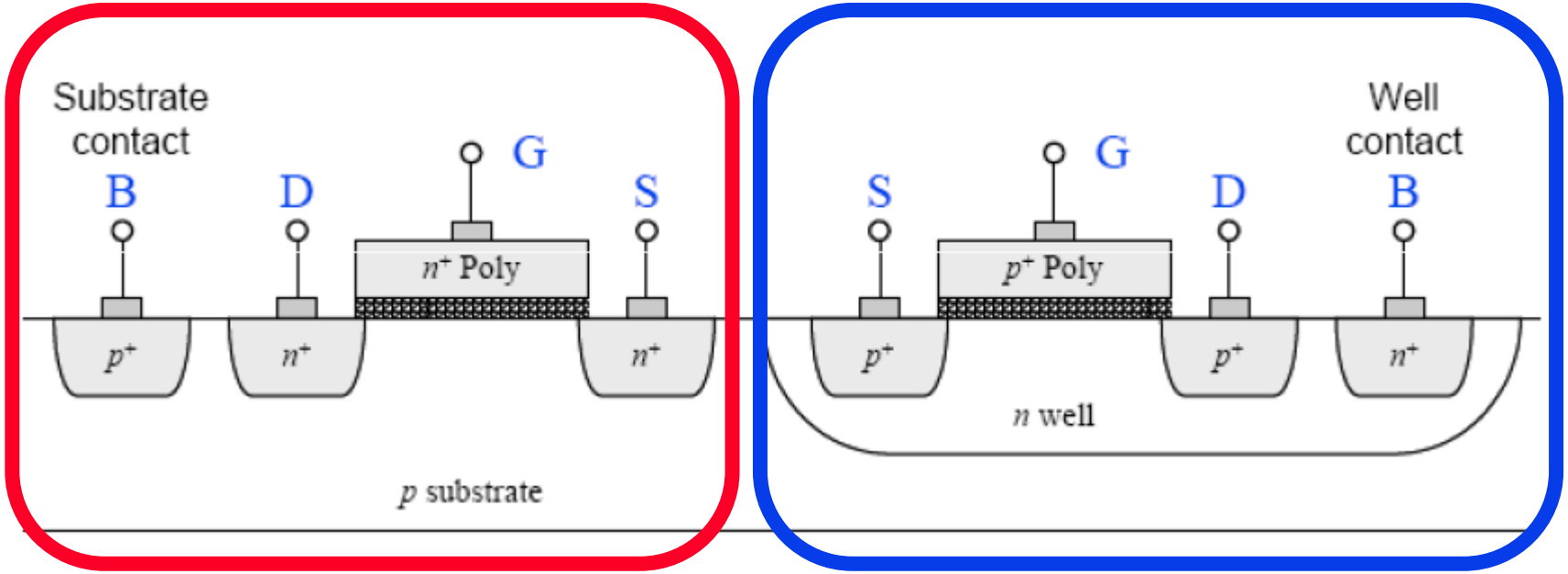
- If you want to learn more advanced hot key or get more detailed information, please refer to Laker User Guide and Tutorial.



Process & Layout

Process

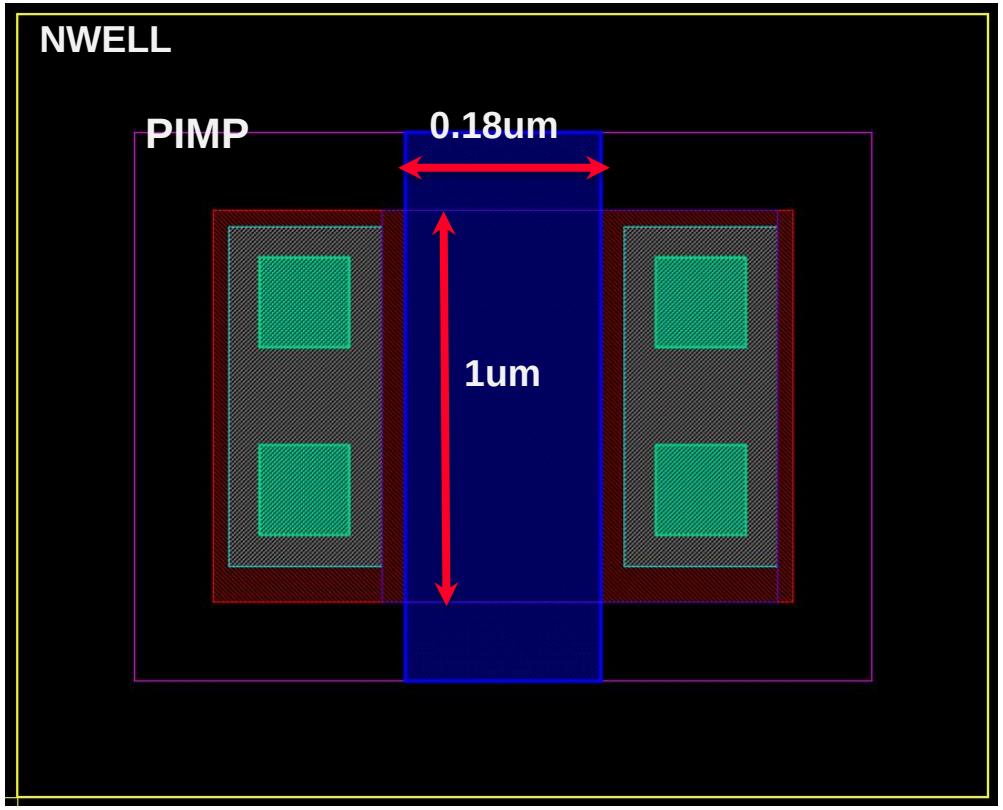
- Cross Section View of NMOS & PMOS

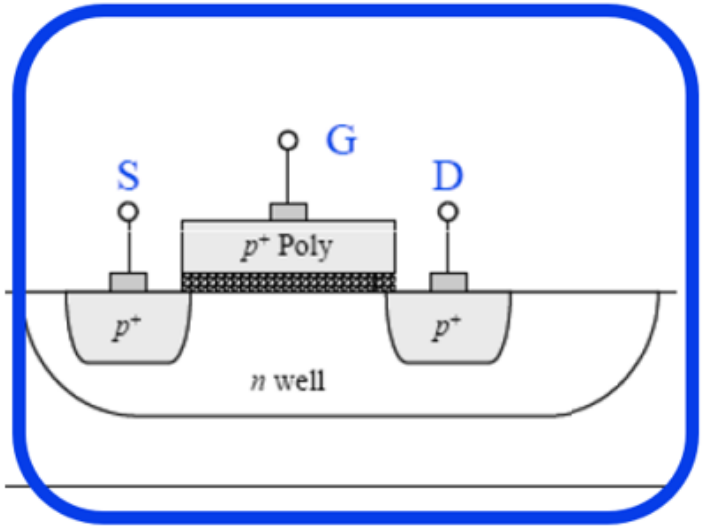


NMOS **PMOS**

Example – PMOS

- Draw a PMOS with L=0.18um W=1um



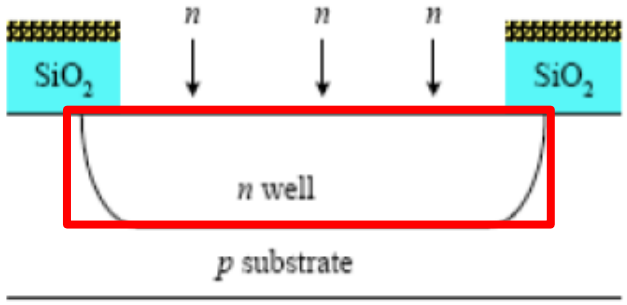


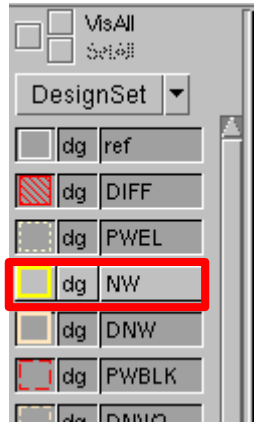
PMOS

PMOS Process vs. Layout

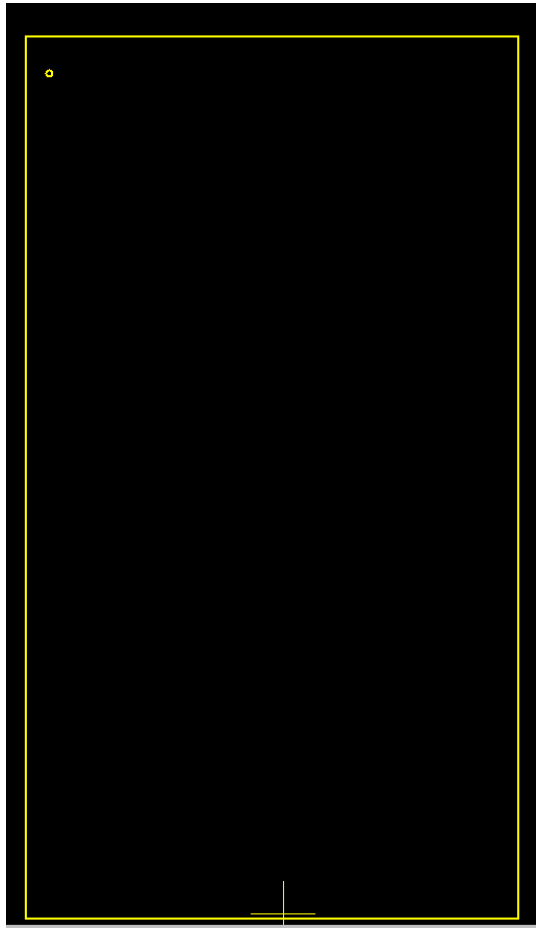
- Process v.s. Layout

1. **N well**



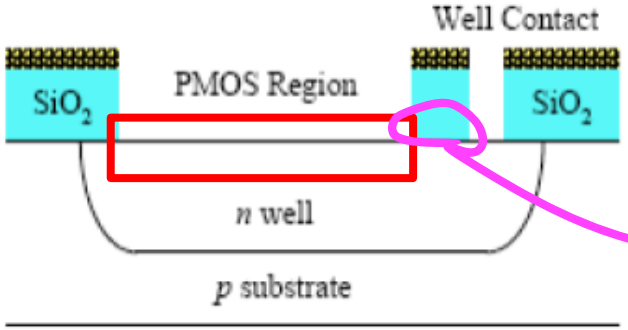


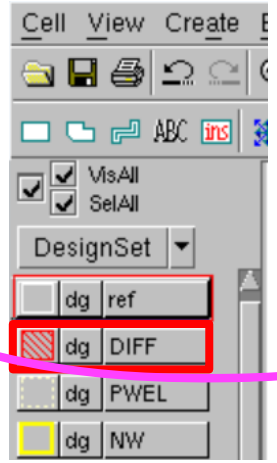
- NWELL

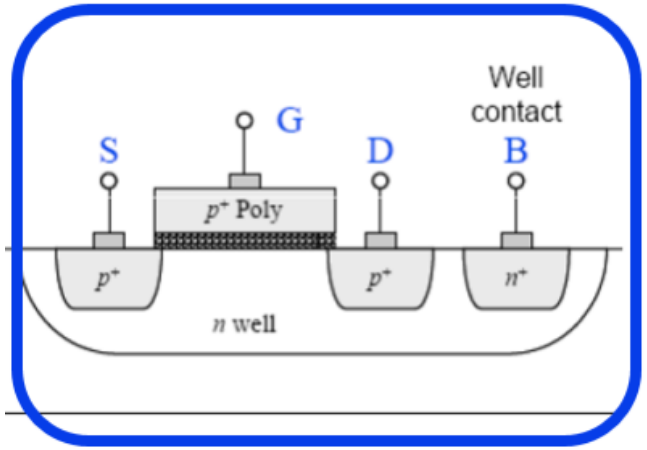


PMOS Process vs. Layout

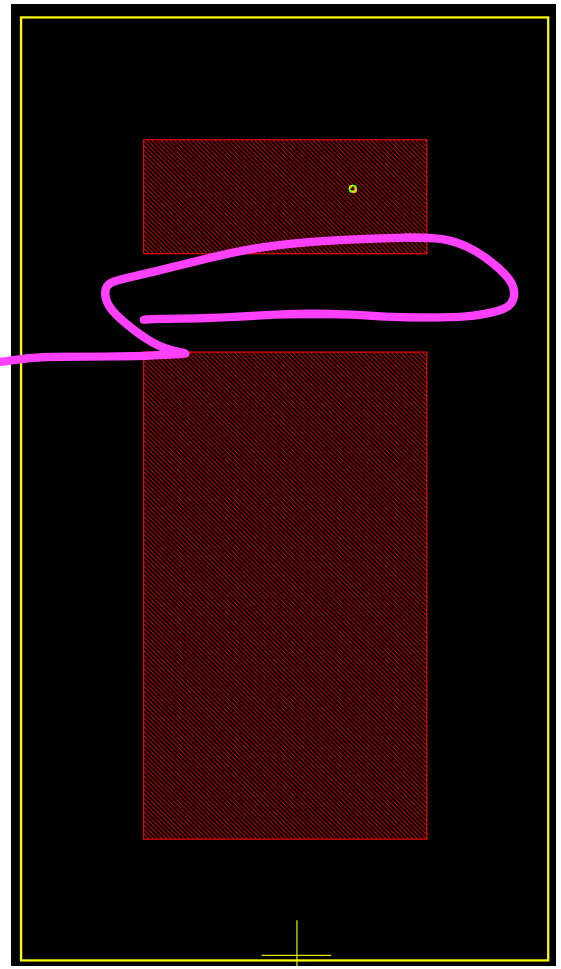
- Process v.s. Layout
  - 2. **Diffusion**





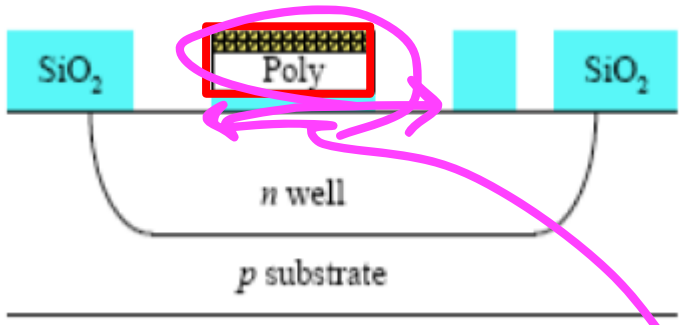


- DIFF

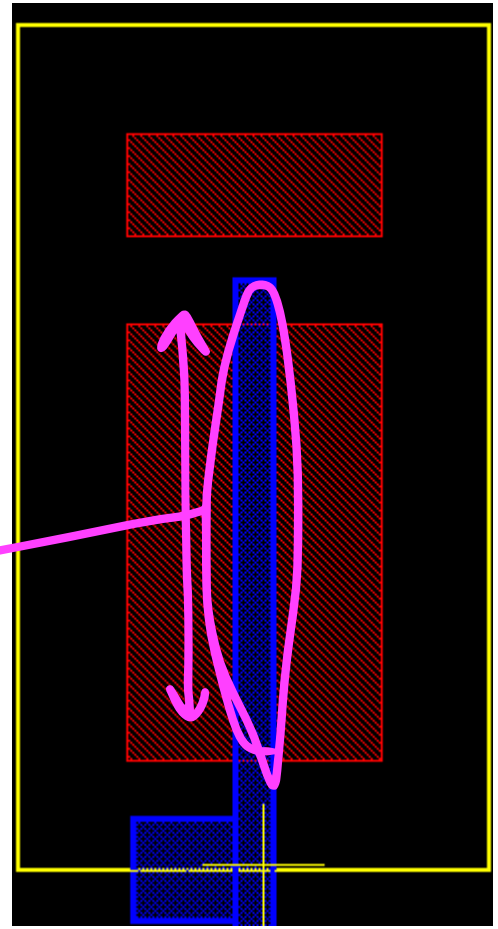


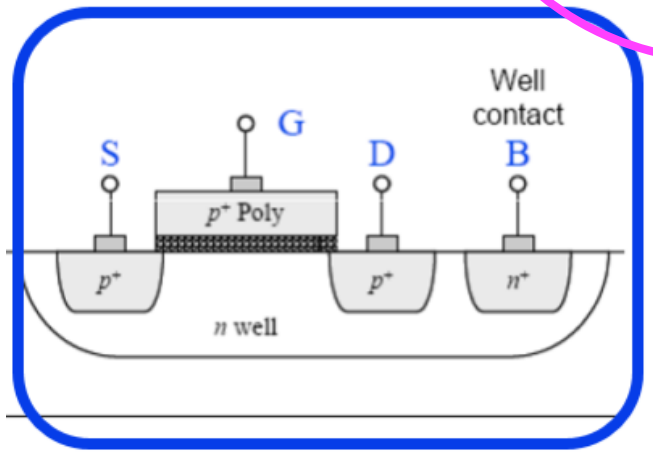
PMOS Process vs. Layout

3. Poly gate



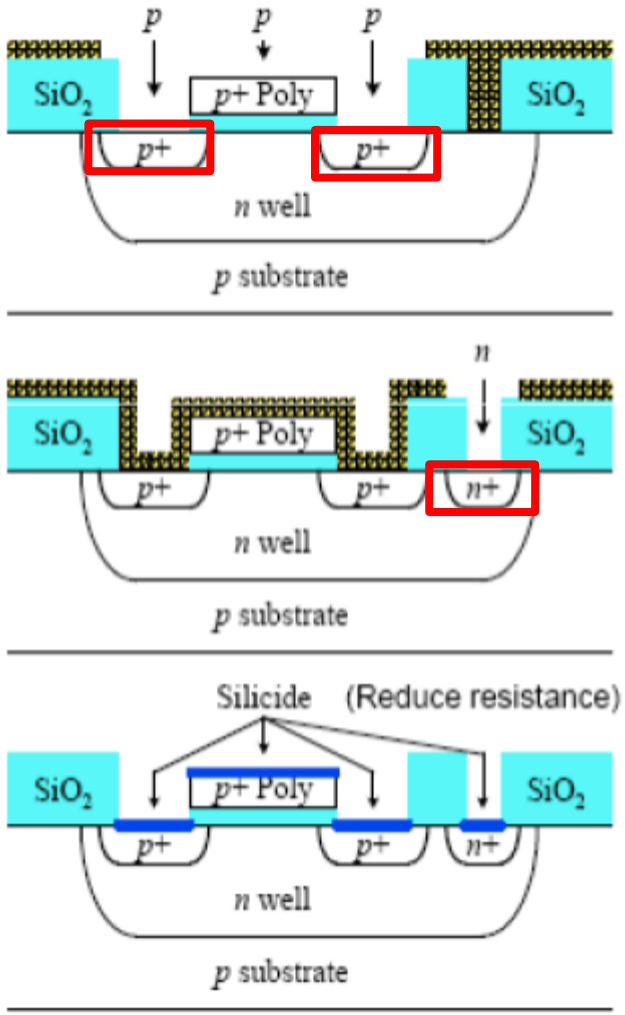
- PO1

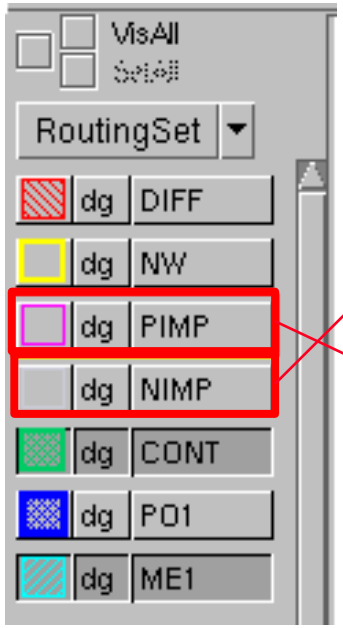




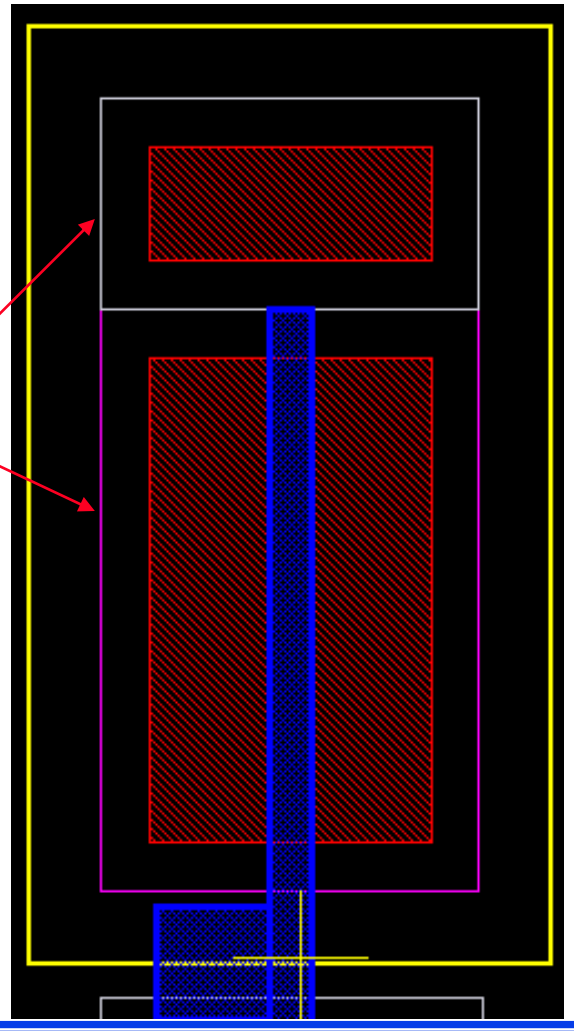
PMOS Process vs. Layout

4. P+/N+ Implant



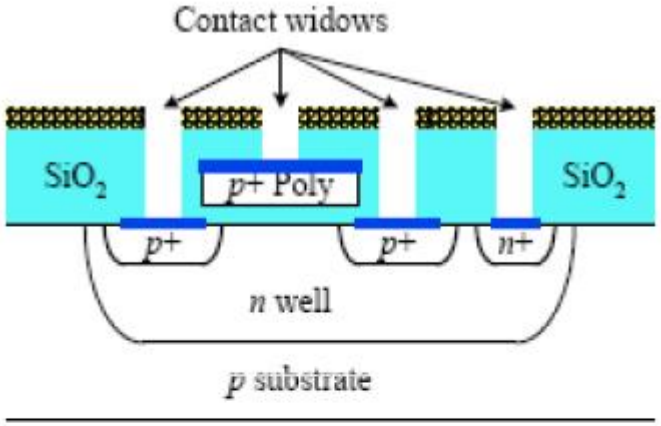


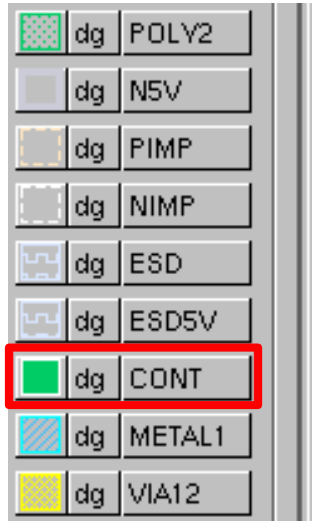
- PIMP



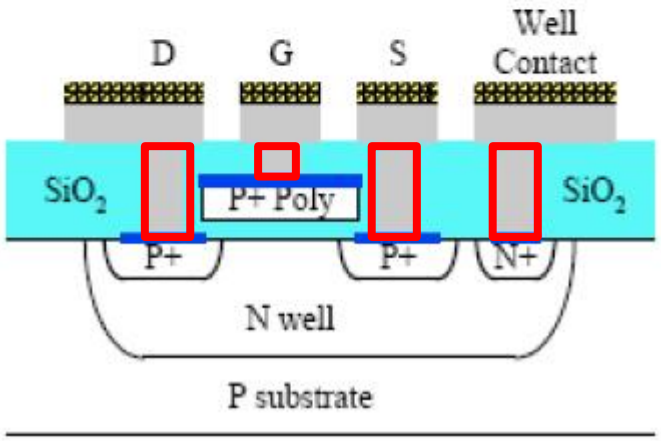
PMOS Process vs. Layout

5. Contacts

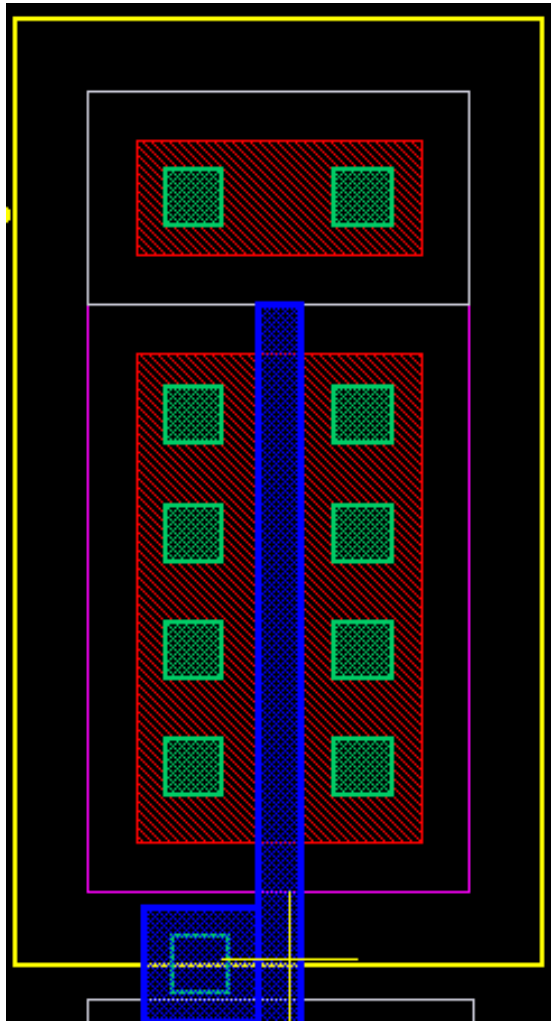




Metal: Al or Cu

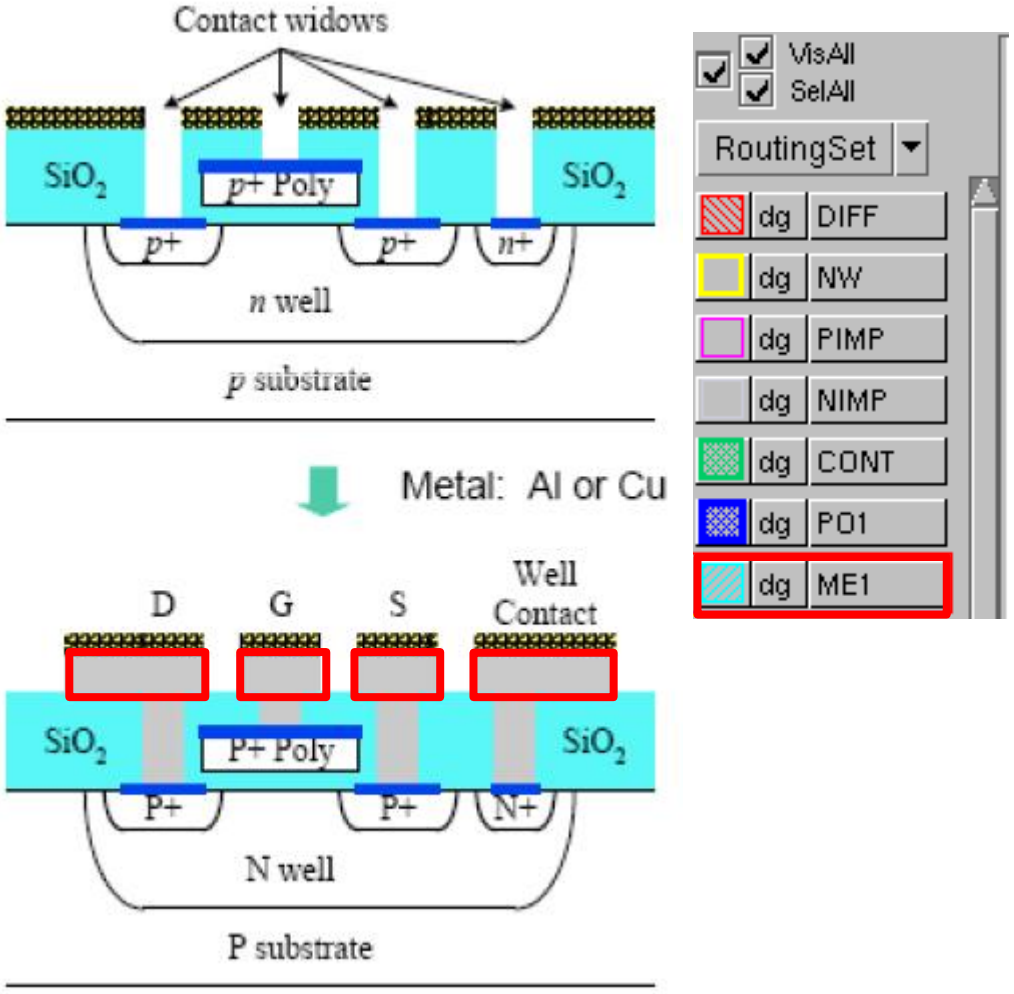


- CONT

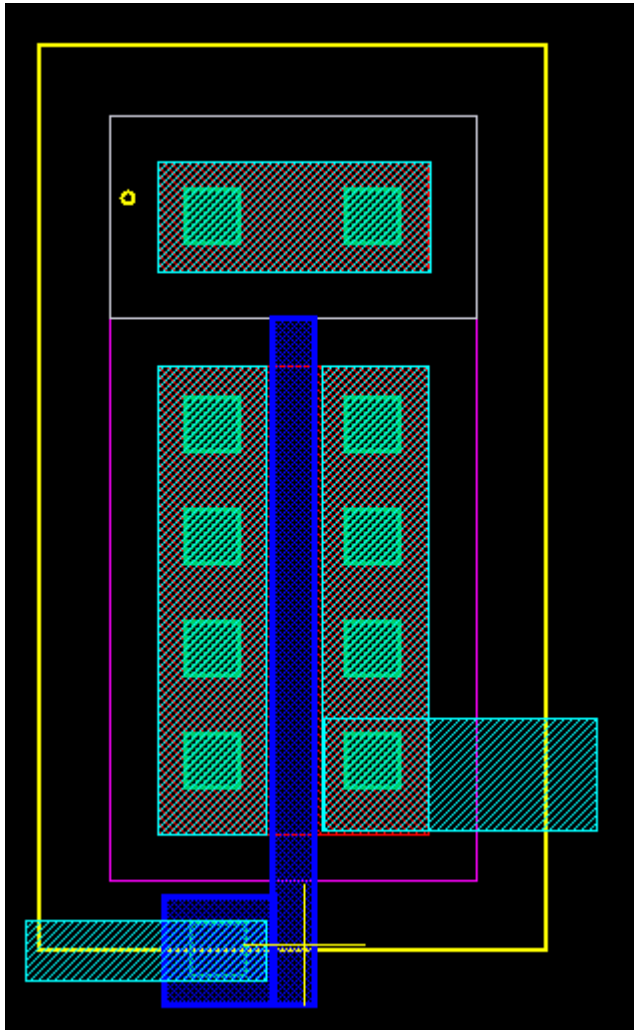


PMOS Process vs. Layout

5. Metal lines

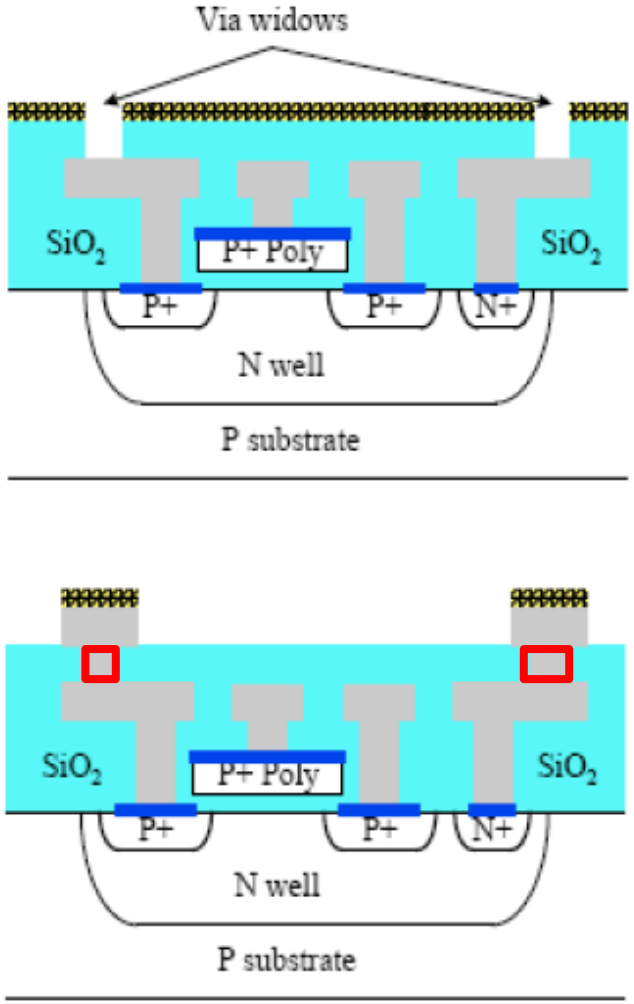


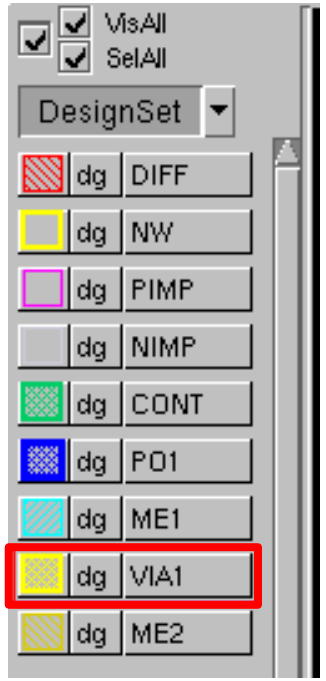
- ME1



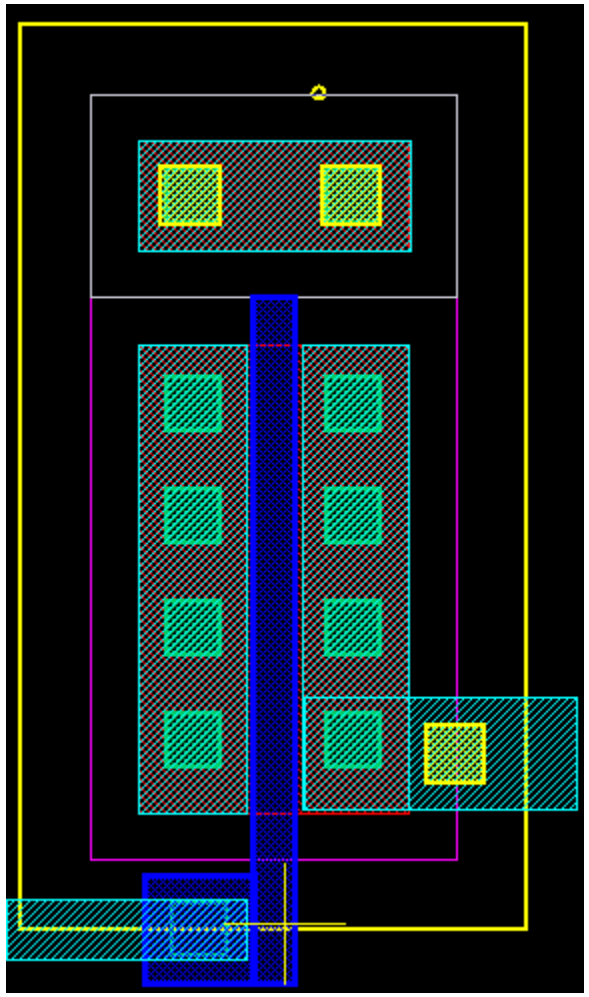
PMOS Process vs. Layout

6. Metal vias/lines



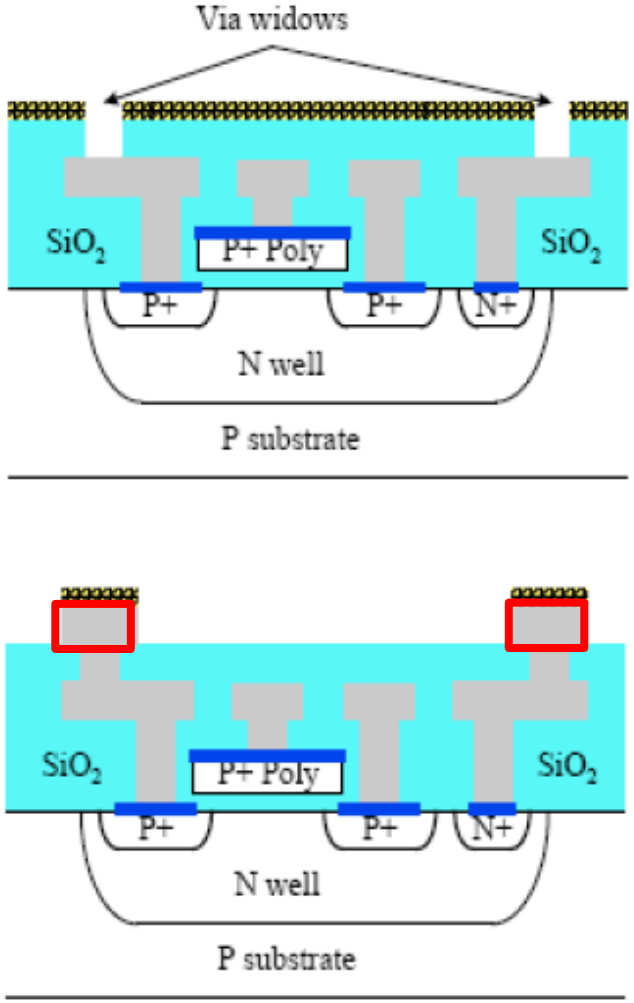


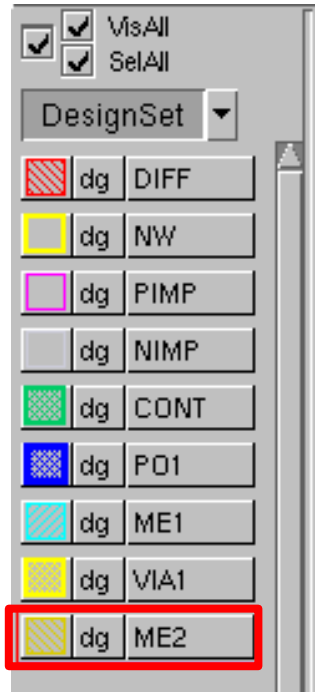
- VIA1



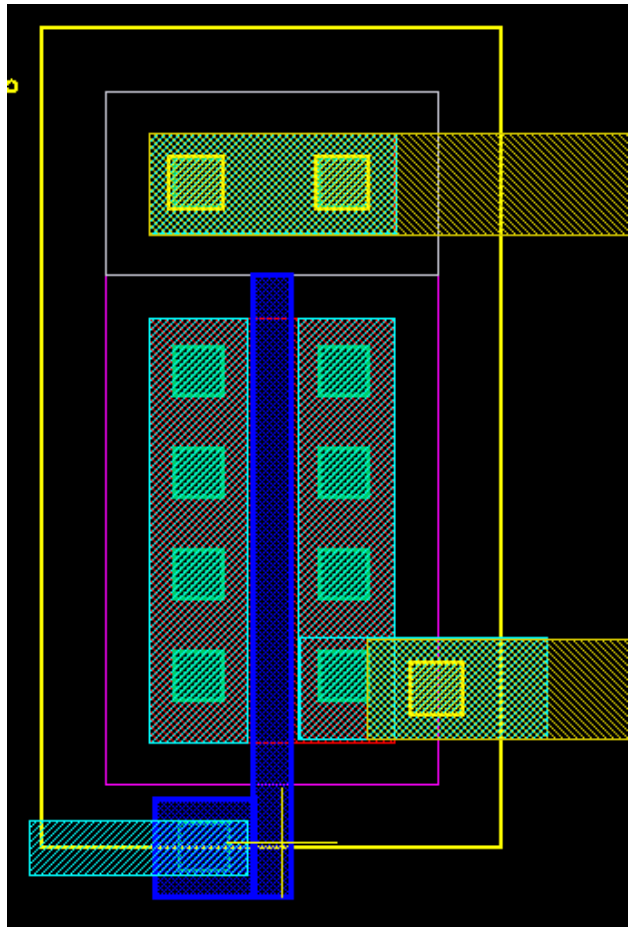
PMOS Process vs. Layout

6. Metal vias/lines



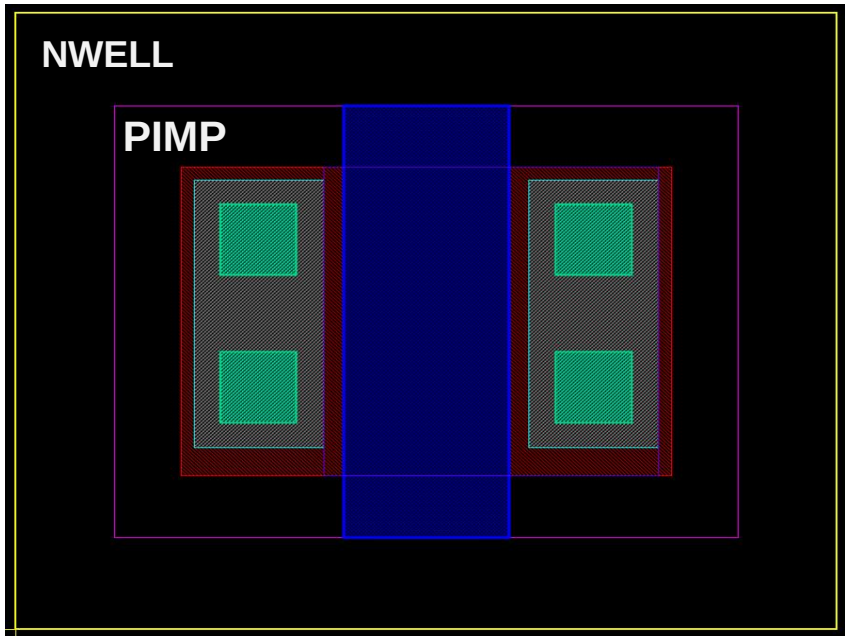


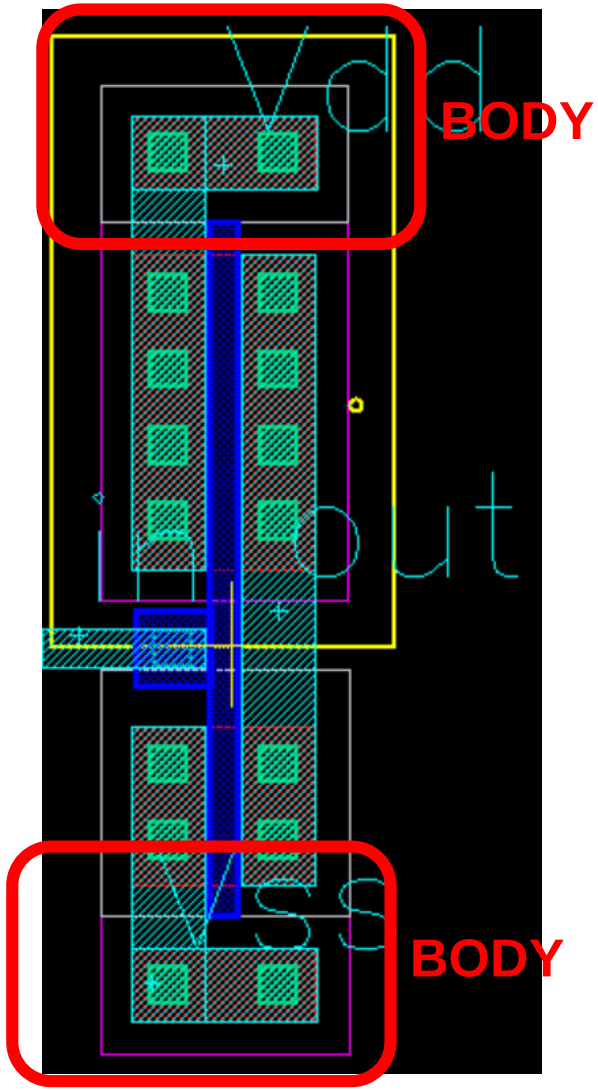
- METAL2



Practice – Inverter

- Please Draw an Inverter with
  - (W_n/L_n = 1um/0.18um)
  - (W_p/L_p = 2um/0.18um)





Multiply the Width

Multiply the Width

- If we have a MOS with multiple of unit sizes, it's impractical to draw it directly. We can use the following 2 method to make it easily to implement.

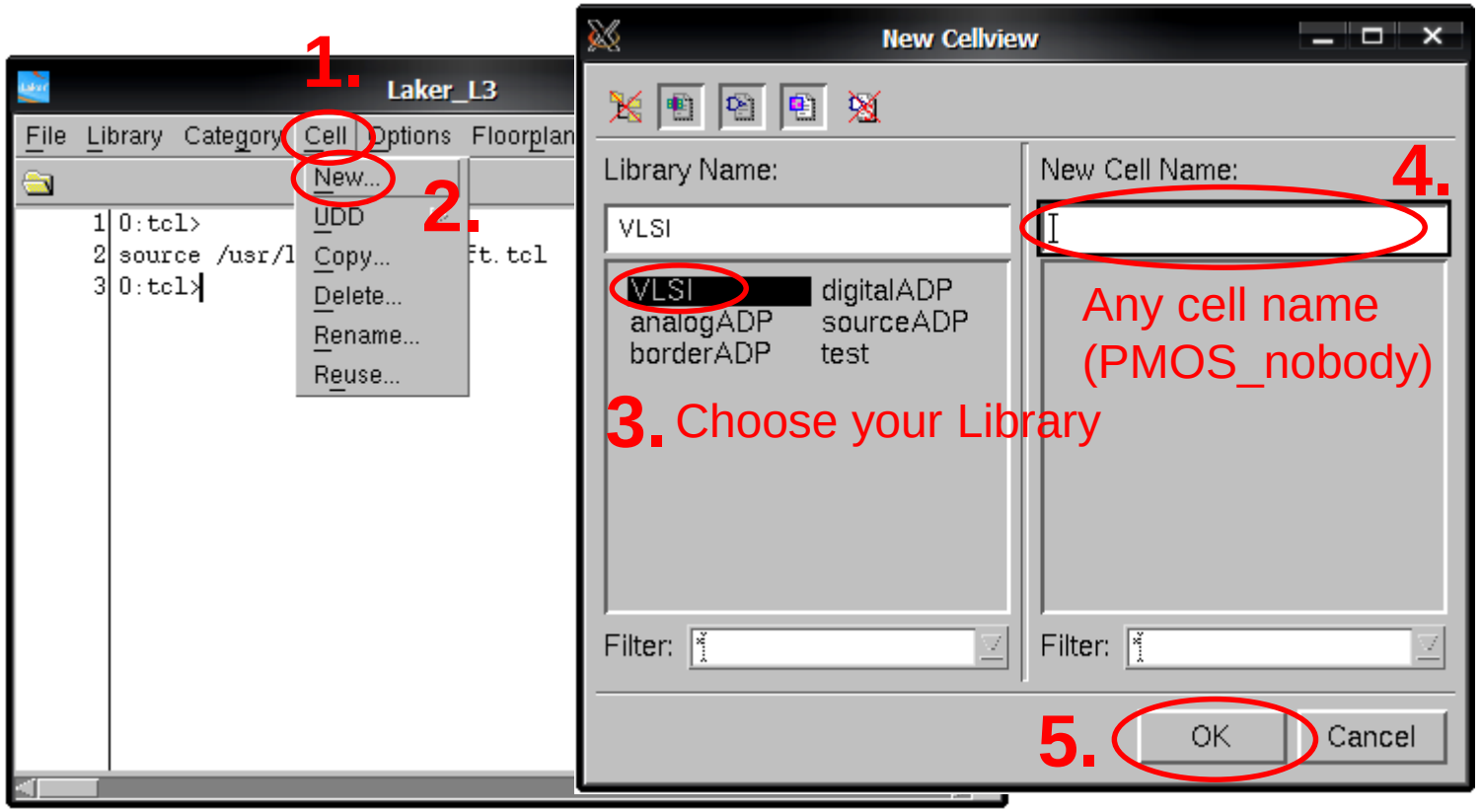
1. Connect with Cell Boundary
2. Fold the MOS

- EX: MM1 VD VG VDD VDD p_18 W=2u L=0.18u m=2

If we encounter this condition, we can apply the above 2 methods or just draw a MOS with Width=4u Length=0.18u.

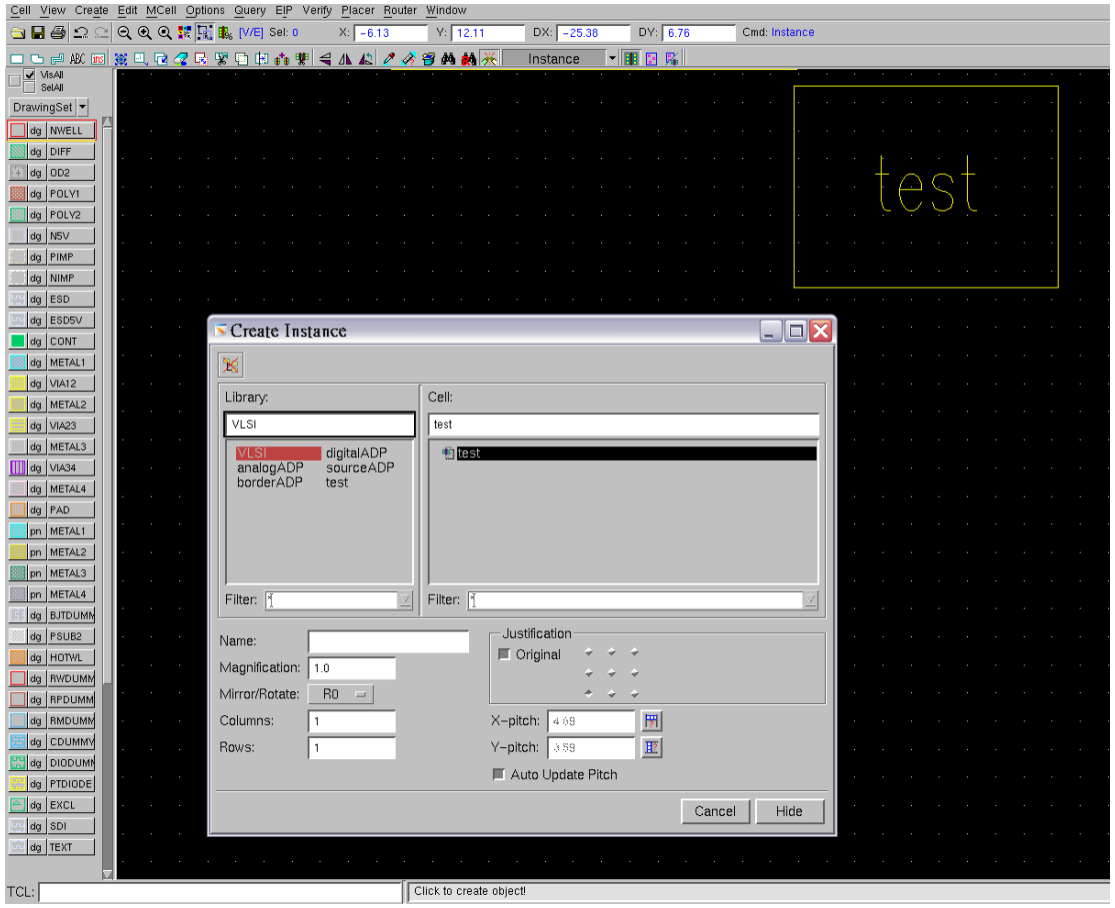
Connect with Cell Boundary (1/6)

- New Cell



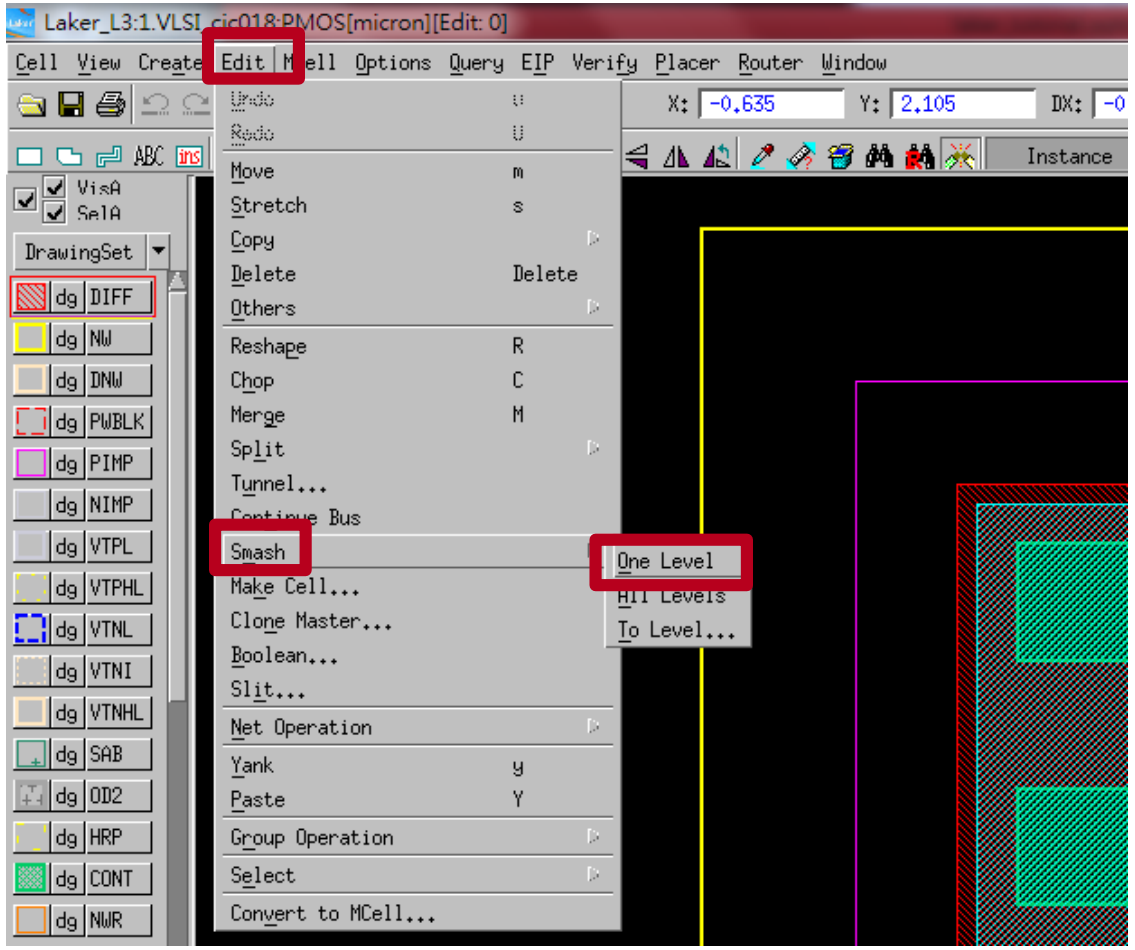
Connect with Cell Boundary (2/6)

- Add Instance (i)
  - Press i → choose the instance → press Hide → point dest.



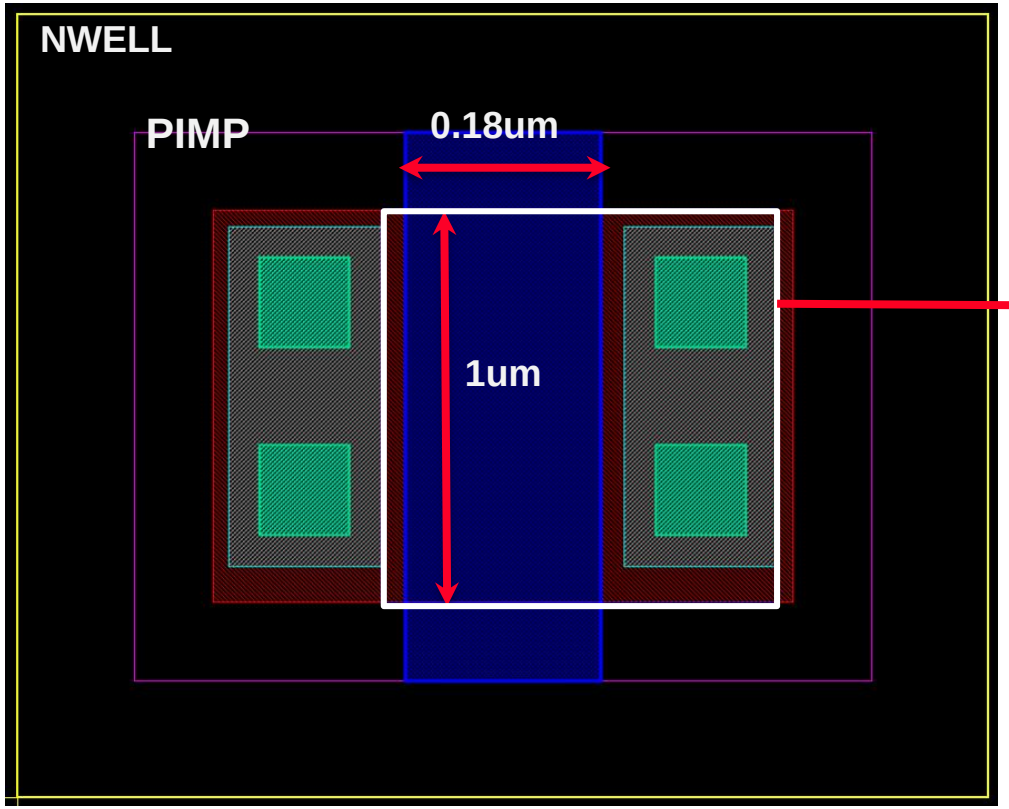
Connect with Cell Boundary (3/6)

- Smash



Connect with Cell Boundary (4/6)

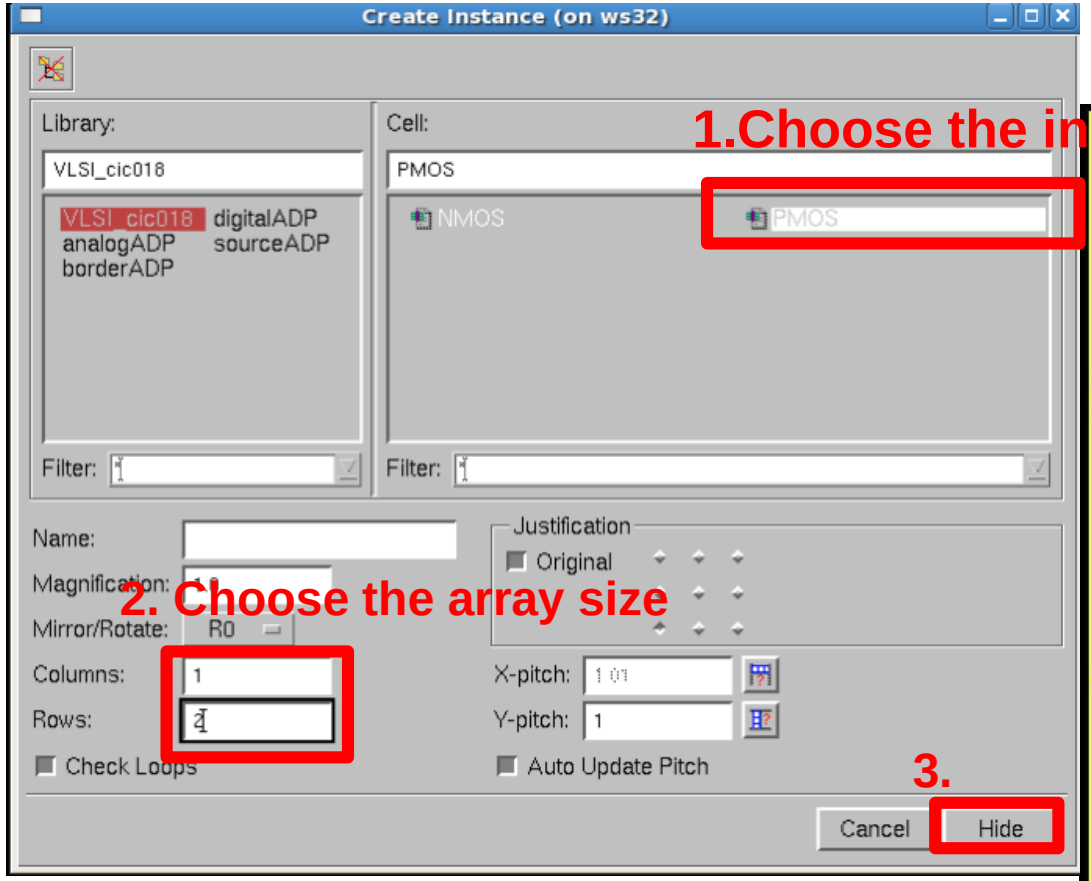
- Add the cell boundary

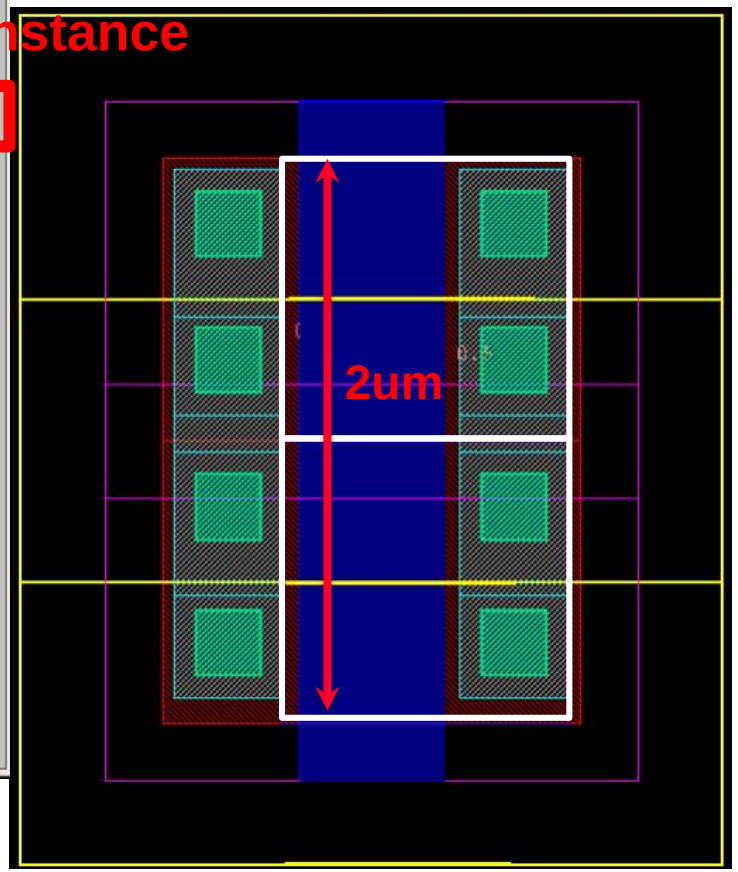


CellBdry

Connect with Cell Boundary (5/6)

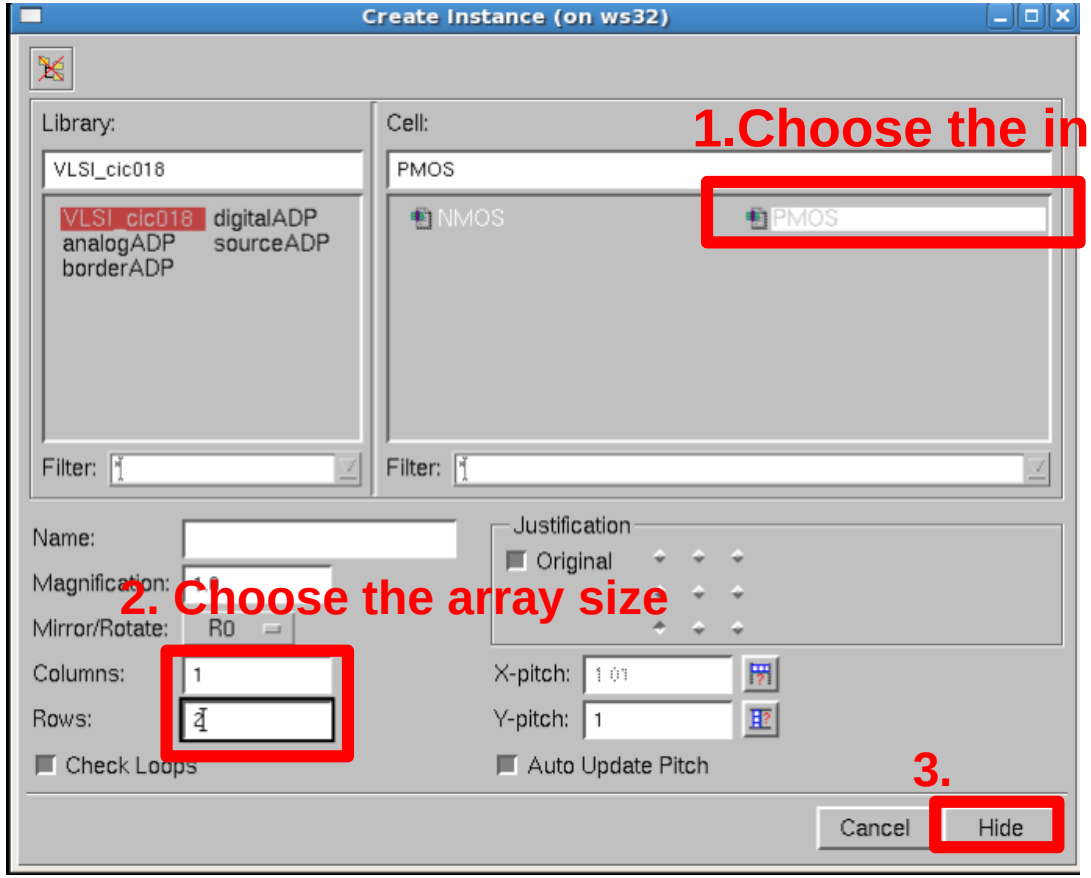
- Add Instance (i)

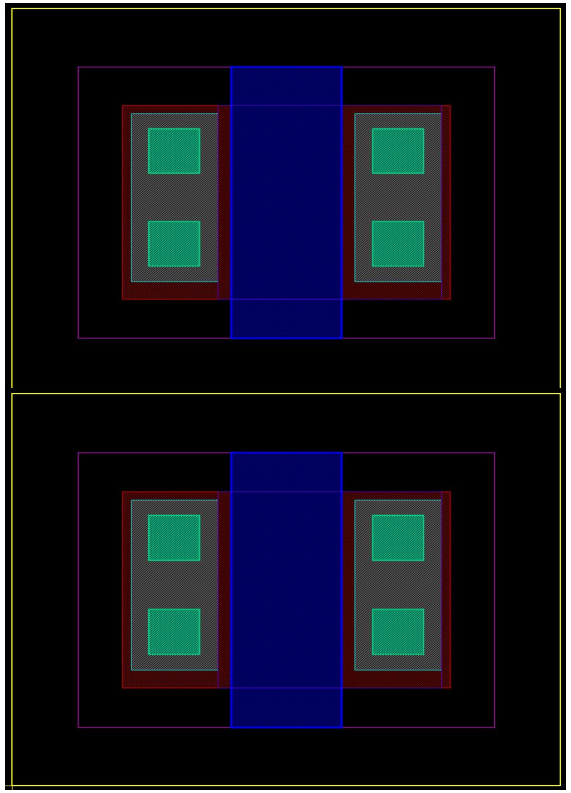




Connect with Cell Boundary (6/6)

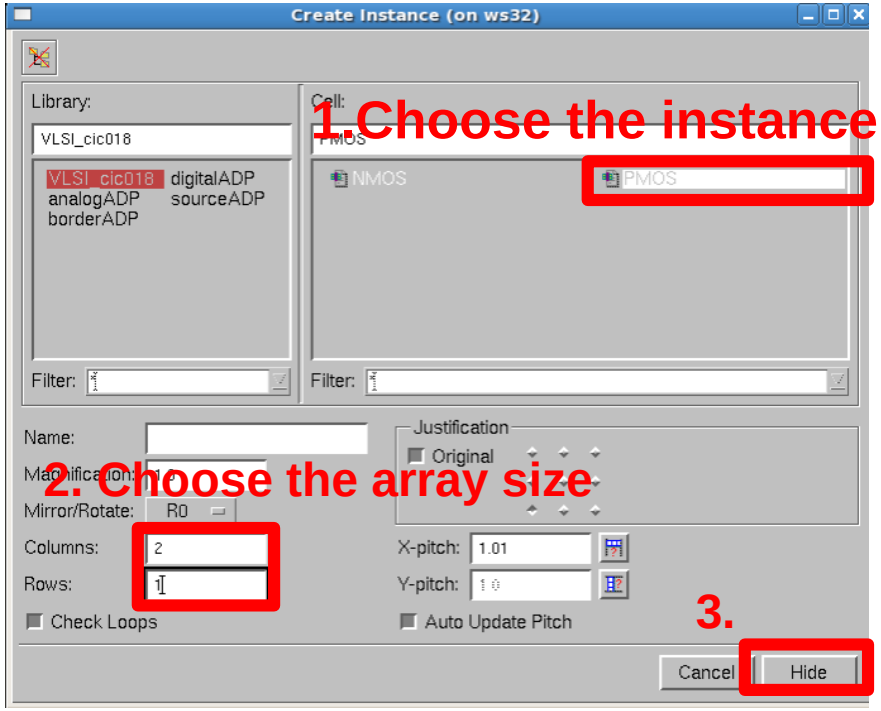
- Fail case : If without the Cell Boundary…

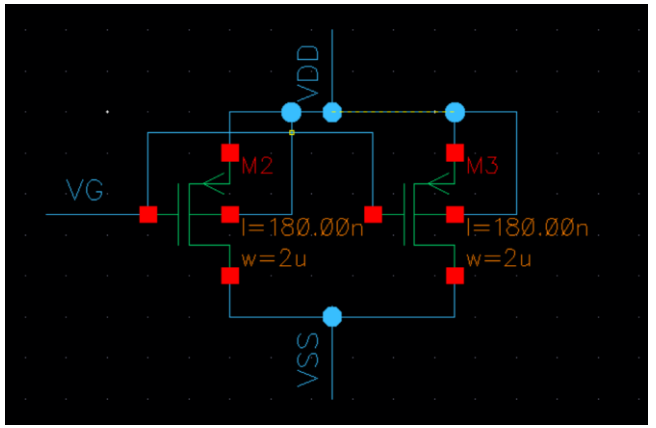


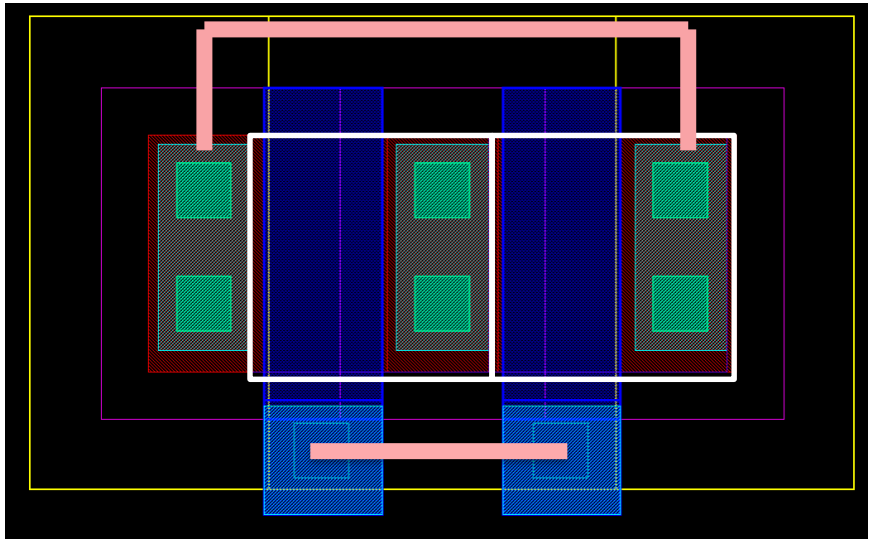


Folded MOS

- Another way to multiple the width, folded MOS.



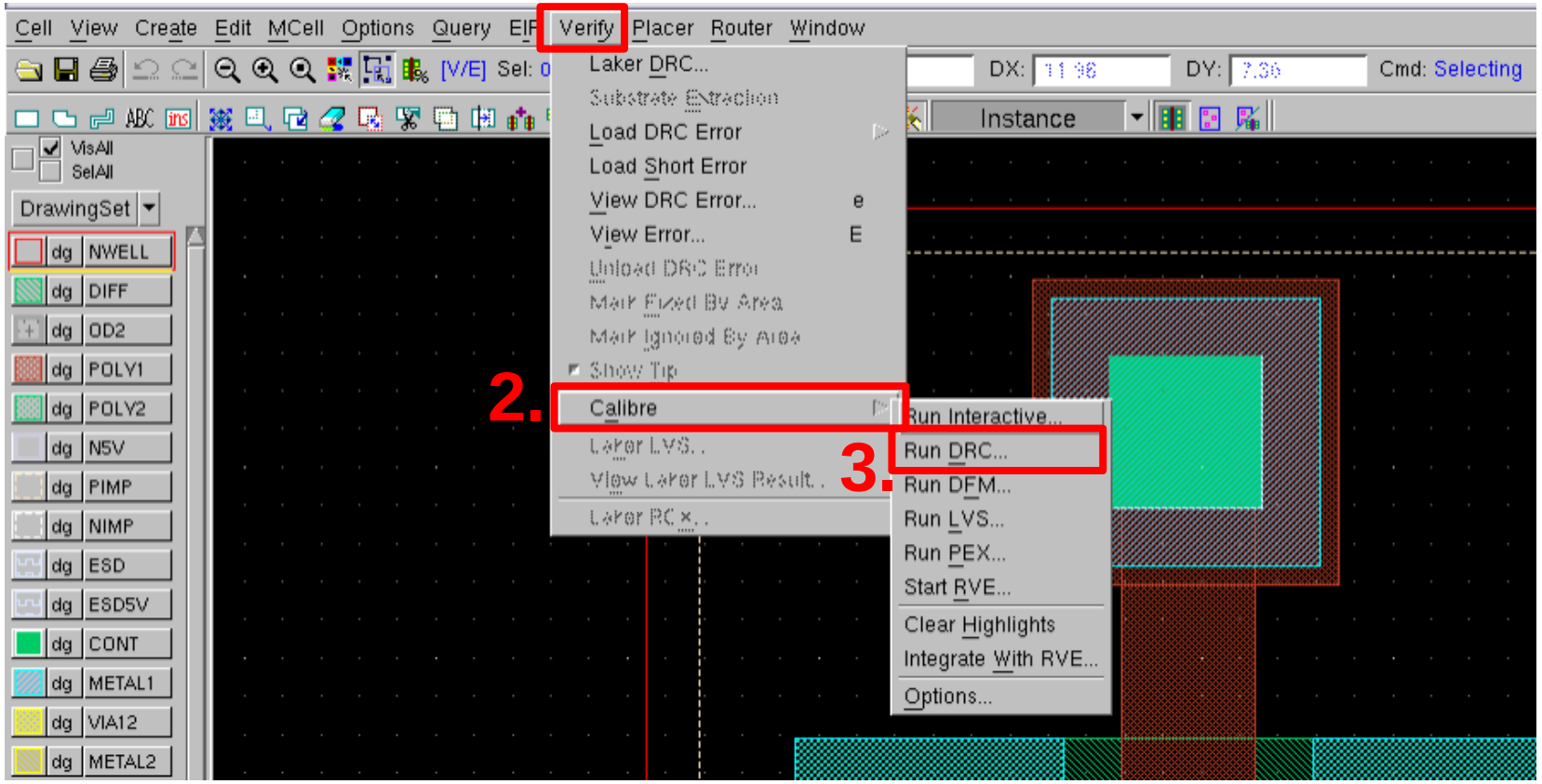




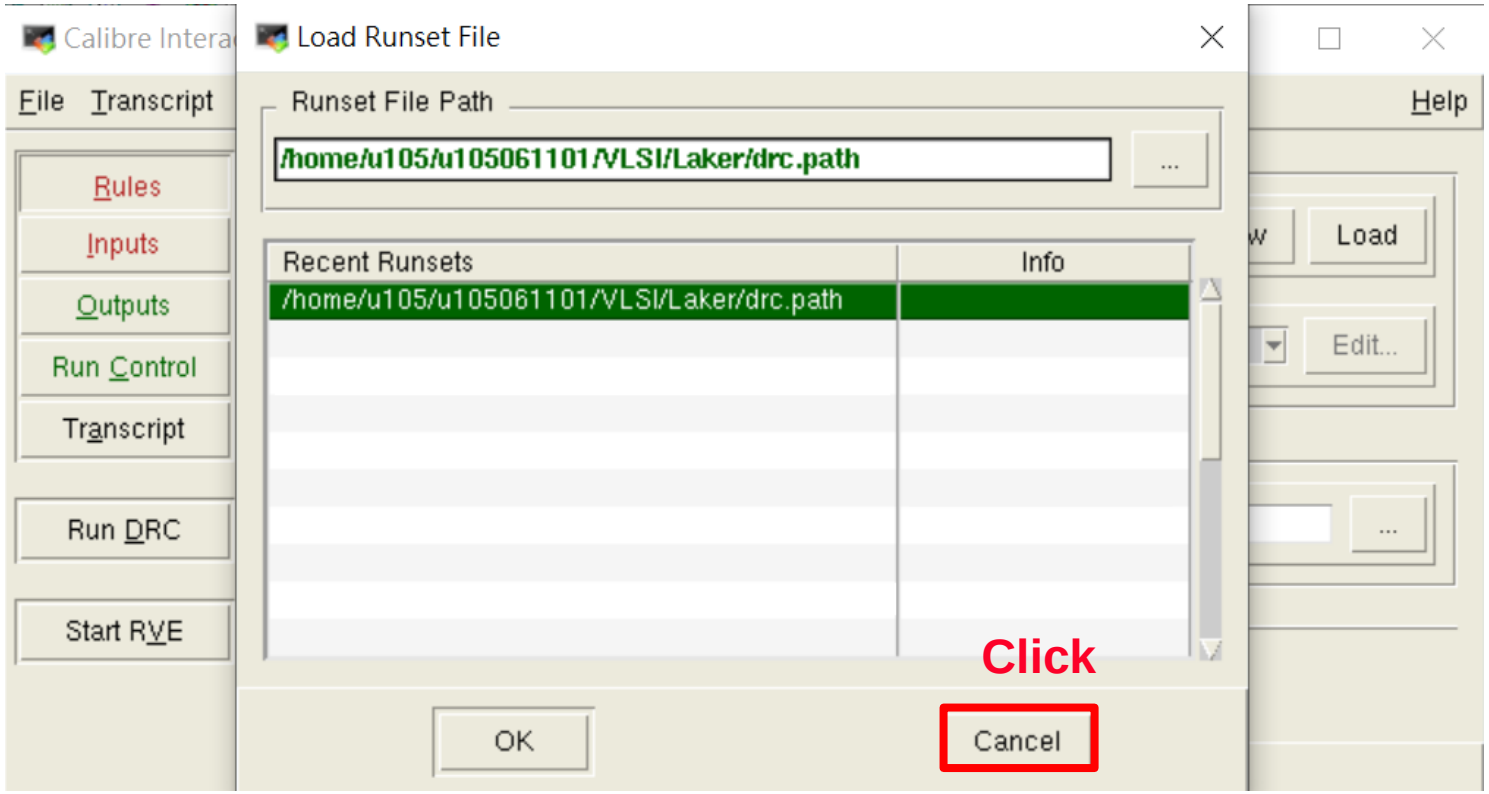
Calibre DRC Flow

DRC

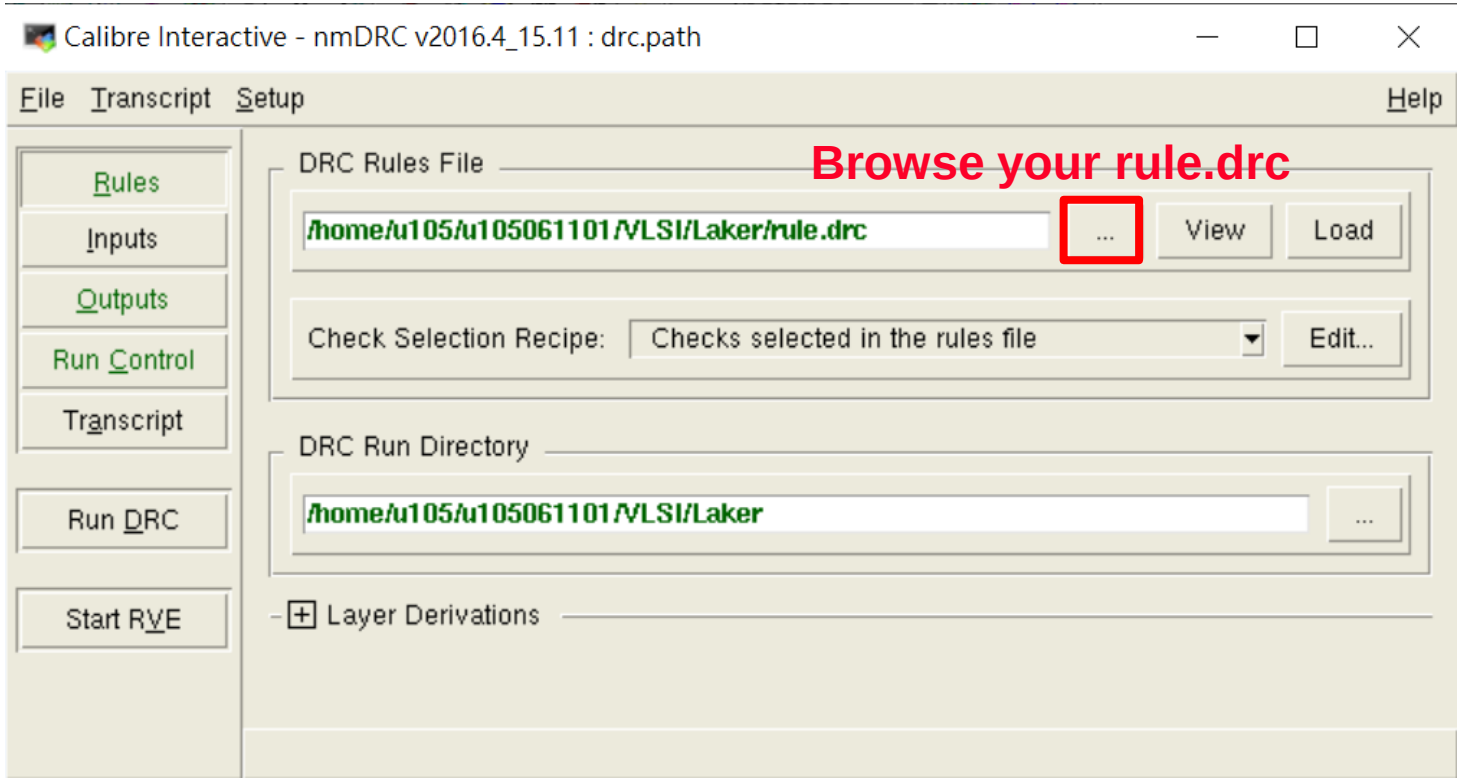
- Design Rule Check
  - To check if the layout violates fabrication rule



DRC

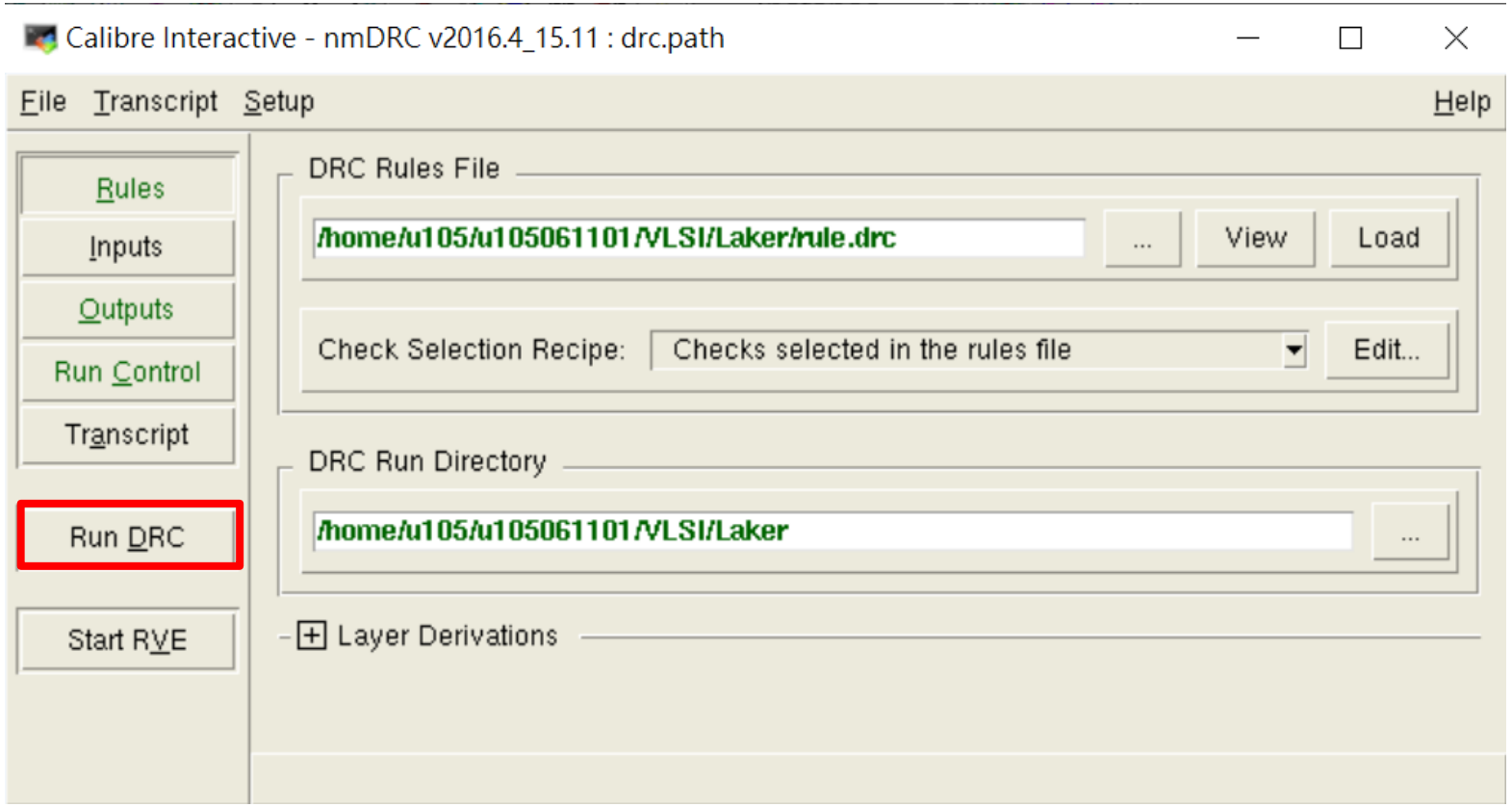

Calibre Intera
File Transcript
Rules
Inputs
Outputs
Run Control
Transcript
Run DRC
Start RVE
Load Runset File
Runset File Path
/home/u105/u105061101/VLSI/Laker/drc.path
...
Recent Runsets
Info
/home/u105/u105061101/VLSI/Laker/drc.path
Click
OK
Cancel
Help
Load
Edit...

DRC – Rules

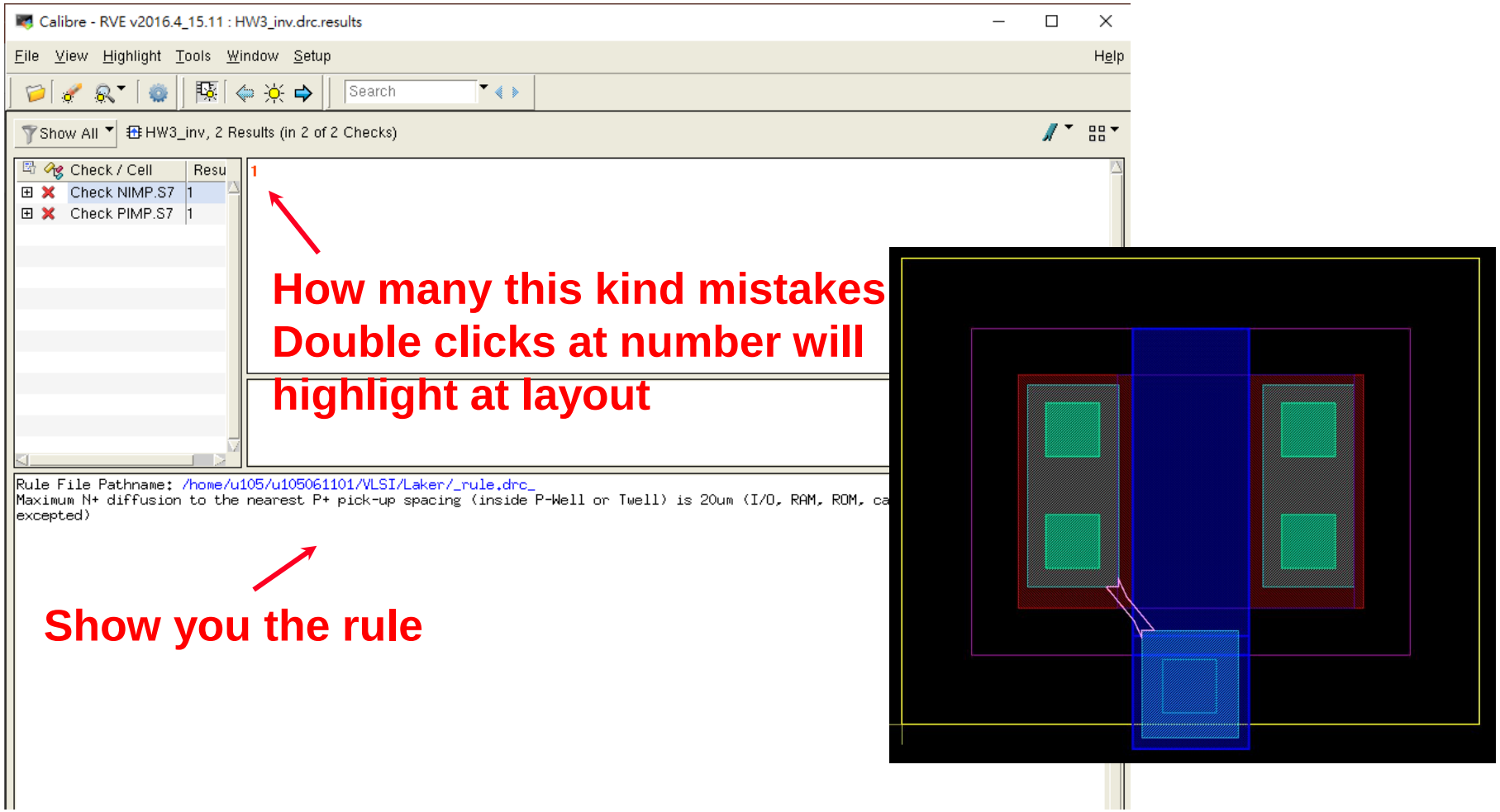

Calibre Interactive - nmDRC v2016.4_15.11 : drc.path
File
Transcript
Setup
Help
Rules
Inputs
Outputs
Run Control
Transcript
Run DRC
Start RVE
DRC Rules File
Browse your rule.drc
/home/u105/u105061101/VLSI/Laker/rule.drc
...
View
Load
Check Selection Recipe:
Checks selected in the rules file
Edit...
DRC Run Directory
/home/u105/u105061101/VLSI/Laker
...
Layer Derivations

DRC – Run

- Run DRC



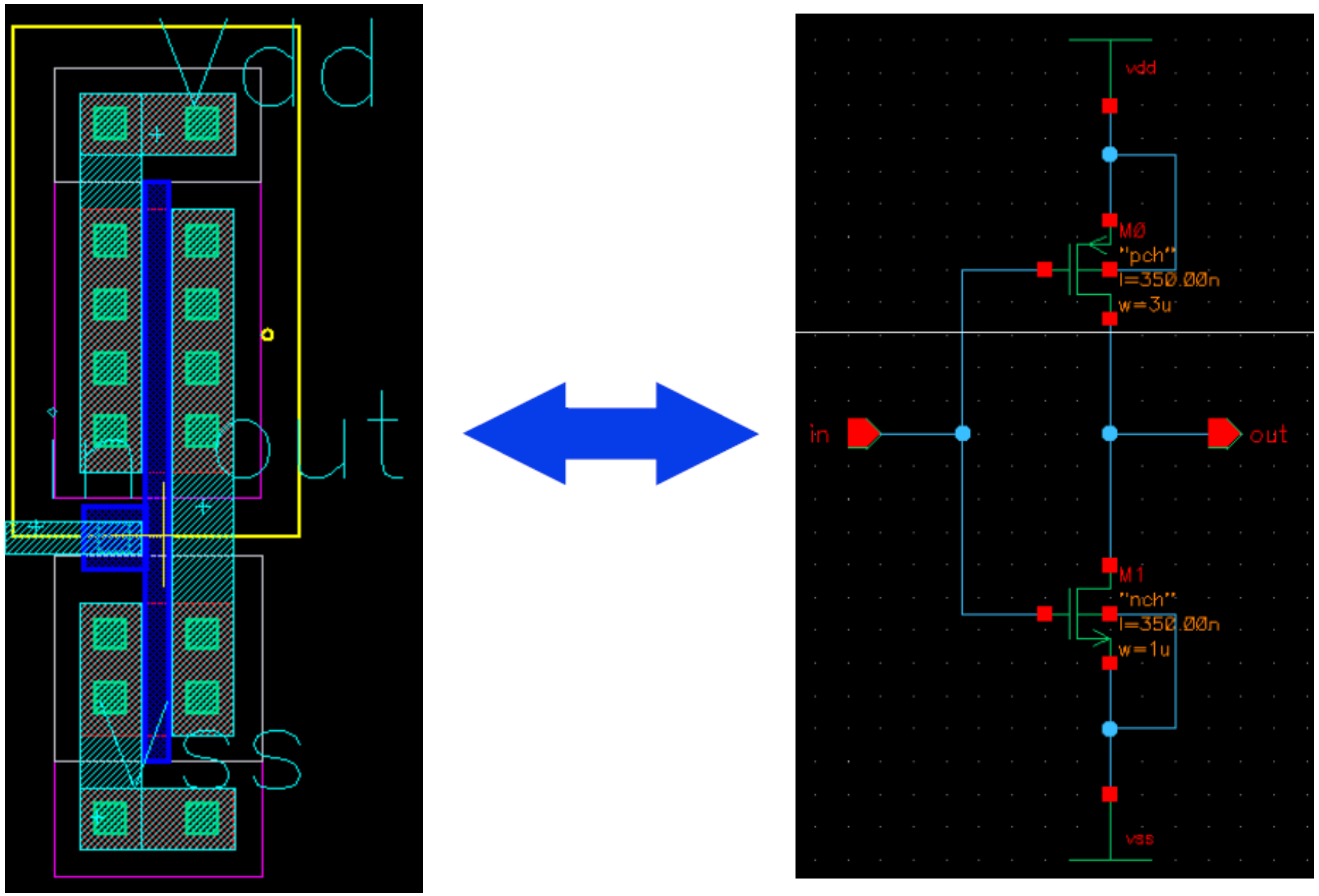
DRC – Results


Calibre - RVE v2016.4_15.11 : HW3_inv.drc.results
File View Highlight Tools Window Setup Help
Search
Show All
HW3_inv, 2 Results (in 2 of 2 Checks)
Check / Cell
Resu
Check NIMP.S7 1
Check PIMP.S7 1
1
How many this kind mistakes
Double clicks at number will
highlight at layout
Rule File Pathname: /home/u105/u105061101/VLSI/Laker/_rule.drc_
Maximum N+ diffusion to the nearest P+ pick-up spacing (inside P-Well or Twell) is 20um (I/O, RAM, ROM, ca
excepted)
Show you the rule

Calibre LVS Flow

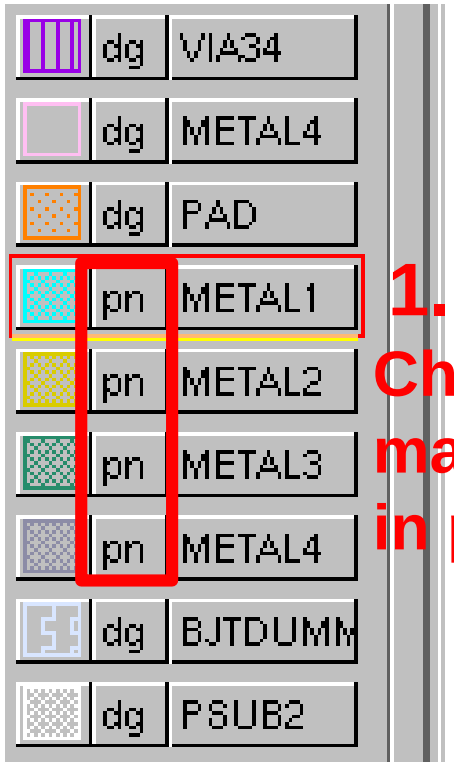
LVS

- Layout v.s. Schematic
  - To check whether layout and schematic are the same

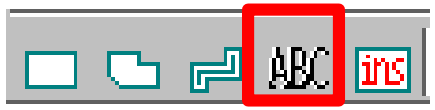


LVS – PIN (1/2)

- Create the pin

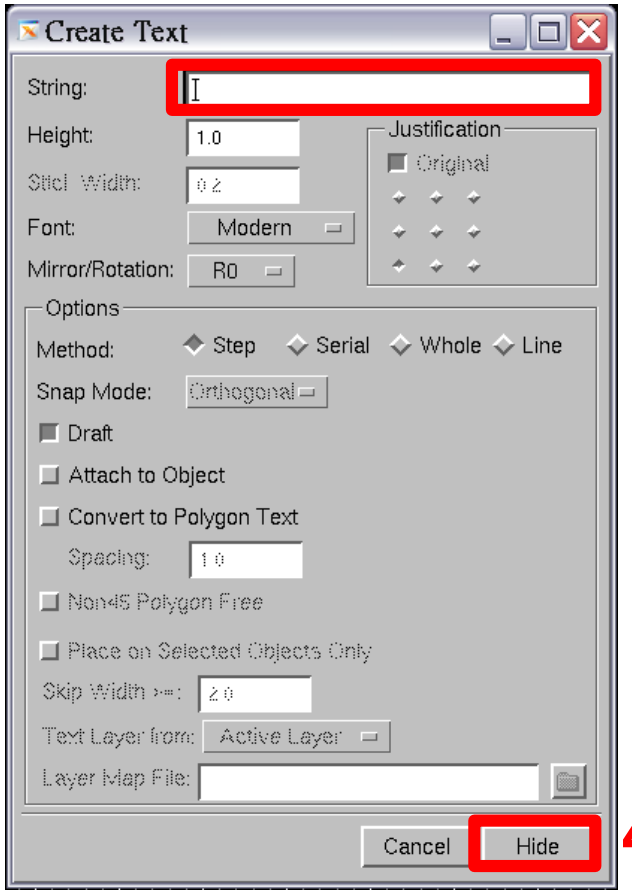


1. Choose one material in pn type



2.

3. Names of I/O or VDD or GND

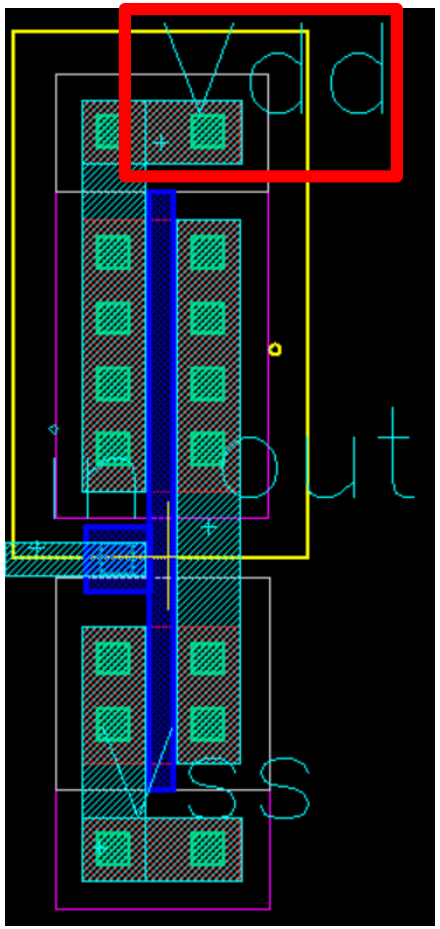


4.

LVS – PIN (2/2)

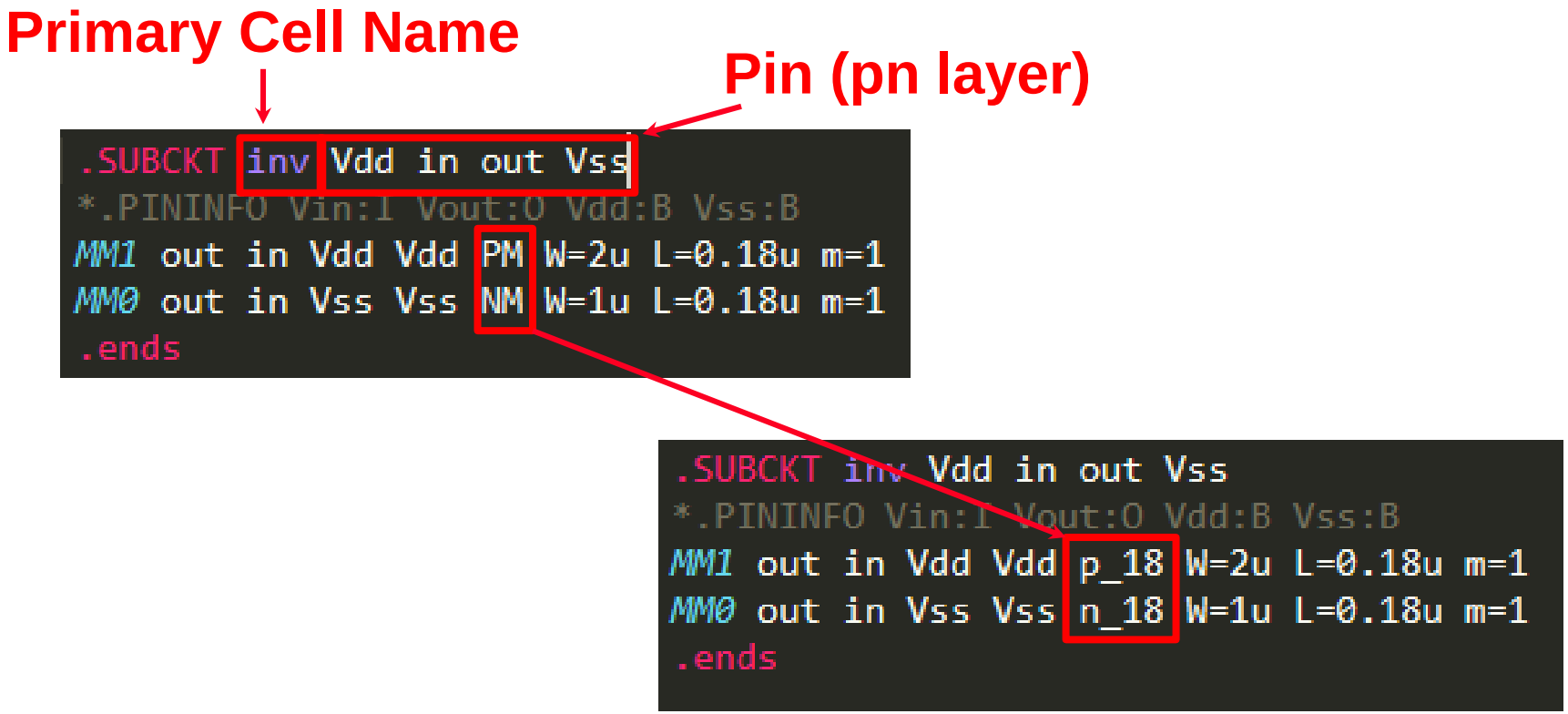
- Put the pin on the corresponding position

This sign must touch that kind of metal



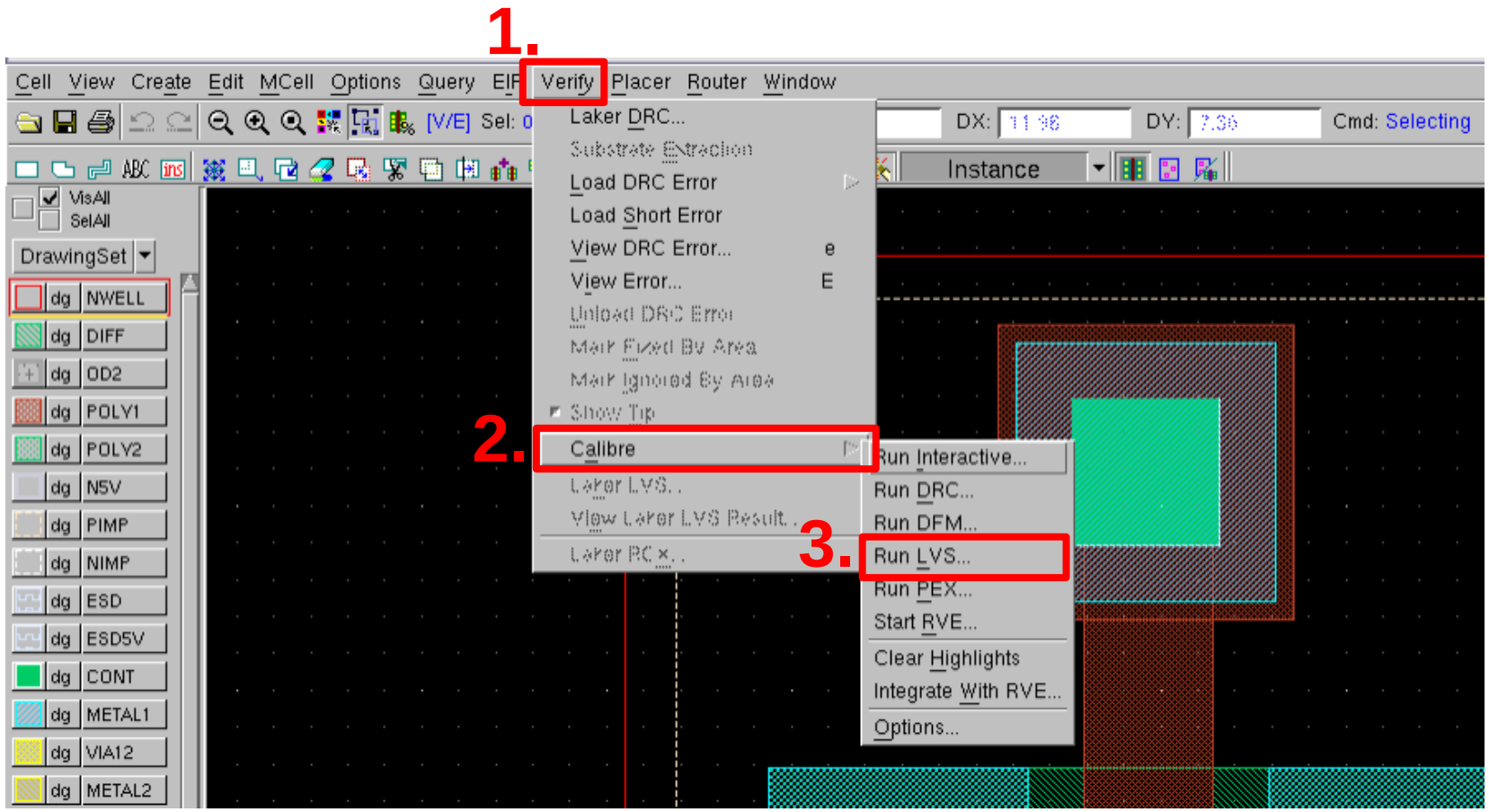
Netlist File

- The netlist has to be in SUBCKT type
- Change PM to P_18, NM to N_18

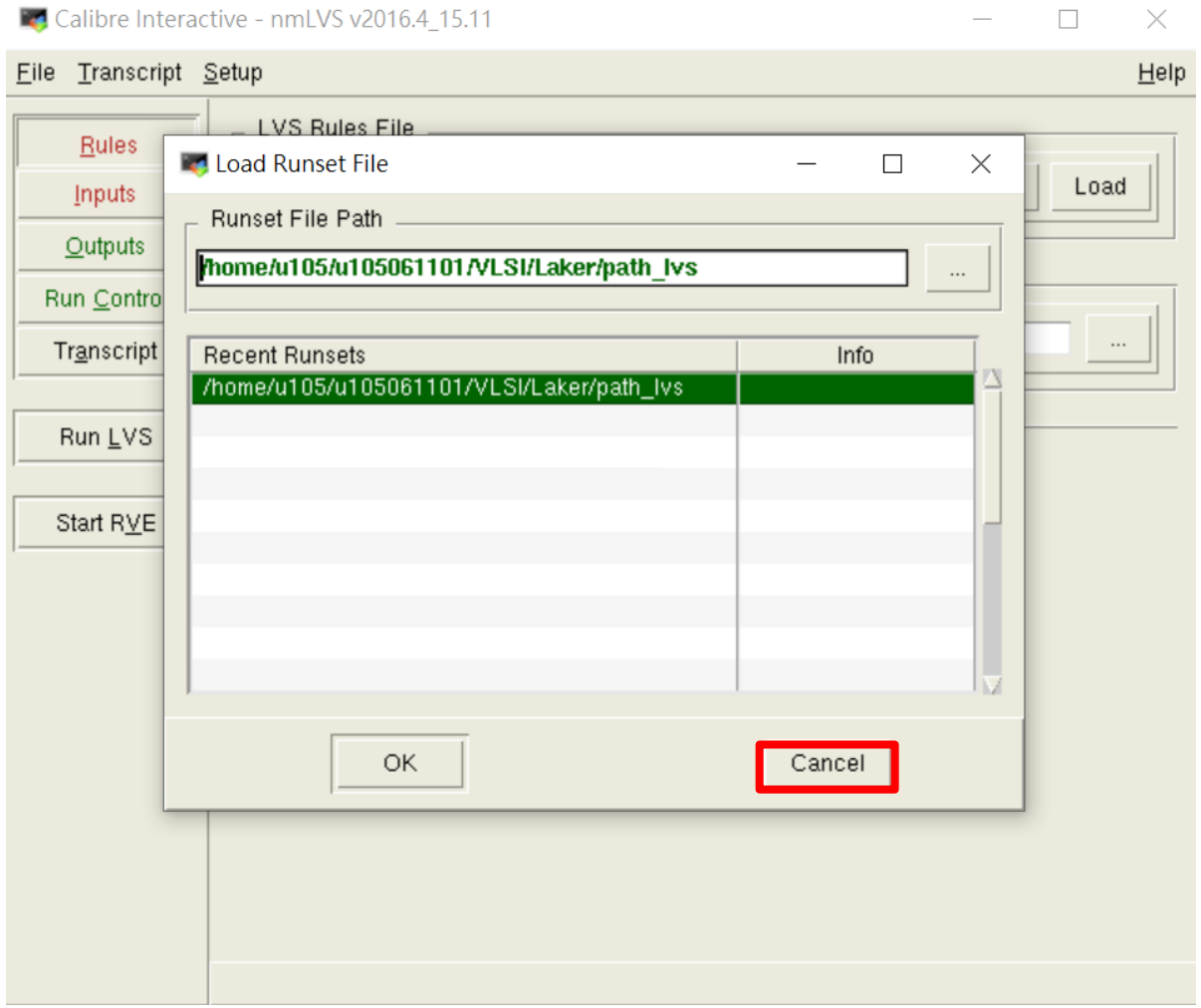


LVS

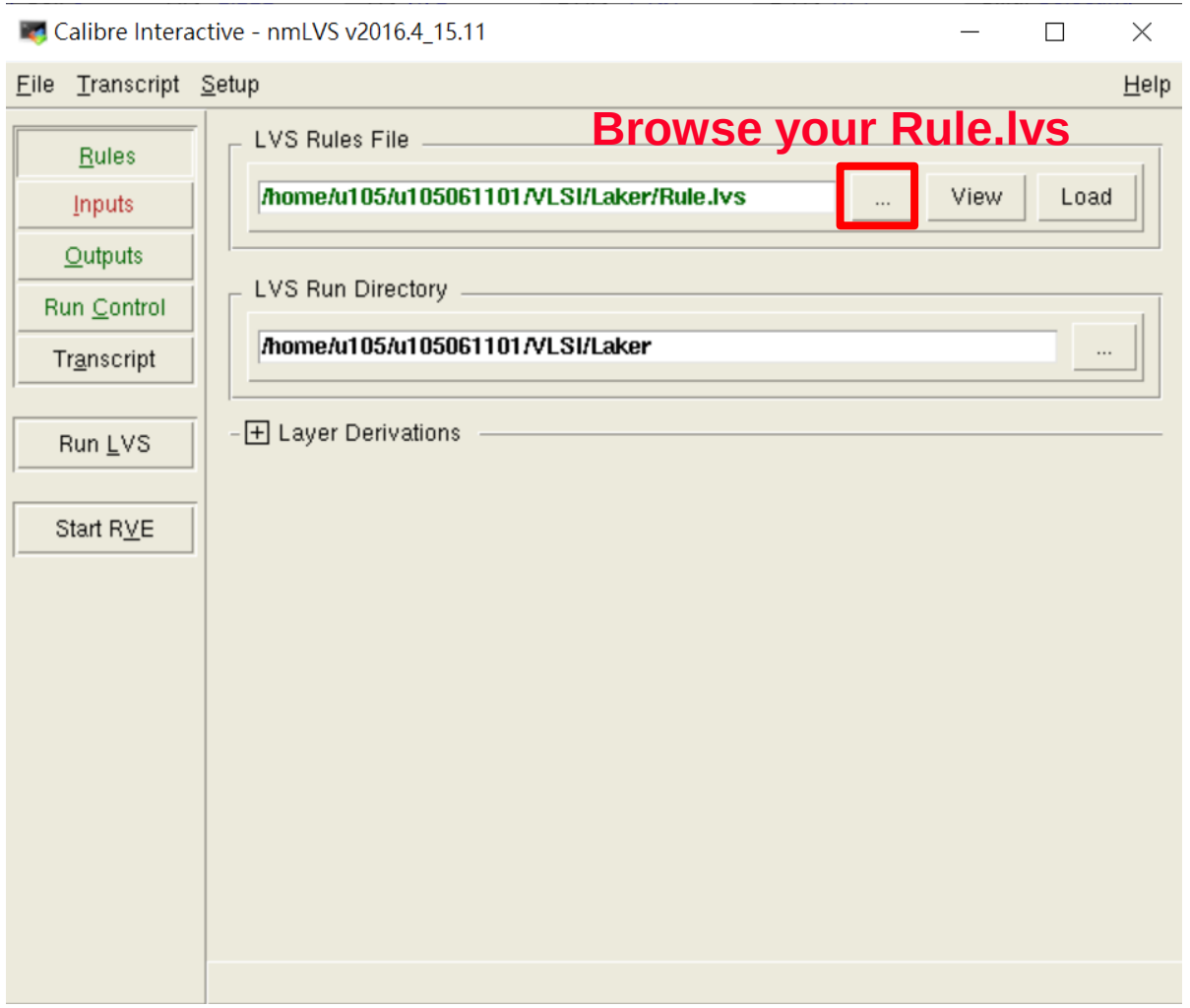
- Verify → Calibre → Run LVS



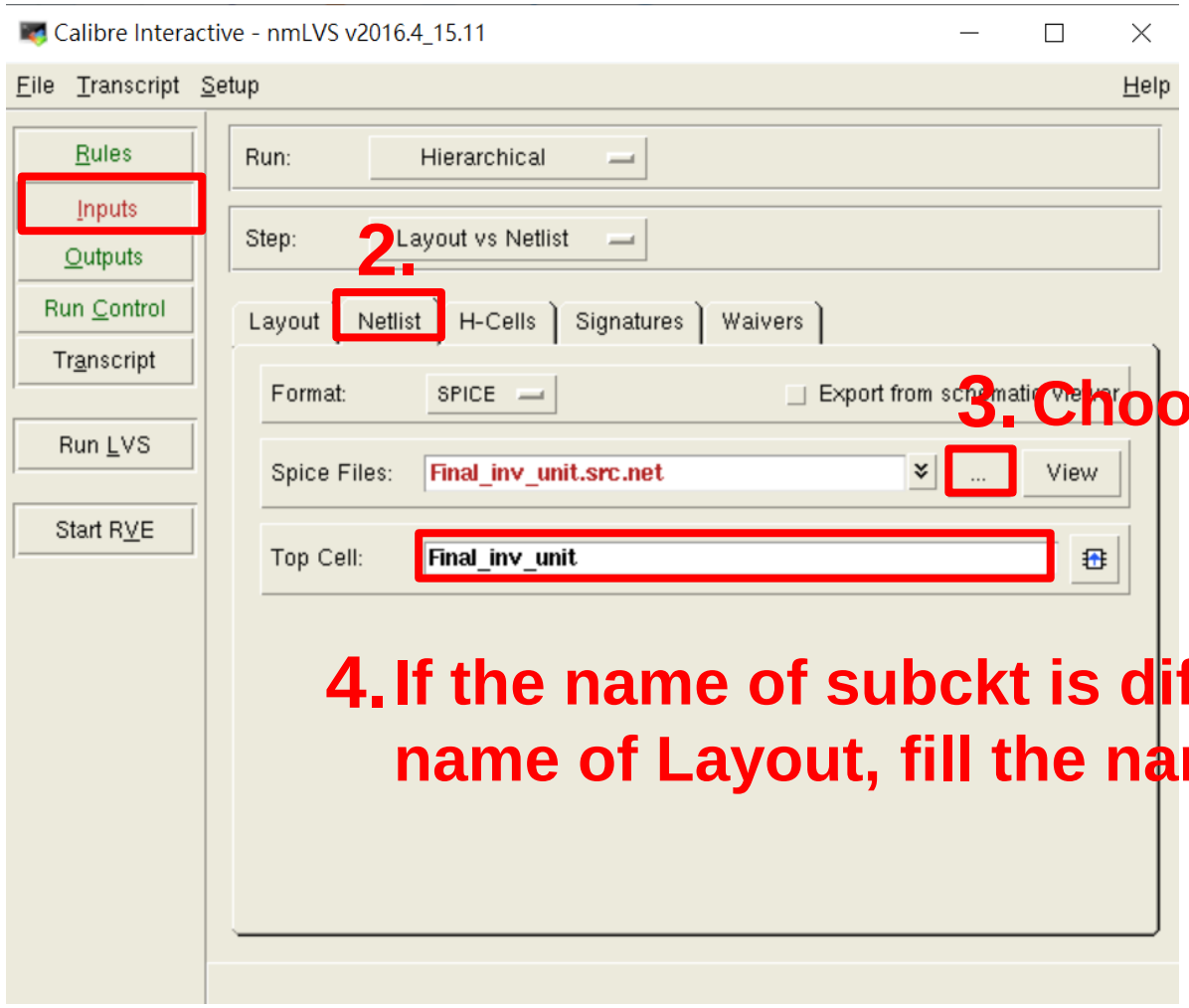
LVS


Calibre Interactive - nmLVS v2016.4_15.11
File
Transcript
Setup
Help
Rules
Inputs
Outputs
Run Contro
Transcript
Run LVS
Start RVE
LVS Rules File
Load
Load Runset File
Runset File Path
/home/u105/u105061101/VLSI/Laker/path_lvs
Recent Runsets
Info
/home/u105/u105061101/VLSI/Laker/path_lvs
OK
Cancel

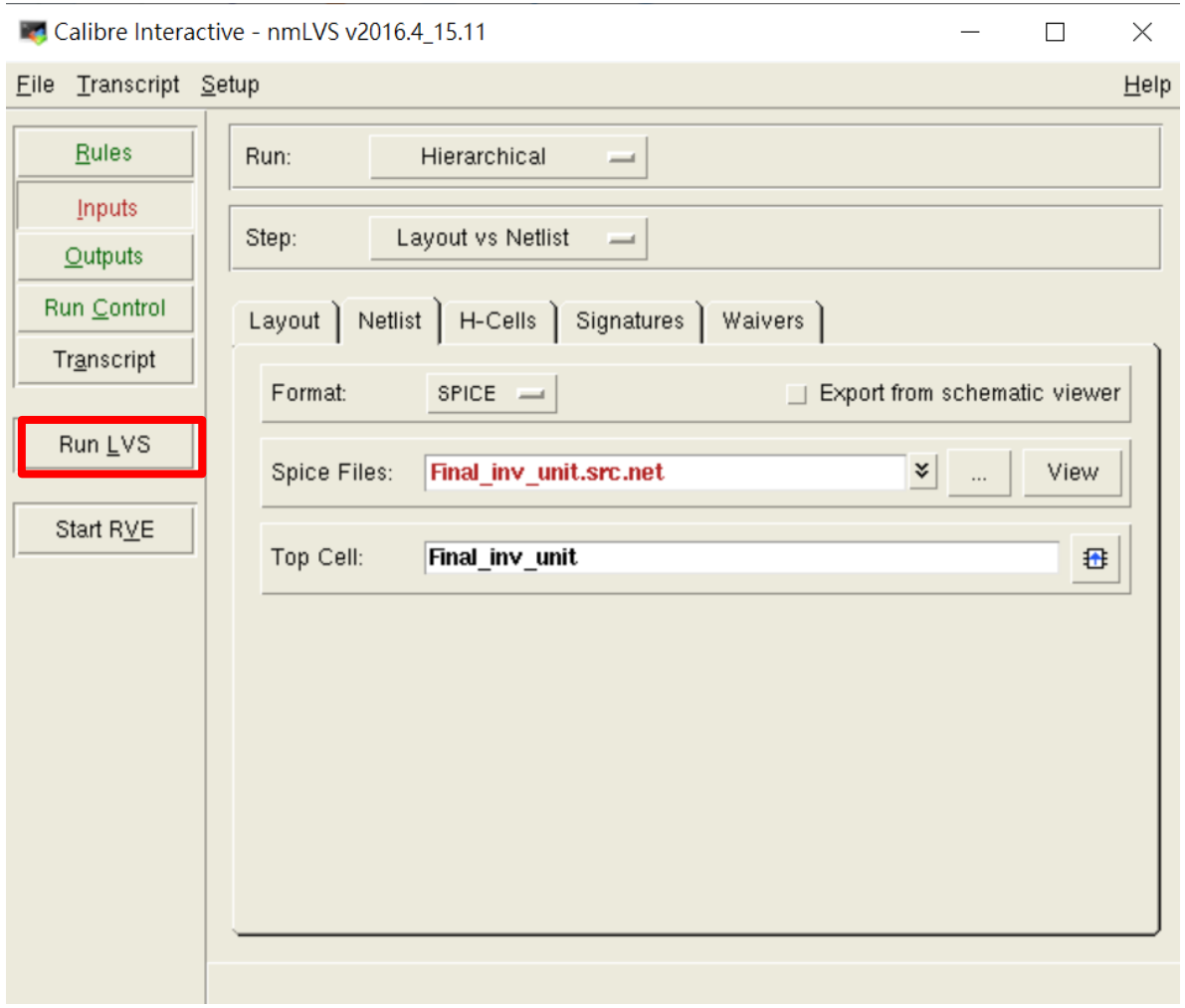
LVS – Rules


Calibre Interactive - nmLVS v2016.4_15.11
File
Transcript
Setup
Help
Rules
Inputs
Outputs
Run Control
Transcript
Run LVS
Start RVE
Browse your Rule.lvs
LVS Rules File
/home/u105/u105061101/VLSI/Laker/Rule.lvs
...
View
Load
LVS Run Directory
/home/u105/u105061101/VLSI/Laker
...
Layer Derivations

LVS – Inputs

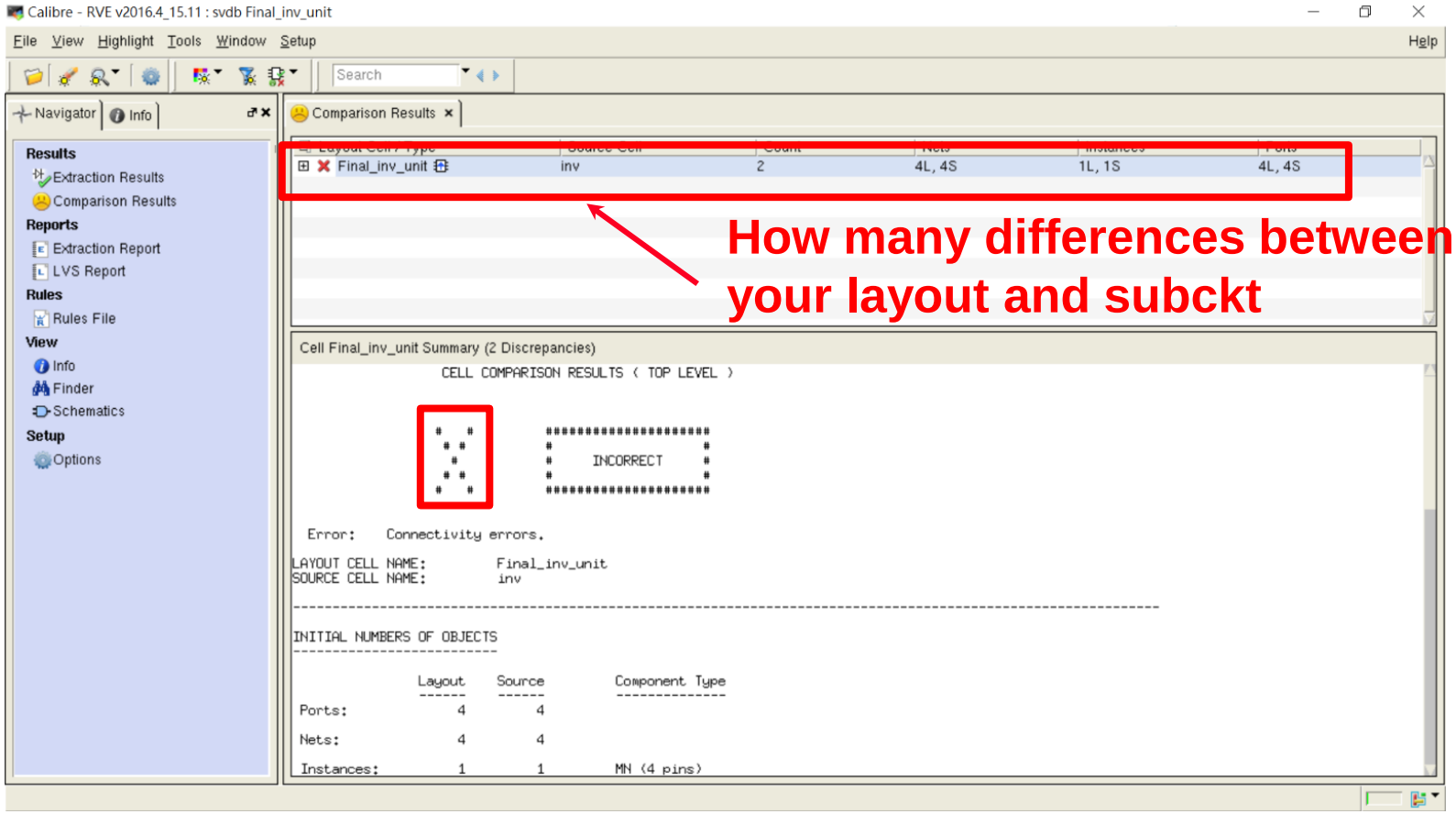

Calibre Interactive - nmLVS v2016.4_15.11
File Transcript Setup Help
Rules
Inputs
Outputs
Run Control
Transcript
Run LVS
Start RVE
Run: Hierarchical
Step: Layout vs Netlist
Layout Netlist H-Cells Signatures Waivers
Format: SPICE
Export from schematic viewer
Spice Files: Final_inv_unit.src.net ... View
Top Cell: Final_inv_unit
1.
2.
3. Choose your *.spi file
4. If the name of subckt is different with the name of Layout, fill the name of subckt here

LVS – Run


Calibre Interactive - nmLVS v2016.4_15.11
File
Transcript
Setup
Help
Rules
Inputs
Outputs
Run Control
Transcript
Run LVS
Start RVE
Run:
Hierarchical
Step:
Layout vs Netlist
Layout
Netlist
H-Cells
Signatures
Waivers
Format:
SPICE
Export from schematic viewer
Spice Files:
Final_inv_unit.src.net
...
View
Top Cell:
Final_inv_unit

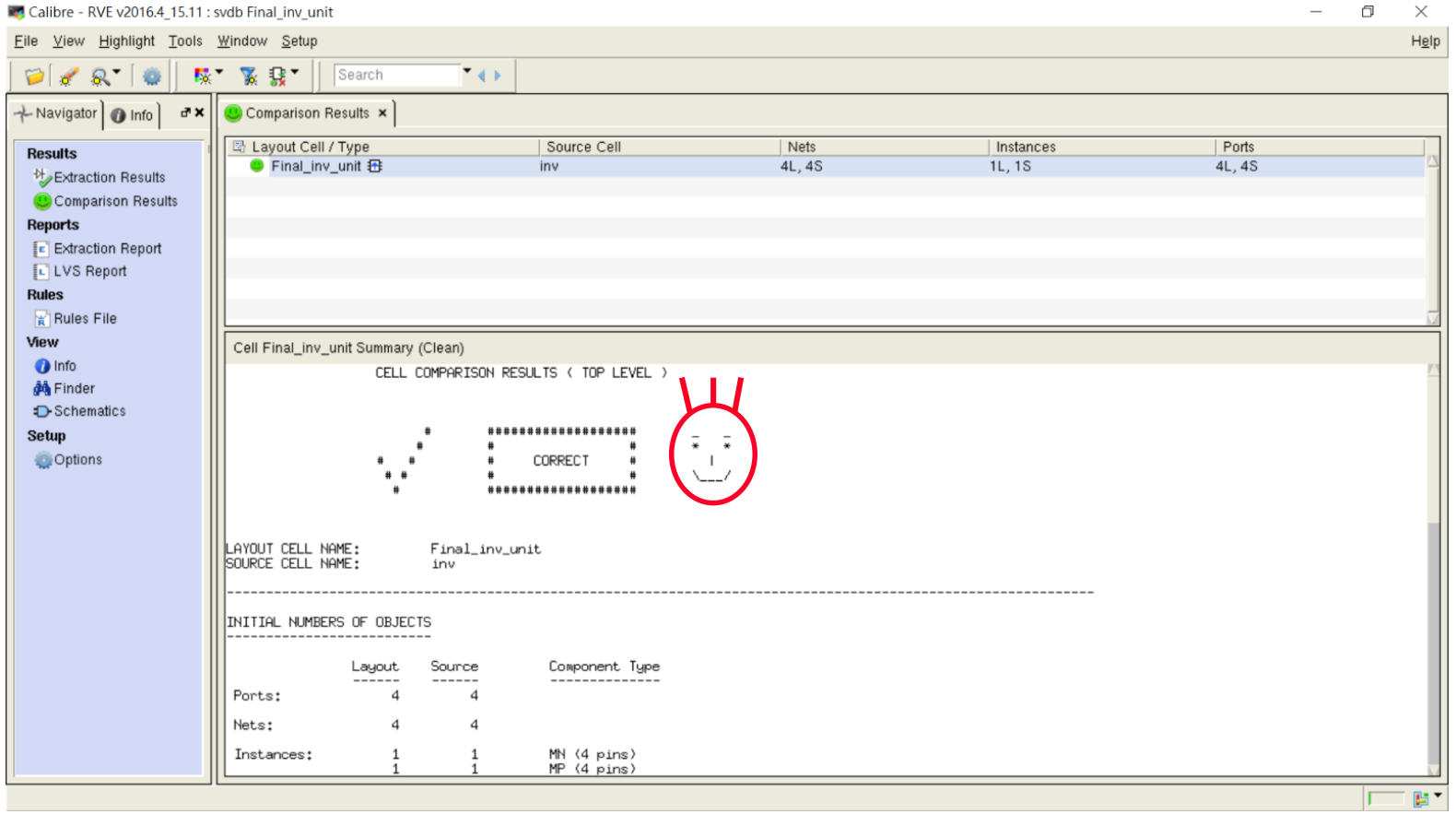
LVS – Results

- Result
  - If your layout is different with subckt, you will get a big X



LVS – Results

- Result
  - If your layout is the same as subckt, you will get a smile

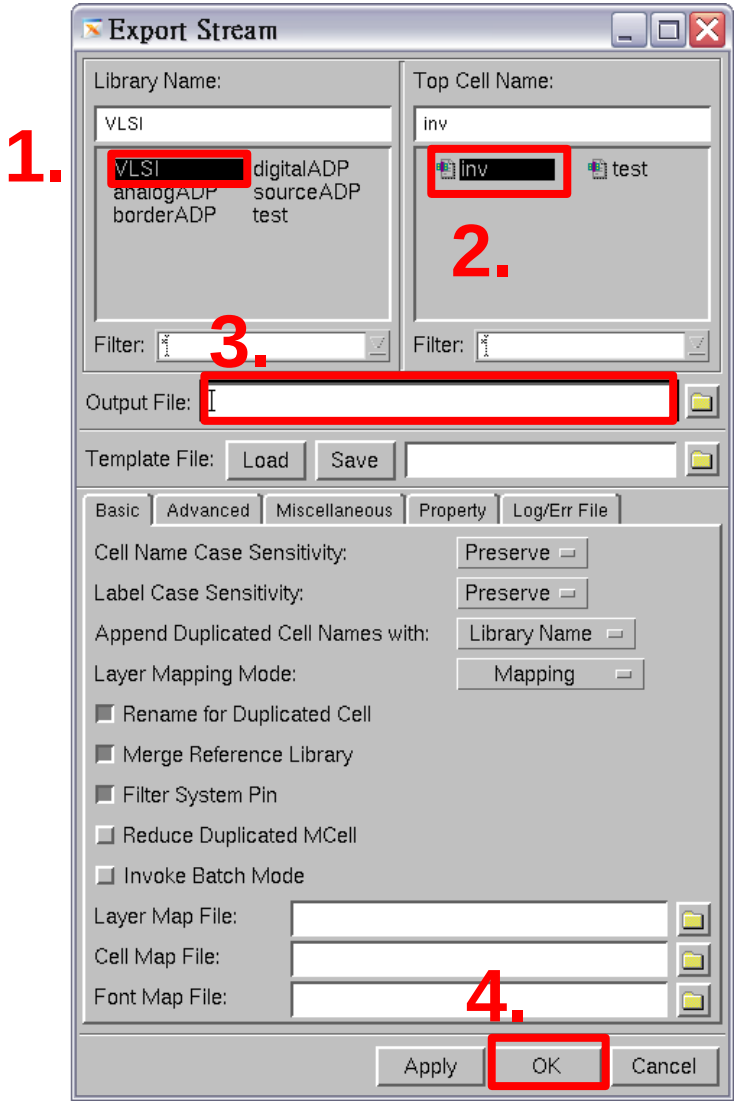


Export / Import Design

Laker – Output Design

- Stream Out
  - File → Export → Stream
    - → Choose Library
    - → Choose Cell
    - → Output File Name(Ex: inv.gds)
    - → OK

- GDS : A file used to store the position of your layout.



Laker – Import Design

- Stream In
  - File → Import → Stream

(It'll create a new Library)

→ Browse .gds file

→ New Library name

→ Technology file (*.tf)

→ OK