Wesley Wu

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Education

University of Illinois at Urbana-Champaign Aug 2020 - Dec 2023
Bachelor of Science in Computer Engineering GPA: 3.76/4.00

Relevant Coursework

Computer Organization & Design, Accelerator Architectures, Digital Systems Laboratory, IC Device Theory and Fabrication, Semiconductor Devices, Computer Systems Engineering, Applied Parallel Programming, Digital Signal Processing, Data Structures, Artificial Intelligence

Technical Skills

- **Languages**: SystemVerilog, C, C++, CUDA, Python, Java, x86 ASM
- **Verification Methodologies:** UVM
- **Software:** ModelSim, Altera Quartus, Synopsys Tools - VCS, Verdi, DVE; Linux, VSCode
- **Workflow**: Git, GitHub, Gerrit, Jira, Agile, ClearCase

Work Experience

Qualcomm **San Diego, CA**
SoC APSS Integration DV Intern *May 2023-Current*

- Incorporated functional coverage for an in-house methodology, enhancing quality of mobile SoC design verification
- Developed verification plans for functional coverage, ensuring comprehensive coverage for mobile SoC design verification

Motorola Solutions **Schaumburg, IL**
Embedded Android Engineer Co-Op *Nov 2022-May 2023*

- Implemented dump function for fastboot protocol, enabling user to check image in any partition in case of corruption
- Added special fastboot commands, enabling developers to change flag bits in system images without need for remounting
- Updated fastbootd user-mode display, giving developers more useful information about the device they're working on
- Enabled flashing lock/unlock for fused devices, allowing developers to flash different HLOS images in fastbootd user mode

Android Platform Software Engineering Intern *May 2022-Aug 2022*

Improved bootloader security on Aloha radio (work-in-progress software-defined radio running on Android)

- Devised logic in C to prevent malicious users from reverting to old, vulnerable firmware or modifying vital image data
- Upgraded pre-existing preflash validation in C, ensuring the device doesn't brick in fastboot mode or during boot
- Prevented device bricking in bootloader stage, allowing user to recover the device in the case of image data corruption
- Added new AP factory properties, strengthening Sanmina factory flow control to prevent product processing exceptions

Projects

Homomorphic Encryption Accelerator | *SystemVerilog, Synopsys VCS, Verdi, C* Jan 2023-May 2023

- Designed a hardware accelerator to speed up encrypted computation, with a focus on encrypted-space multiplication
- Drafted top-down design of accelerator, from loading in input values to computation stages to low-level functional units
- Wrote simple encrypted-space multiplication workload kernel in C to compare accelerator performance to baseline CPU
- Implemented each layer of the design hierarchy in HDL and verified layers using Synopsys VCS and Verdi simulator

391OS | *C, x86 ASM* Mar 2023-May 2023

- Implemented an OS kernel which integrates setup of IDT, a keyboard driver, RTC, PIT, multiple terminals, ext2fs with support for execution of six tasks from program images within filesystem, paging, and ten system call interfaces
- Employing GRUB to boot OS image file and using QEMU virtual machine with GDB to perform step-by-step debugging

RISC-V Processor | *SystemVerilog, Synopsys VCS + Verdi* *Oct 2022-Dec 2022*

- Implemented datapath and controller FSM for non-pipelined processor whose ISA is a subset of the RV32I ISA
- Improved the processor's performance by designing and verifying a 2-way set-associative cache
- Performed RTL simulation on the design at each stage of development, using Synopsys Verdi to verify design functionality
- Implemented basic 5-stage in-order pipeline with data forwarding and integration with L1 caches and a cache arbiter

FPGA Crossword | *SystemVerilog, C, Altera Quartus, ModelSim* *April 2022-May 2022*

- Implemented a NIOS-II processor on a MAX10 DE10-Lite FGPA board and interfaced it with a custom graphics controller
- Upgraded the graphics controller to draw a game board, a main menu, and a cell highlight
- Devised a state machine to communicate to the graphics controller whether to display the main menu or the game board
- Expanded on-chip memory to load it with the puzzles' clues and answers after serializing them into 8-bit ASCII values
- Leveraged pointer arithmetic in C to read the clues, then parse together and store the clues and answers
- Implemented check and reveal logic in C, and passed win condition back to state machine and stopwatch from C code

Activities

IEEE-HKN Alpha Chapter *Dec 2021-Curr*
Member

Help provide student services to the UIUC ECE community, including, but not limited to:

- Administering one-on-one tutoring and leading exam review sessions for core ECE classes
- Conducting resume reviews, mock interviews, and similar career-oriented events