CPE301 – SPRING 2019

Design Assignment 2B

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Primary Github address: https://github.com/westbrian2/Spring2019

Directory: Spring2019/DesignAssignments/DA2A\_submission

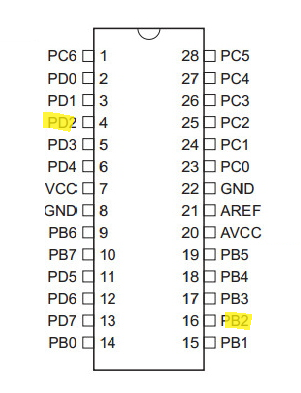
Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

Components: Xplained Mini board, wires, Logic Analyzer

Block Diagram:



1. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A**

None given

1. **DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A**

ASM CODE

.include <m328pdef.inc>

.org 0 ; body of program

jmp main ;

.org 2 ; external interrupt

jmp EX0\_ISR

main:

;setting up stack

ldi r20,high(RAMEND)

out sph,r20

ldi r20,low(RAMEND)

out spl, r20

;setting up timer

ldi r20,4 ; prescaler 1024

sts tccr1b,r20;

ldi r20,0x2;INT0 is falling edge triggered

sts EICRA,r20

sbi ddrb,2; portb2 is output

sbi portb,2; turning off led

sbi portd,2; pull up resistor

ldi r20,1<<INT0; enables INT0

out EIMSK,r20

sei; enables interrupts

end:

jmp end

delay:

lds r22,tcnt1h; getting upper bits from counter

lds r23,tcnt1l; getting lower

cpi r23,0x25; comparing against target value

brsh upper

jmp delay ; if target value isn't met restart loop

upper:

cpi r22,0x26

brlt delay

ret

EX0\_ISR:

ldi r20,0

sts tcnt1h,r20; resetting timer

sts tcnt1l,r20;

in r21,portb;

ldi r22,(1<<2);

eor r21,r22; toggles LED

out portb,r21;

rcall delay ; starting delay

eor r21,r22

out portb,r22;

reti ; returns

C CODE

#define F\_CPU 8000000UL

#include <util/delay.h>

#include <avr/io.h>

#include <avr/interrupt.h>

int main ()

{

DDRB = 1<<2;//PB5 as an output

PORTD = 1<<2;//pull-up activated

PORTB = 1<<2;

EICRA = 0x2;//make INT0 falling edge triggered

EIMSK = (1<<INT0);//enable external interrupt 0

sei ();//enable interrupts

while (1);//wait here

}

ISR (INT0\_vect)//ISR for external interrupt 0

{

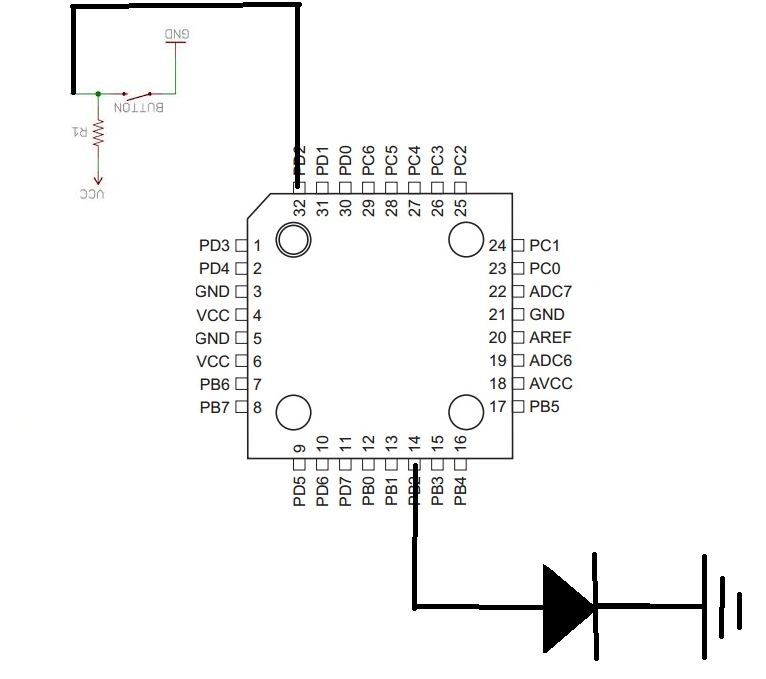
PORTB ^= (1<<2);//toggle PORTB.2

\_delay\_ms(1250);

PORTB ^=(1<<2);

}

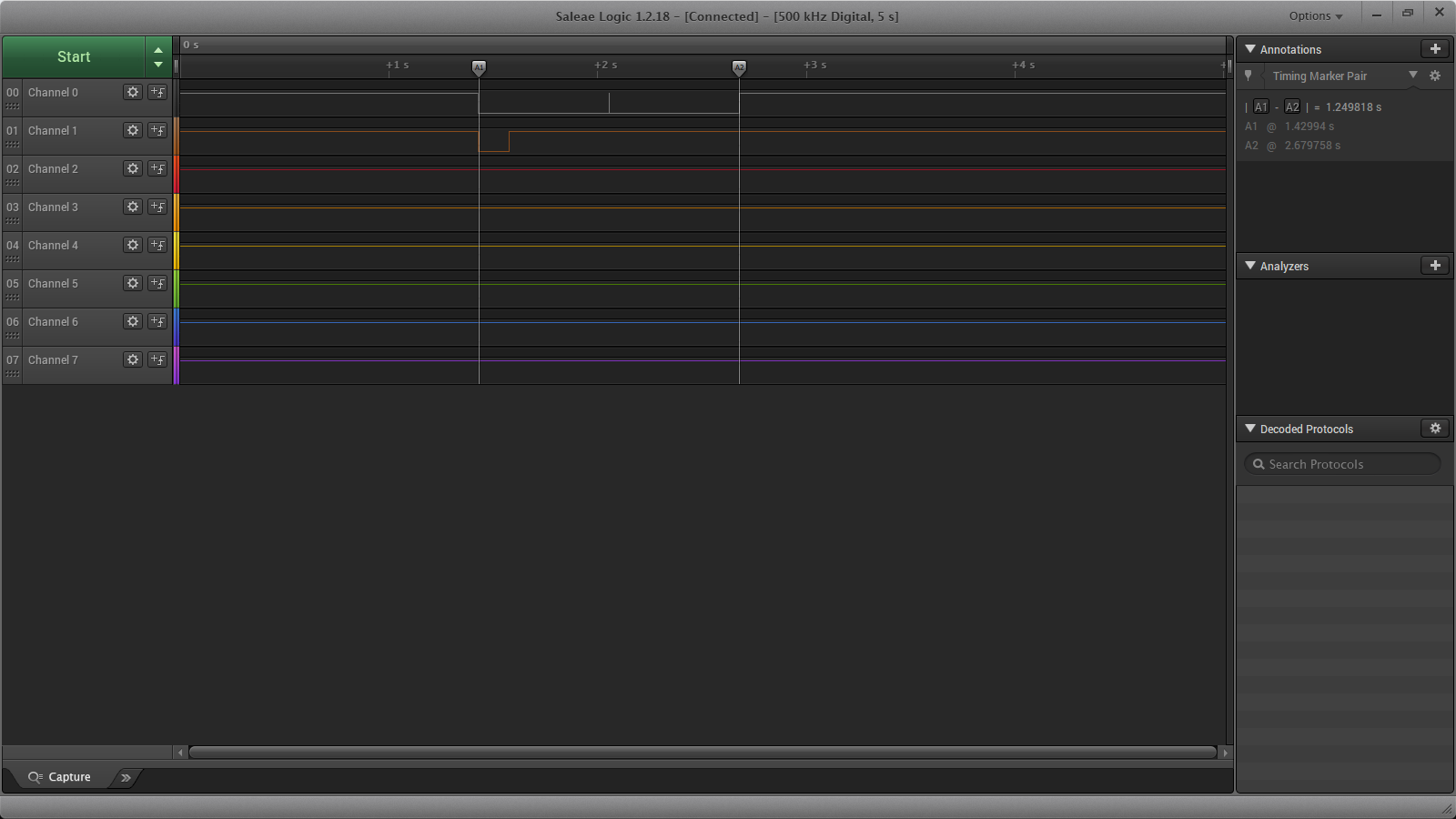
1. **SCHEMATICS**

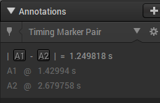


1. **SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)**

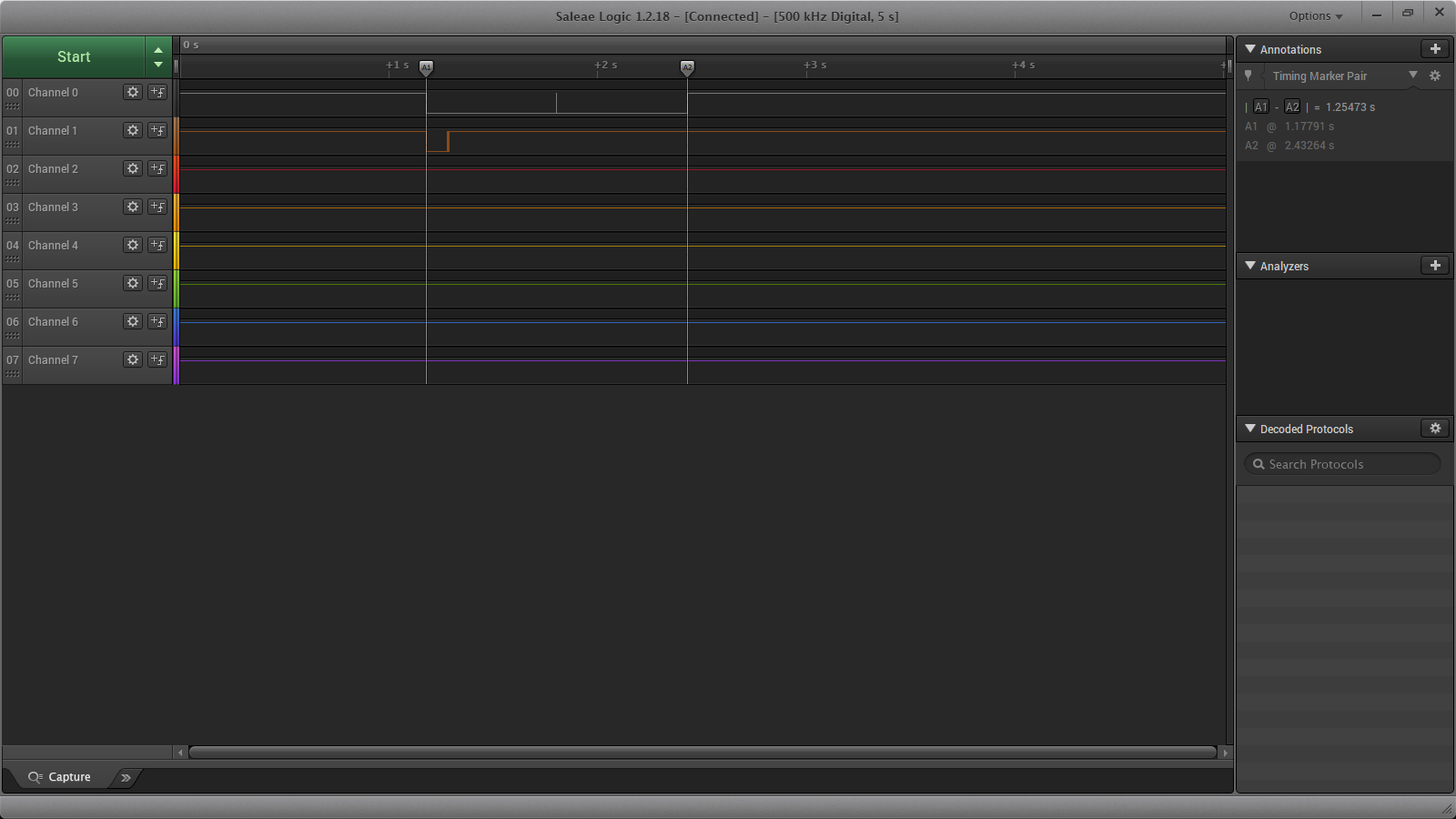
Screenshots from LOGIC

ASM



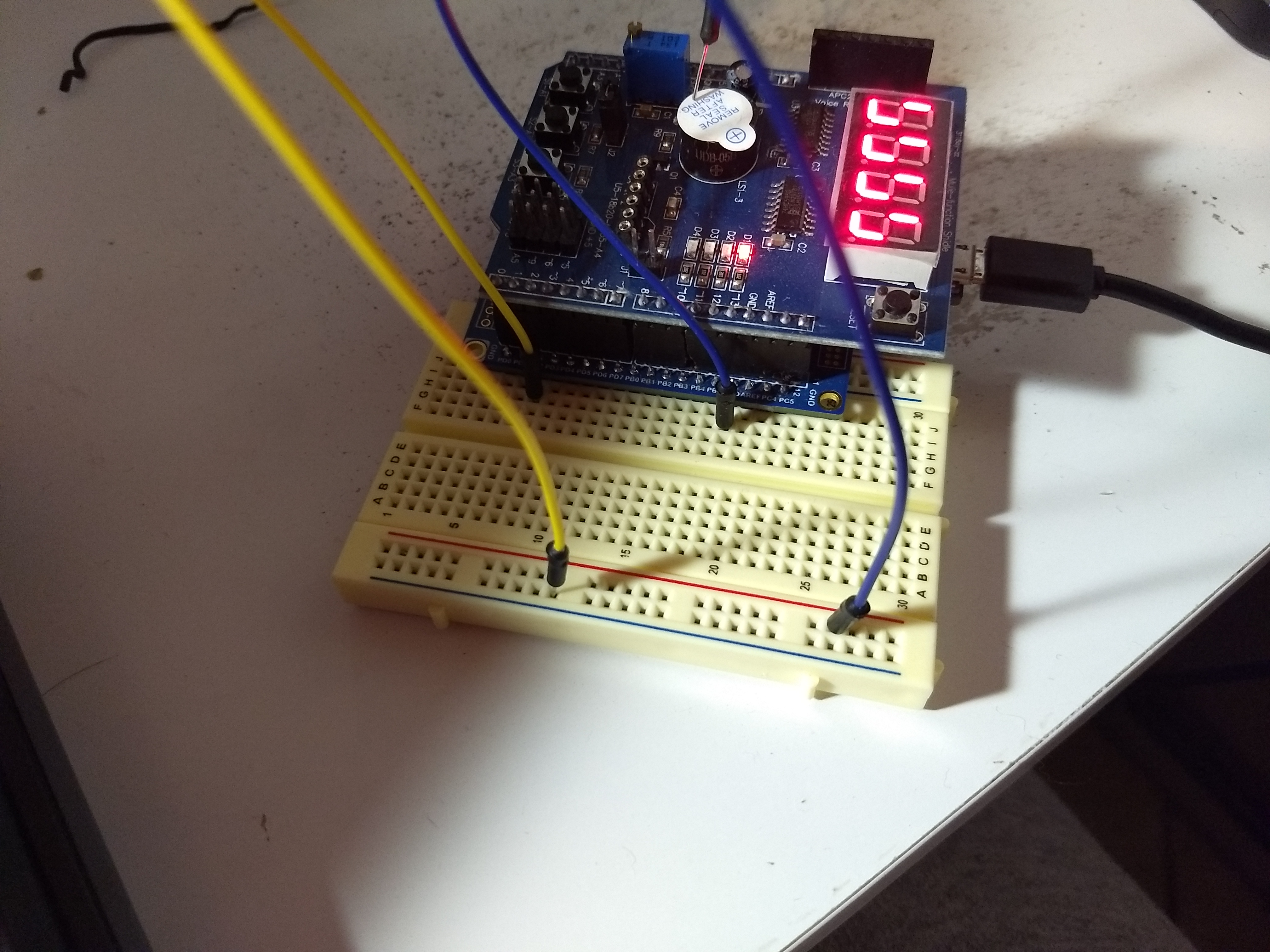
Time for event is 1.249s

C Code



 Time for event is 1.254s

1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**



The two wires were brought together to trigger the Interrupt.

1. **VIDEO LINKS OF EACH DEMO**

https://youtu.be/3B4we0\_-obA

1. **GITHUB LINK OF THIS DA**

https://github.com/westbrian2/Spring2019/tree/master/DesignAssignments/DA2B\_submission

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

Brian West