

### Flow Navigator

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### Sources Netlist

- swerv\_eh1\_reference\_design
  - Nets (1054)
  - Leaf Cells (24)
    - axi\_intc\_wrapper\_inst (axi\_intc\_wrapper)
    - clk\_and\_rst\_wrapper\_inst (clk\_and\_rst\_wrapper)
    - swerv\_wrapper\_inst (swerv\_wrapper)

### Source File Properties

swerv\_eh1\_reference\_design.v

- Enabled
- Location: /home/arup/projects/github/swerv1
- Type: Verilog
- Library: xil\_defaultlib
- Size: 25.2 KB
- Modified: Wednesday 05/08/19 10:50:55 AM
- Read-only: No

### Project Summary

Status: ✔ Complete  
 Messages: ! 1543 warnings  
 Active run: synth\_1  
 Part: xc7a100tcsg324-1  
 Strategy: Flow\_PerfOptimized\_high  
 Report Strategy: Vivado Synthesis Default Reports

### Project Summary

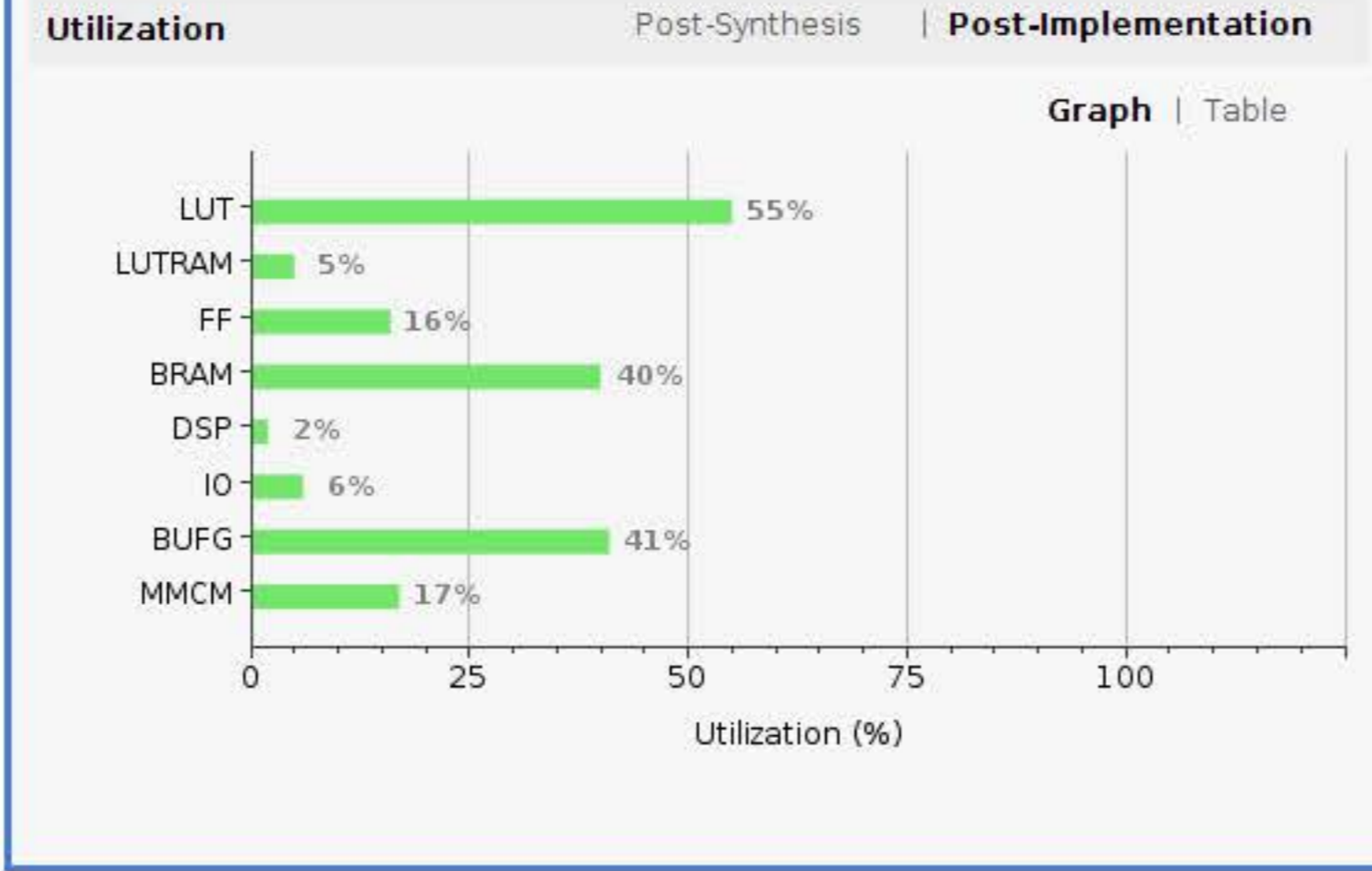
Status: ✔ Complete  
 Messages: ! 542 warnings  
 Active run: impl\_1  
 Part: xc7a100tcsg324-1  
 Strategy: Performance\_Explore  
 Report Strategy: Timing Closure Reports  
 Incremental compile: None

### DRC Violations

Summary: ! 601 warnings  
[Implemented DRC Report](#)

### Timing

Worst Negative Slack (WNS): 0 ns  
 Total Negative Slack (TNS): 0 ns  
 Number of Failing Endpoints: 0  
 Total Number of Endpoints: 54261  
[Implemented Timing Report](#)



### Power

**Total On-Chip Power: 0.4 W**  
**Junction Temperature: 26.8 °C**  
 Thermal Margin: 58.2 °C (12.6 W)  
 Effective θJA: 4.6 °C/W  
 Power supplied to off-chip devices: 0 W  
 Confidence level: Medium  
[Implemented Power Report](#)

### utilization\_1

Name	Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	F8 Muxes (15850)	Slice (15850)	LUT as Logic (63400)	LUT as Memory (19000)	LUT Flip Flop Pairs (63400)	Block RAM Tile (135)	DSPs (240)	Bonded IOB (210)	BUFGCTRL (32)	MM
swerv_eh1_reference_...	34578	20557	204	28	10583	33625	953	9641	54	4	12	13	
axi_intc_wrapper_in...	4702	7291	0	0	1930	3750	952	2555	32	0	0	0	
clk_and_rst_wrappe...	274	40	0	0	192	273	1	15	0	0	0	2	
swerv_wrapper_in...	29636	13226	204	28	8759	29636	0	7030	22	4	0	0	