EE272B Design Verification: Current Mode Buck Converter

(The Open PMIC Project)

Git commit:
https://github.com/westonb/open-pmic/tree/d76df9e774dbea55497aa11a23e2d0d3f026fd26

Design Methodology

The current mode buck converter is a non-linear analog system consisting of two feedback loops, a feedback loop for current sensing that is internal to the converter, and the voltage feedback loop that controls the output voltage that is compensated off-chip.

In an effort to reduce design complexity we focus on maximal design re-use and have relatively loose specifications for the individual modules. Beyond characterizing individual modules for their rough suitability we focus our verification efforts on system level, where issues between the interaction between individual modules are more readily apparent. We have written a script to simulate our full converter across the full range of PVT and load corner cases.

Testbench Instructions

Each analog component that has been characterised has a testbench that can be open and run in xschem in its design folder that ends in "_tb". These testbenches will run ngspice and automatically plot and print the relevant data.

The system level testbench can be run in xschem. Once xschem has generated the testbench the automatic test script in the verification folder can be run.

For xschem to correctly generate netlists the base folder must be added to the user's xschemrc file and the SKYWATER_STDCELLS variable in the users xschem file must be set to point to the sky130_fd_sc_hvl library.

List of Blocks:

1. **bias-circuit**
   The bias circuit generates the cascode bias voltages for the opamps. Verification if it occurs through testing the opamps.

2. **comparator**

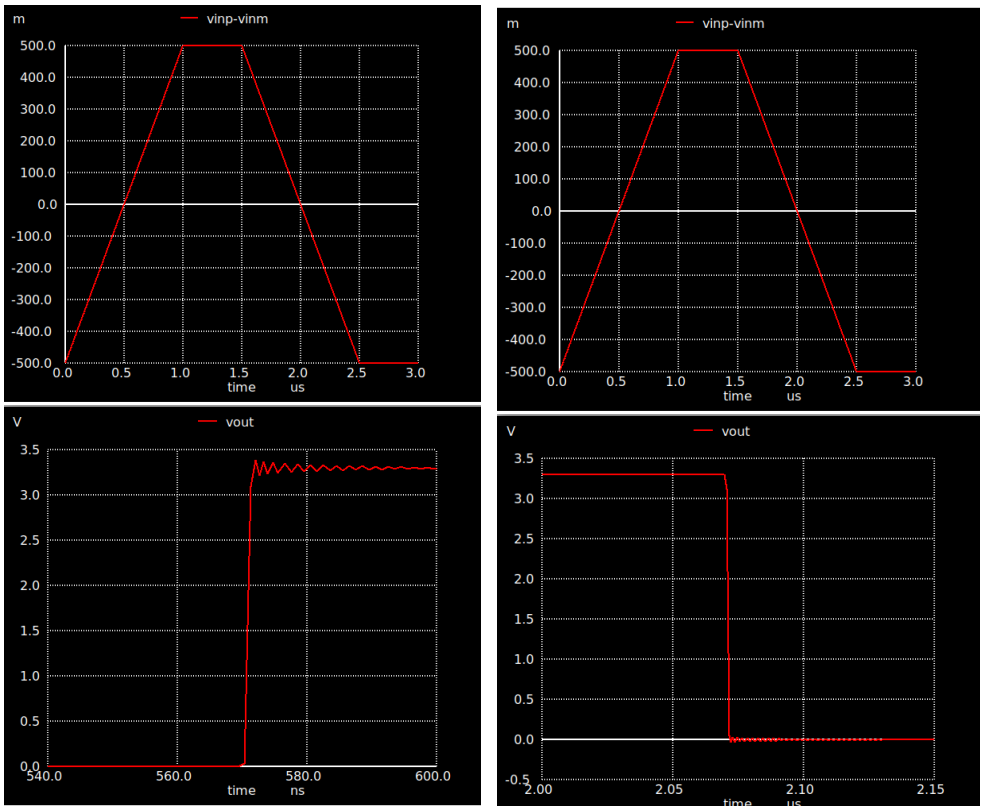
Test:
Static and dynamic characterisation

Running the test:
Used the testbench "open-pmic/design/comparator/comparator_w_obuff _tb.sch", while using an appropriate voltage source from the file "open_pmic/design/comparator/ voltage_source.sch".

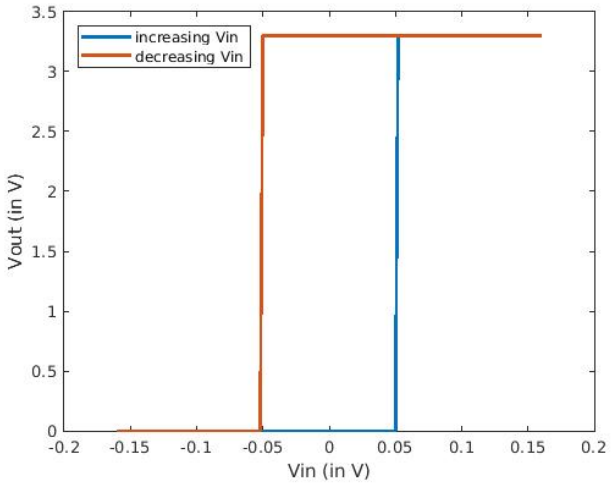
For dynamic characterisation, plotted vinp-vinm and vout signals in xschem.

For static characterisation, plotted vout vs. vinp-vinm graph using the script "open-pmic/design/comparator/static_characteristics.m". To enter values into the script vinp-vinm and vout were plotted in xschem first.

Plots:
Dynamic characterisation: To verify the comparator responds fast enough to the inputs. Two inputs to the comparator are error amplifier output and ramp from slope compensation circuit.



Static characterisation: To verify comparator had sufficient hysteresis to avoid noise in power mosfet switch control signal.



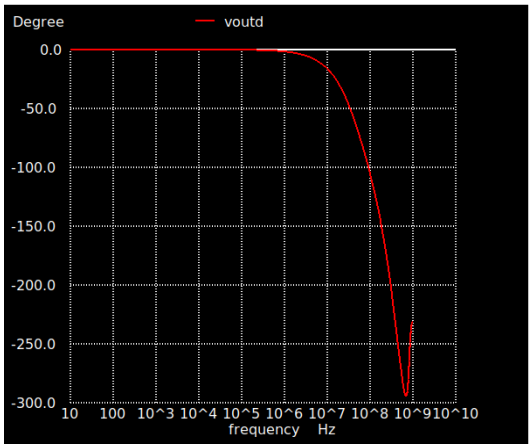
Specs verified:
For an input that changed at the rate of 1V/us, the comparator rise time was 3ns
The comparator had a hysteresis of approxixmately 50mV

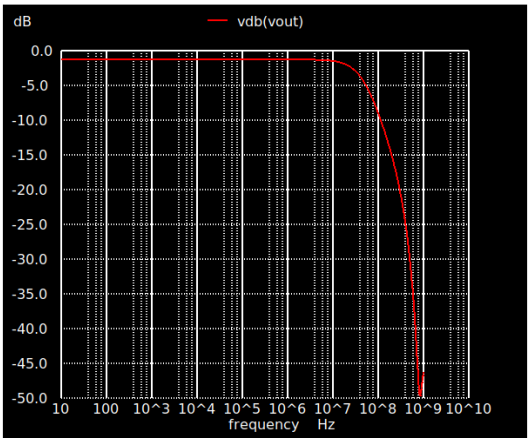
3. **current-sense**
   With two different analog test benches the open loop frequency response of the current sense amplifier was measured to calculated phase margin and the closed loop response after the additional current mirrors was measured to verify the system bandwidth.

   The transconductance of the pmos used to control the current through the sense fet increases with current, so the worst case stability would be at the maximum sensed current. Here we used a sensed value of 1A through the main power switch, which should exceed the maximum switch current in the actual converter.

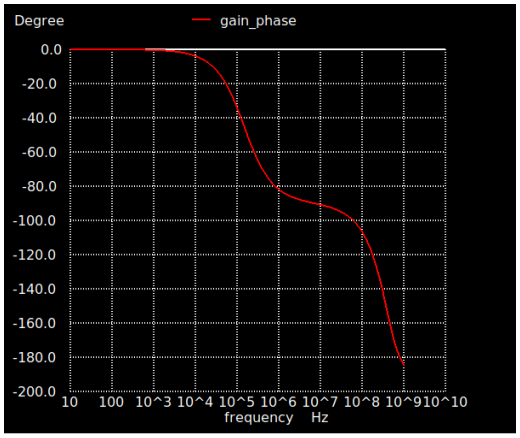
   Below are plots of the open loop response and closed loop response. From these plots it can be seen that thre is a phase margin of 65 degrees and the -3db bandwidth of the current sensing circuit is 24 MHz, which is a sufficient margin compared to the switching frequency of 500 KHz. The Vsense/Isw transfer ratio can not be directly measured from the small-signal plots as it is a large signal measurement. However, we can calculate the value from the DC operating point analysis in the testbench.

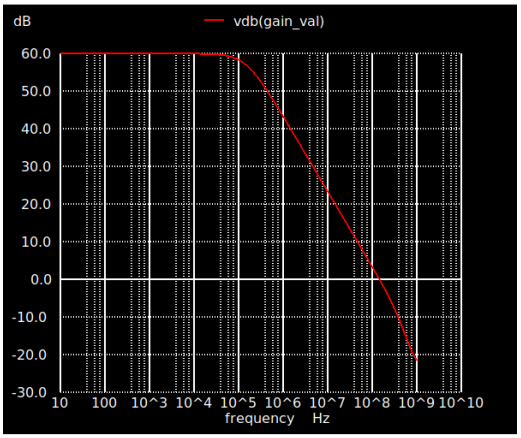
   Closed Loop:





Open Loop:



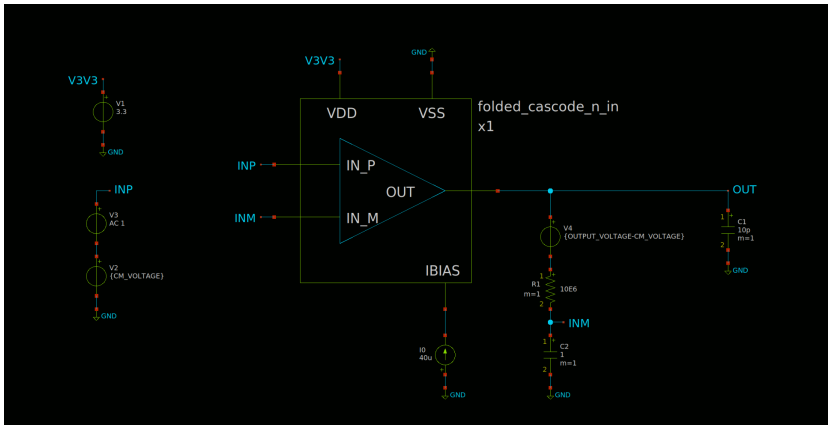


Transfer ratio	**1.1 V/A**
-3dB frequency	**24 MHz**
Phase Margin	**65 deg**

4. **folded-cascode-n-in**
   The folded cascode with nmos inputs is an output transconductance amplifier. We created a testbench which allows the DC values for the input common mode voltage and output voltage to be set and then the small signal open loop gain to be measured. The amplifier is externally compensated with dominant pole compensation in its application circuit so phase margin measurements are not directly applicable. However, the location of the second pole, which determines maximum bandwidth when the amplifier is compensated, can be measured. An

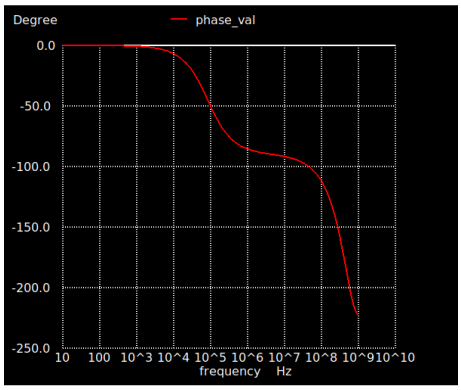
output loading capacitor allows for transconductance of the amplifier to be calculated from the 0 dB frequency with the relation 2*pi*Fc = Gm/Cl.

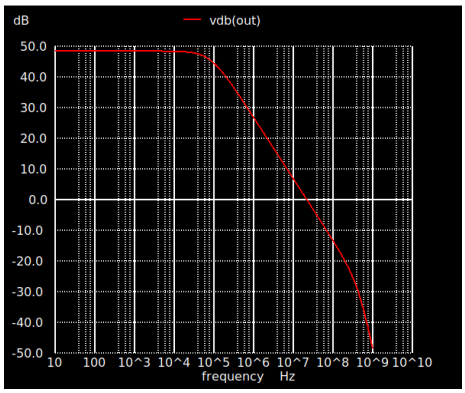
Our testbench, design/folded-cascode-n-in/folded_cascode_n_in_tb.sch, uses spice commands to calculate the crossover frequency, phase margin, and offset voltage at the operating point.



Based on the use of this opamp the common mode input voltage is the DC supply (3.3V) while the output voltage is the DC supply - Vth(p) (3.3-0.8V)

Below are plots of the phase and gain of the amplifier at 25C and the tt process corner and a table summarizing the performance of the amplifier at the this operating point:





DC Gain	**48.5 dB**
Gm	**1.35 mmho**
Offset Voltage	**1.7mV**
Second Pole Frequency	**245 MHz**

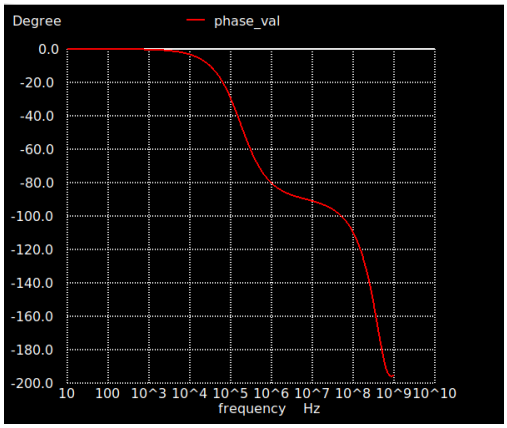
5. **Folded-cascode-p-in**

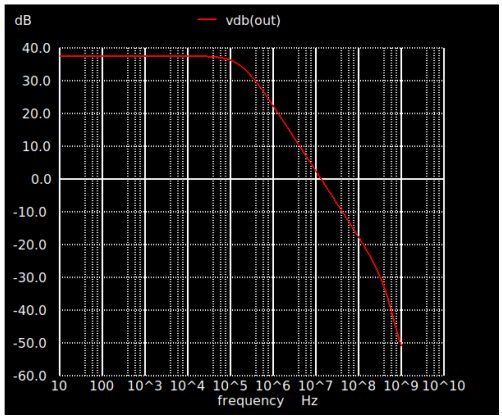
   The folded cascode-p-in is a mirror of the folded cascode-n-in amplifier. The test bench is the same and we use the same methodology to verify it.

   The expected common mode input voltage of this amplifier is the error amplifier voltage of 1.25V while the output voltage varies with the compensation voltage, which is a function of the desired output current of the buck converter.

   Our converter adds an offset voltage of 0.5V to the current sensing voltage, so the minimum DC output voltage is 0.5V. Performance of the amplifier is higher at a more typical DC output voltage.

   Below we have a table and plots showing the typical performance of the amplifier at 25C and the tt process corner:





DC Gain	**37 dB**
Gm	**0.8 mmho**
Offset Voltage	**-3.8 mV**
Second Pole Frequency	**280 MHz**

6. **Modulator**

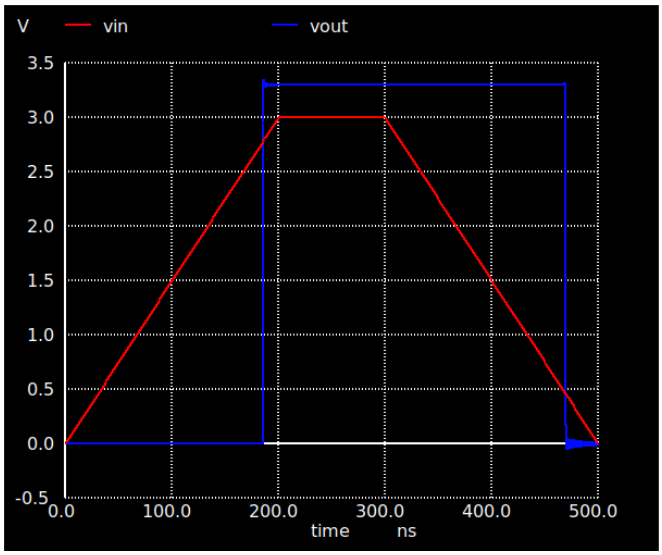
This module is tested in the context of our system level tests. It contains the comparator (verified separately), along with slope compensation circuitry and over current detector.

7. Oscillator

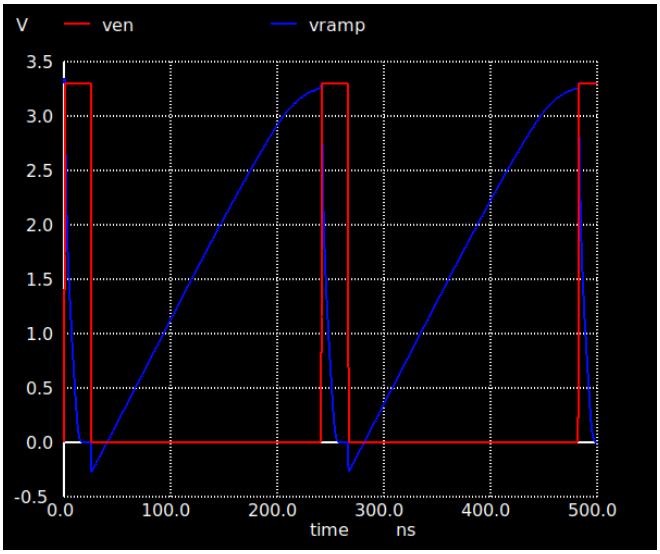
Test:
Test of individual blocks - ramp generator and Schmitt trigger. Overall test of the oscillator, to verify its target frequency.

Running the test:
Used the testbenches rampgen_tb.sch, scmittbuf_tb.sch, and oscillator_tb.sch located in the directory "open-pmic/design/oscillator".

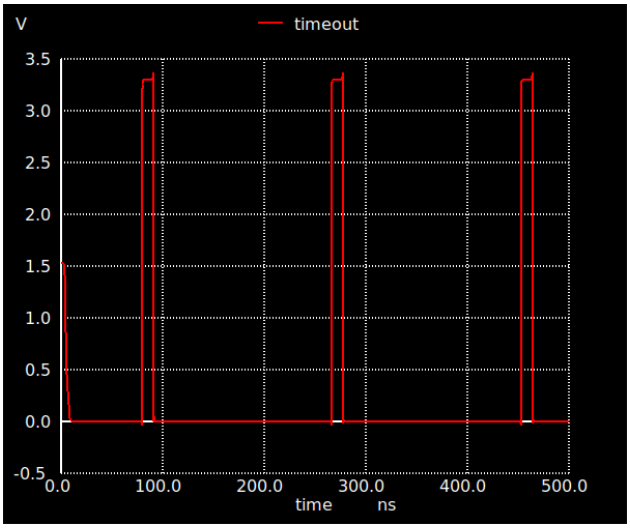
Plots:
The Schmitt trigger was designed to have a higher low-to-high transition voltage and a lower high-to-low transition voltage, so that the timeout signal has low duty cycle, given that the ramp output of rampgen has a much faster ramp down than ramp up. The following plot verifies this required characteristic of the Schmitt trigger:



The following plot verifies that the rampgen circuit's ramp output rises slowly and falls fast. The enable signal (ven) is a fixed signal of approximately 10% duty cycle and 4MHz frequency that is provided in the testbench.



Finally, the overall oscillator built with the ramp generator and Schmitt trigger in feedback has the following output waveform:



Specs verified:
We achieved our target frequency of 5MHz for the oscillator output. Though we will need to add extra digital circuitry to divide and bring down the frequency.

8. Power-stage

We created a test bench to check the on-resistance of different transistor sizes across different corner cases, which, along with the area utilization, aided in determining transistor sizing.

The functionality of the power stage is checked through our system level tests, where waveforms are checked to make sure that the PMOS and NMOS conduction period does not overlap.

9. **Switch-control**

The switch control block is a handpicked array of gates that implements the control signal muxing, deadtime generation, and stores the switching state. Pending conversion of this design to verilog for place and route, there is no formal specification. The main requirement is that the deadtime be much larger than our switching transitions to ensure that there is no simultaneous conduction of the power PMOS and NMOS.

This module is tested in the context of our system level tests.

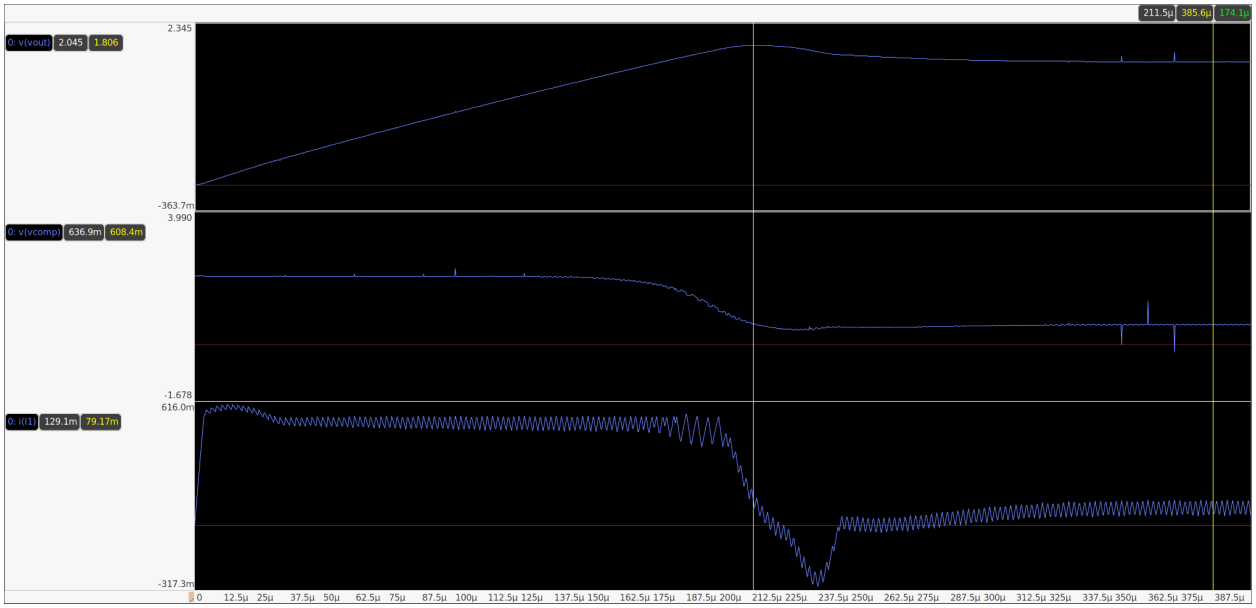
10. **system (top level)**

A large portion of the verification has occurred at the top system level due to the challenges posed by modeling the interaction between all of the sub-components across corner cases.

Our testbench (full_system_tb.sch) models the DC/DC converter as it would be integrated into the caravel test harness. It has a set of digital inputs which will be driven by the chip I/O, analog inputs which will be driven by the analog input capability of the standard caravel I/O, and the switching node pin, which will be connected to a set of bare I/O pins.

The full system testbench uses a simplified model of the carval analog I/O parasitics and models the common ground inductance and resistance as well as the inductance on the power rails. This allows for verification that the control circuitry of the buck converter will not be impacted by induced noise during switching transitions.

The testbench can be manually run through xschem and has the load resistance (which controls output power) and input voltage as parameterized values. Below is an example waveform showing the startup of the converter. A single simulation takes around 10 minutes. Top is the output voltage, middle is the compensator (control) voltage, and bottom is the inductor current. There is a slight overshoot on startup due to wind-up of the compensator voltage while the switch current is limited.



We have written a script, located in the verification folder, which takes the initial spice netlist for the spice netlist, varies the parameters for process corner, temperature, supply voltage, and output load, and then runs the simulation. Due to disk-space limitations the waveforms from each run are not saved but values needed to ascertain correct functionality of the converter are extracted: the minimum and maximum inductor current, the efficiency, the maximum transient startup voltage, and the minimum and maximum output voltage once the startup transient has finished.

The transient and steady state output voltage values allow for verification that the converter is operating correctly and has a stable output voltage, while the efficiency is an important performance value and is another check on the correct operation of the converter. Together, these values are what define the performance of any switching converter.
We expect to use this script to continually verify our converter once we start adding extracted netlist for individual converter components. So far we have run 24 simulations, checking the SS/FF, 25C/70C, 3.3V+/-10% corner cases, at full load (300mW) and no load. In all cases the output voltage remains stable within +-1% of the nominal value and the efficiency is high for all loaded operating points. There is a minor transient spike on start-up and a somewhat large negative inductor current during start-up for the no-load cases. This is due to compensator wind-up and could be reduced with a larger output capacitance, but would significantly increase the time required to run the simulations.

Vin	Rload	Temp	Process Corner	Iin	Iout	Ibias	Vmax	Vmin	Vpeak	IL_Max	Il_Min	Eff
3.3	10	25	ss	0.103	0.180	0.002	1.804	1.804	2.028	0.772	-0.140	0.936
3.3	10	25	ff	0.103	0.180	0.002	1.804	1.803	1.951	0.844	-0.078	0.941
3.3	10	70	ss	0.104	0.180	0.002	1.805	1.804	2.023	0.703	-0.062	0.933
3.3	10	70	ff	0.103	0.180	0.002	1.805	1.804	1.943	0.872	-0.105	0.939

3.3	1000	25	ss	0.001	0.002	0.002	1.806	1.806	2.098	0.764	-0.987	0.312
3.3	1000	25	ff	0.001	0.002	0.002	1.805	1.805	1.999	0.811	-0.665	0.314
3.3	1000	70	ss	0.001	0.002	0.002	1.808	1.807	2.090	0.806	-0.796	0.311
3.3	1000	70	ff	0.001	0.002	0.002	1.807	1.806	1.989	0.771	-0.517	0.312
3.6	10	25	ss	0.095	0.180	0.002	1.805	1.804	2.020	0.839	-0.098	0.936
3.6	10	25	ff	0.094	0.180	0.002	1.804	1.804	1.951	0.858	-0.118	0.940
3.6	10	70	ss	0.095	0.180	0.002	1.805	1.805	2.018	0.741	-0.071	0.933
3.6	10	70	ff	0.094	0.180	0.002	1.805	1.804	1.940	0.838	-0.088	0.938
3.6	1000	25	ss	0.001	0.002	0.002	1.806	1.806	2.086	0.761	-0.888	0.291
3.6	1000	25	ff	0.001	0.002	0.002	1.806	1.805	1.994	0.885	-0.639	0.288
3.6	1000	70	ss	0.001	0.002	0.002	1.808	1.808	2.081	0.714	-0.784	0.289
3.6	1000	70	ff	0.001	0.002	0.002	1.807	1.807	1.986	0.829	-0.566	0.289
2.97	10	25	ss	0.115	0.180	0.002	1.804	1.803	2.046	0.759	-0.140	0.936
2.97	10	25	ff	0.114	0.180	0.002	1.804	1.803	1.959	0.830	-0.095	0.942
2.97	10	70	ss	0.116	0.180	0.002	1.804	1.804	2.039	0.730	-0.070	0.931
2.97	10	70	ff	0.115	0.180	0.002	1.804	1.804	1.949	0.809	-0.061	0.939
2.97	1000	25	ss	0.001	0.002	0.002	1.806	1.806	2.128	0.758	-1.030	0.350
2.97	1000	25	ff	0.001	0.002	0.002	1.805	1.805	2.009	0.817	-0.632	0.349
2.97	1000	70	ss	0.001	0.002	0.002	1.808	1.807	2.115	0.718	-0.869	0.339
2.97	1000	70	ff	0.001	0.002	0.002	1.806	1.806	1.997	0.826	-0.524	0.342

Design Metrics

The performance of a DC/DC converter is specified by its efficiency and maximum output power. The initial specifications for our converter are typical of something that would be used for a low to medium power embedded system.

Initial Goals:

Input Voltage	3.3V
Output Voltage	1.8V
Maximum Output Current	>300mA (0.5W)
Efficiency	>85%

Simulated Performance:

Output Voltage	1.8V +/-1%
Maximum Output Current	>330mA (0.6W)
Efficiency	>90%

Below is a plot of simulated efficiency for the SS process corner at 70C, 3.3V in, 1.8V out. The ss process corner and 70C temperature should provide a relatively pessimistic measure of the power loss of the system as this process corner maximizes the on resistance. Even with these assumptions the efficiency is significantly above our initial 85% target for the most load points