Contact Mask Design Principles

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Tutorial Outline

- Simple strategies for getting your masks right the first time, avoiding process headaches, and design for SNF-specific tools.
  - Understanding contact aligners and tool-specific issues
  - How process impacts mask design
  - Alignment marks and strategies
  - Mask layout tips and tricks
  - Design rules: the basics
  - Avoiding data file disasters

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SNF Exposure Tools

Name	Ultratech 1000	Karl Suss	EV 620	Nikon NSR
Type	1:1 Stepper	Contact	Contact/Prox	5:1 Stepper
Mask Size	3X5"	4" and 5"	5"	5"
Wafer Size	4" *	pieces-4"**	4"	4"
Maximum Exposure Area	sq. = 10 x 10 mm. rect = 21 x 7.2 mm	5" mask = 4" 4" mask = 3"	4" diameter	4"array
Obj. Separation	10- 21mm***	50-100mm		65mm
~ mininum resolution	1.25um lens rated****	1um	1um	.6um
Additional Features	Site-by-site stepper	Backside align	Anodic Bond,backside align	5:1 reduct.

Exposure Information

•6 inch manual loader is also available.
** 4 inch diameter is the maximum
*** Aperture separation
**** Down to 0.8um can be achieved in isolated circumstances.

EV620 Objective range

•Top side objective travel range: **x direction 30 - 150mm separation** (8 - 150mm optional); **y direction +-75mm**; z direction +-5mm
•Bottom side objective travel range: **x direction 30 - 100mm separation** (8-100mm optional); **y direction +-12mm**, z direction +-5mm

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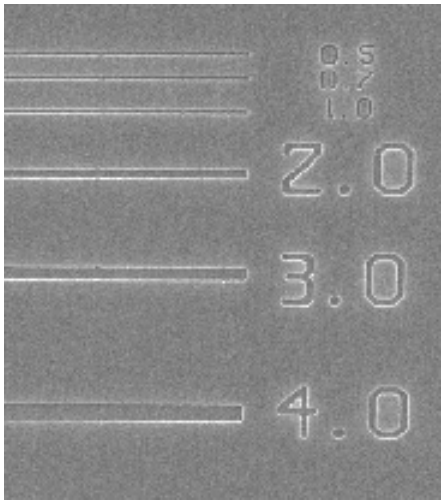
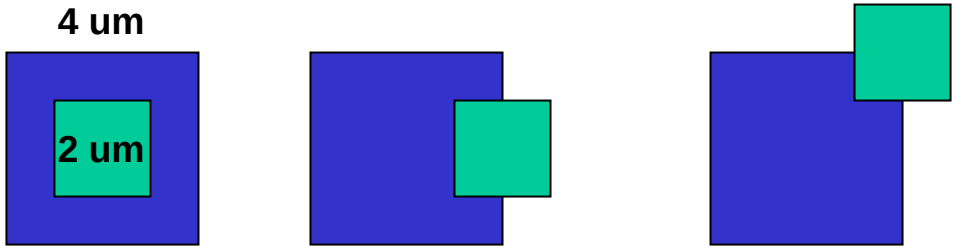
Contact aligners and tool-specific issues

- Max linewidth resolution
  - Don't design linewidths narrower than aligner capability!
- Max x-y tolerances
  - Best case layer-to-layer alignment tolerance (20X objectives, vacuum contact, skill)
    - ~ 0.6 um for top side
    - ~ 1 um front-to-back
  - Your designs should accommodate expected alignment error – based on your skill level and process (2 um is a safe number)



Karl Suss MA-6 resolution



x + 2 um misalignment

x + 2 um, y + 2 um misalignment

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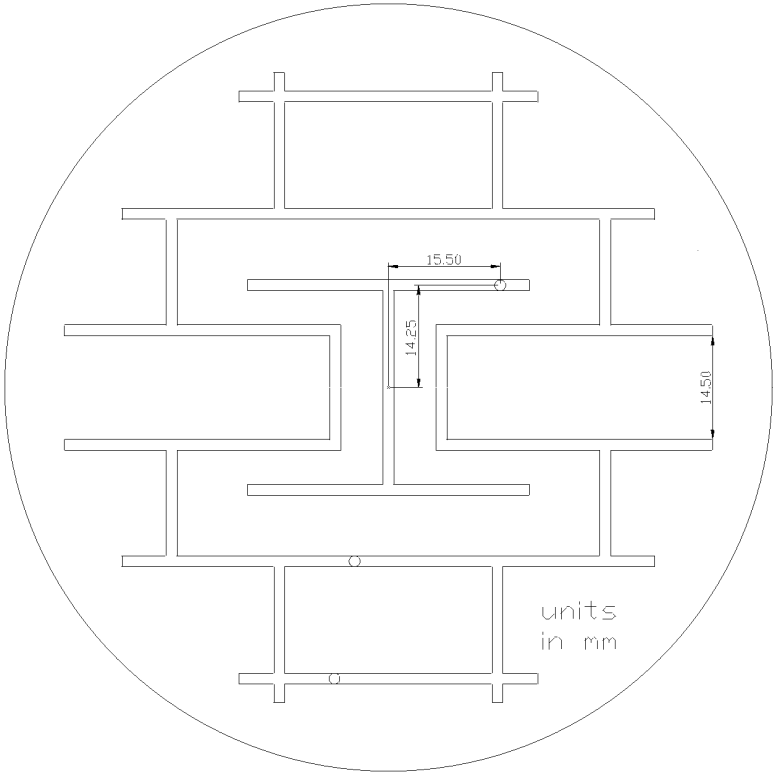
Contact aligners and tool-specific issues

- Location of objectives
  - Range of motion is limited, so alignment marks must be in specific locations on mask

EV620 Objective range

- Top side objective travel range: **x direction 30 - 150mm separation** (8 - 150mm optional); **y direction +-75mm**; z direction +-5mm
- Bottom side objective travel range: **x direction 30 - 100mm separation** (8-100mm optional); **y direction +-12mm**, z direction +-5mm

- Objective field of view size
  - Determines how large to make alignment marks
- Unique tool features
  - Karl Suss vacuum lines, e.g.



Karl Suss Chuck Vacuum lines

drawing by Matt Hopcroft

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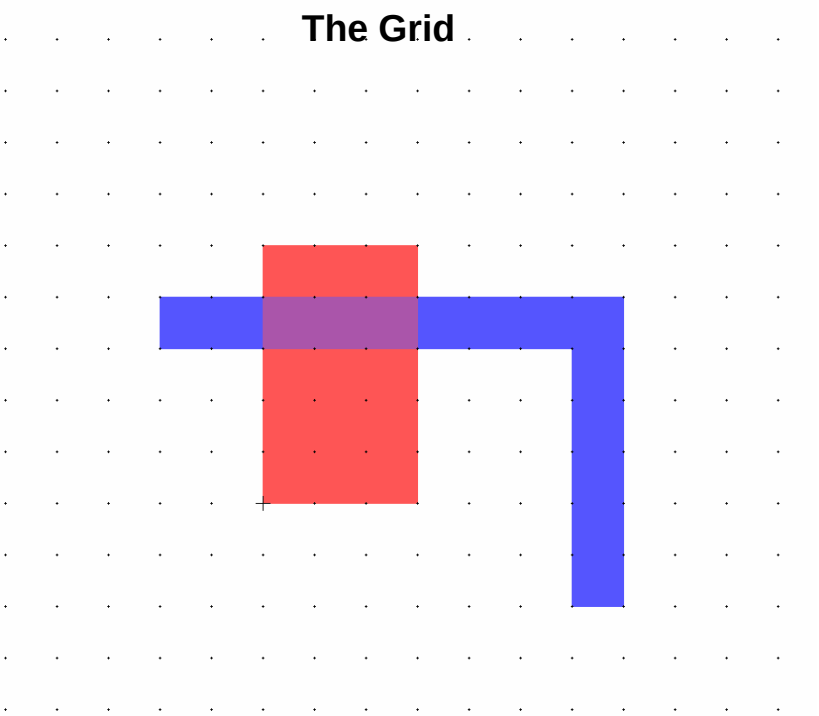
Mask writer features

- The fracturing grid: 0.5um for contact masks made at SNF
  - Mask writer takes in GDSII data, and ‘fractures’ or pixelates it
  - Fracturing grid determines ultimate resolution of the mask
  - Contract vendors can do 0.10 um, 0.25 um, but you pay dearly for resolution



- Maskwriter is designed to best handle ‘Manhattan geometry’
  - Squares, rectangles, 90 degree corners

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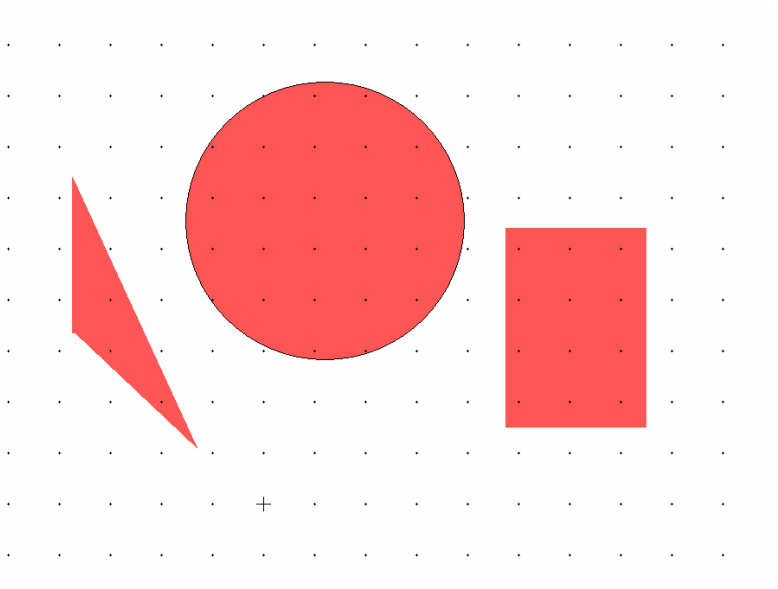
Mask writer features

- Polygons can be problematic
  - Circles, polygons, and slanted lines burden the conversion process because they are ‘off-grid’
  - Large numbers of polygons will dramatically increase conversion time
    - At SNF, you may exceed mask writer capability
    - At commercial vendor, this will increase your mask cost
- Avoid polygons unless you really need them



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How process affects mask design

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Know your process before you start your mask

- Design your mask to fit your process and vice versa
  - Alignment to crystal axis (piezoresistors, anisotropic Si etch)
  - Lithography
    - Edge bead removal
    - Critical dimensions
  - Wet etch
    - Undercut compensation
  - DRIE etch
    - Center to edge variations in etch rate
    - Undercut compensation

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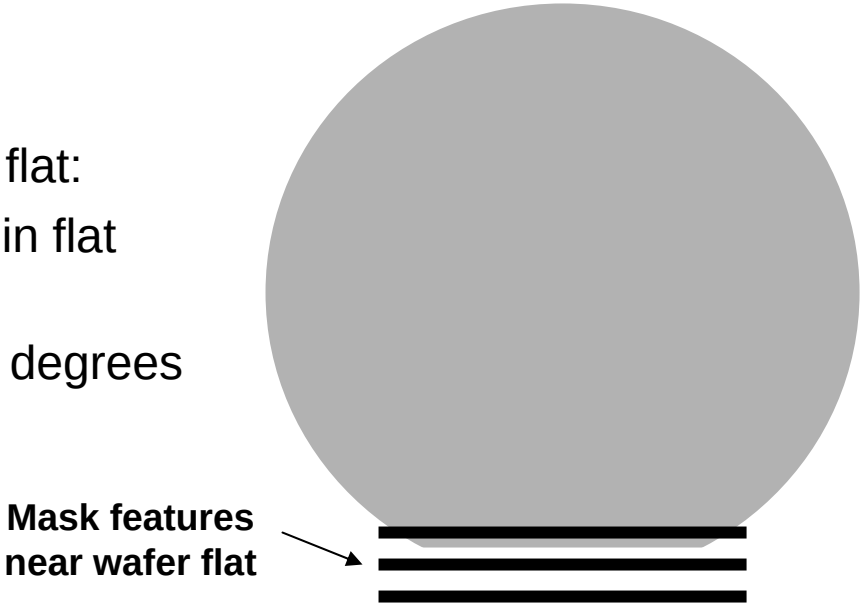
Alignment to crystal axis: crude alignment

- Some processes require alignment to crystal axis
  - Piezoresistors
  - TMAH/KOH etching
- For crude alignment to wafer flat:
  - Need alignment features in flat area of mask
  - Wafer flat is only within 2 degrees of true crystal axis



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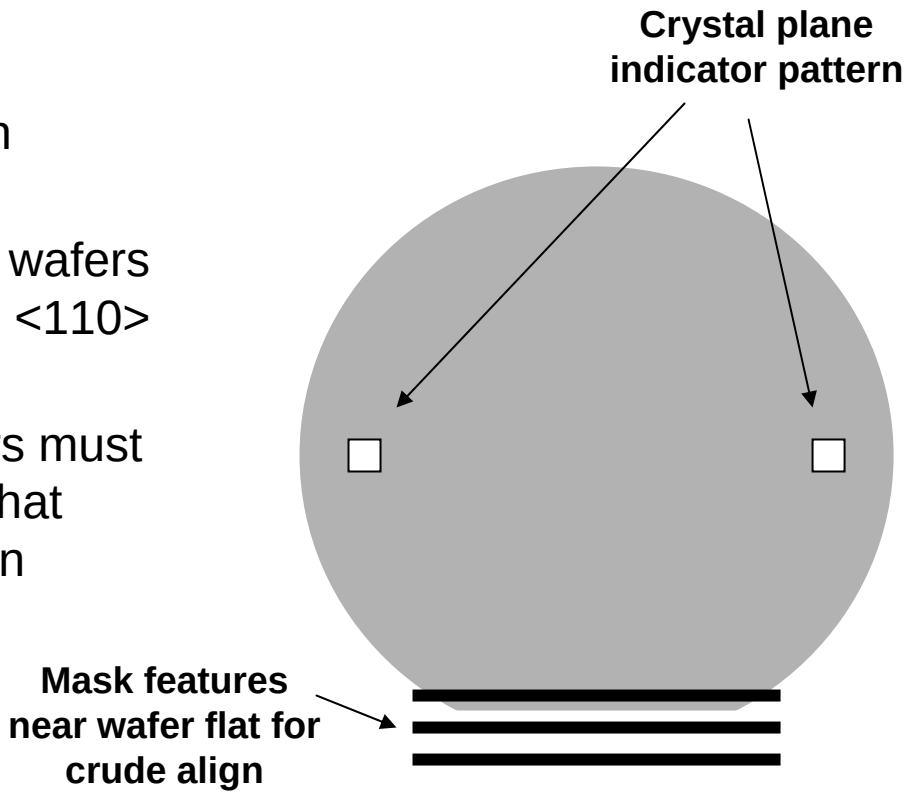
Alignment to crystal axis: precise alignment

- For precise alignment:
  - Need mask with an etch pattern
  - First process step: etch wafers in KOH/TMAH to reveal <110> direction
  - Subsequent mask layers must have alignment marks that register with etch pattern



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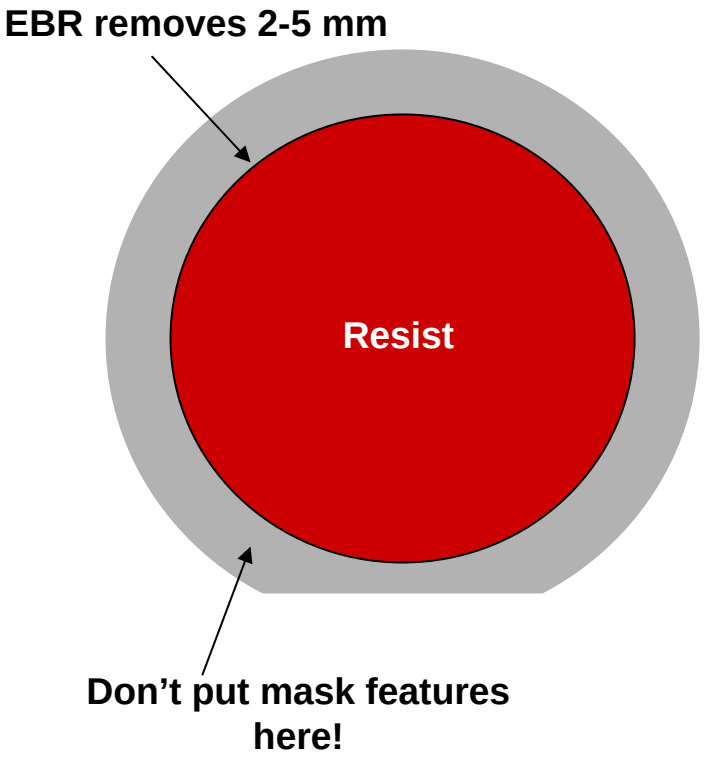
Lithography considerations

- Edge bead removal (EBR) will remove outer 2 – 5 mm edge of resist
  - Any mask features in this area will be lost
  - Don't put alignment marks in this zone
- Don't pattern to edges of wafers
  - Tool holders
  - Etch non-uniformity
  - Device yield usually poor



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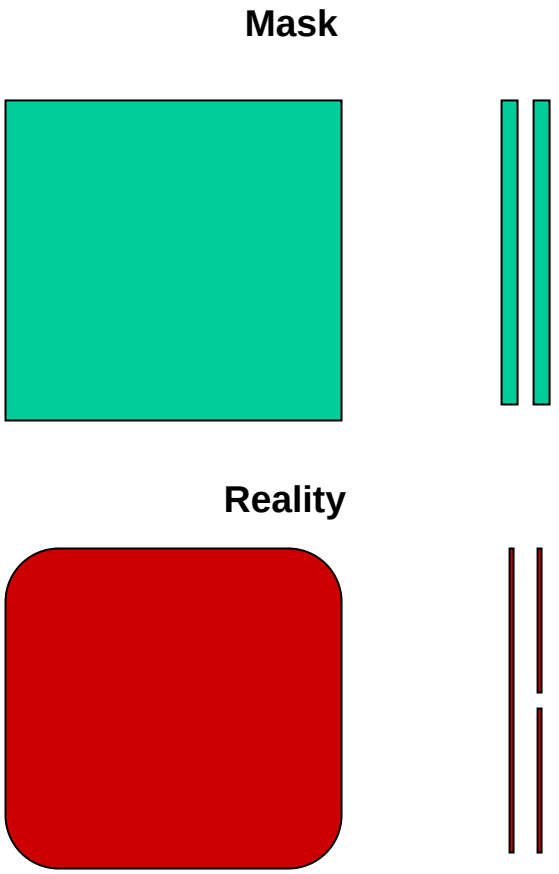
Lithography considerations

- Disparate feature sizes will drive you crazy during processing
- For a given expose and develop time, or etch process:
  - By the time large features are developed, small features may be over-developed
- Options:
  - Split your designs into two separate mask sets
  - Compensate smaller features



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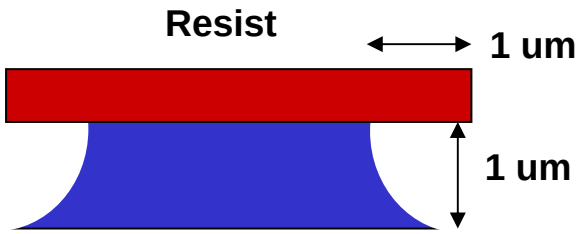
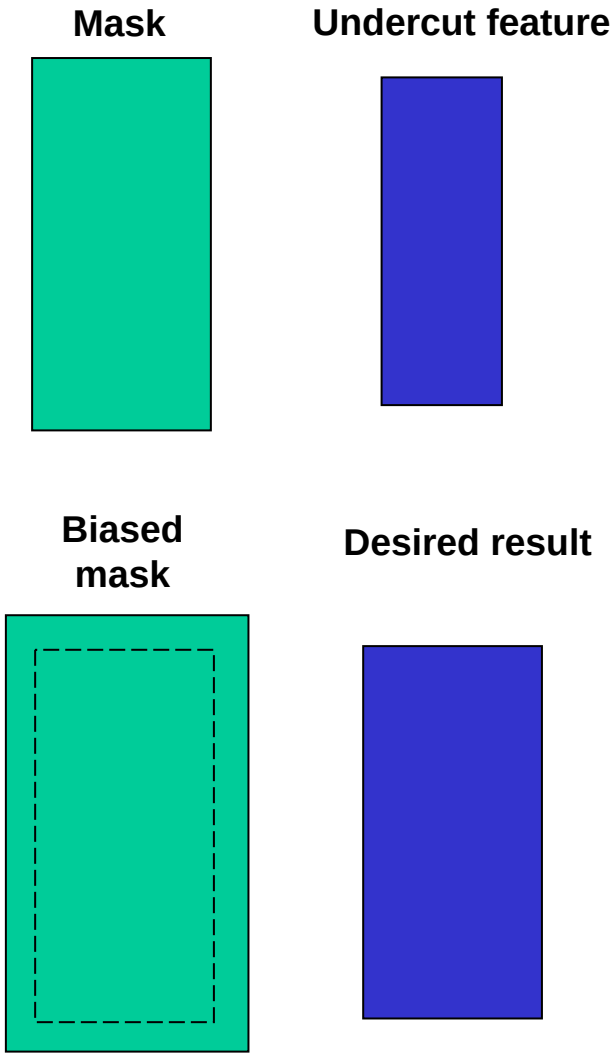
Wet etch considerations

- Undercut compensation needed for isotropic etch processes
  - Lateral loss is equal to etch depth
  - Compensate mask data to make sure you get what you want on the wafer
  - Some mask writers can automatically add “bias” – positive or negative



Lateral undercut = etch depth



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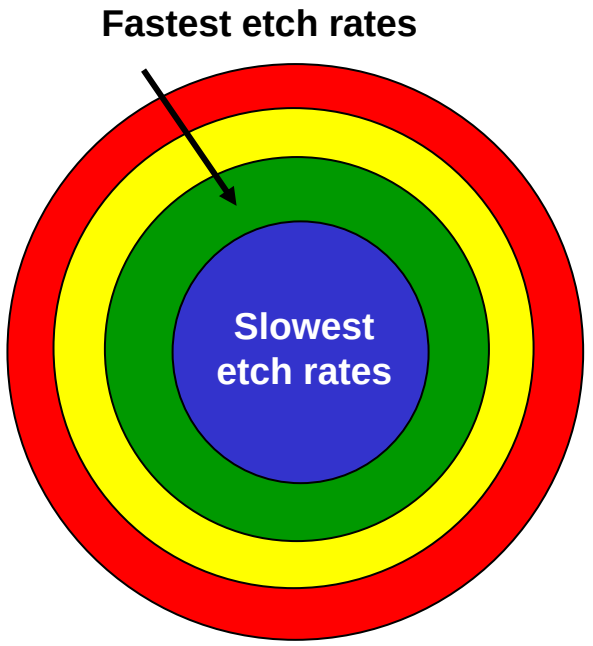
DRIE etch considerations

- Non-uniform etch rates
  - Wafer location
  - Feature size
  - Loading (open area/wafer area)
- Use it to your advantage!
  - Small features on wafer perimeter
  - Large features in wafer center



Wafer location affects etch rate

Pattern area affects etch rate

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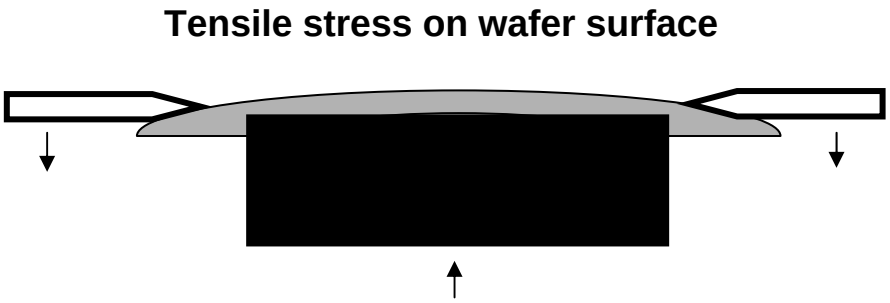
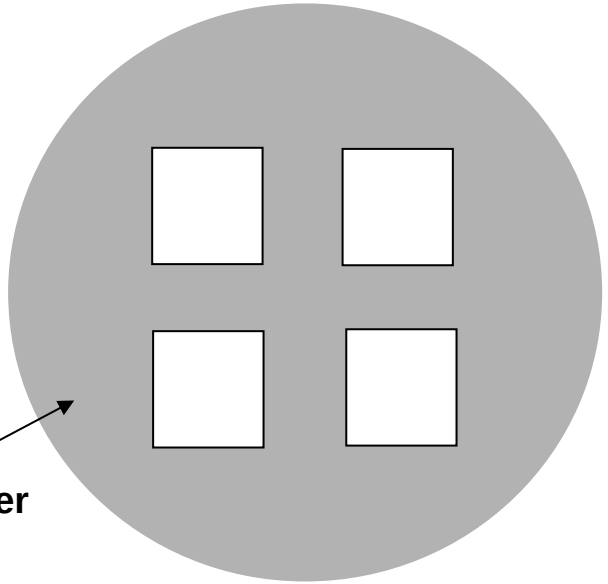
DRIE etch considerations

- STS chuck exerts mechanical pressure on wafer
  - Designs must maintain mechanical integrity during etch
  - Avoid:
    - Scribe lines
    - Free die
    - Etch patterns to edge of wafer
    - High load layouts





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Mask Layout

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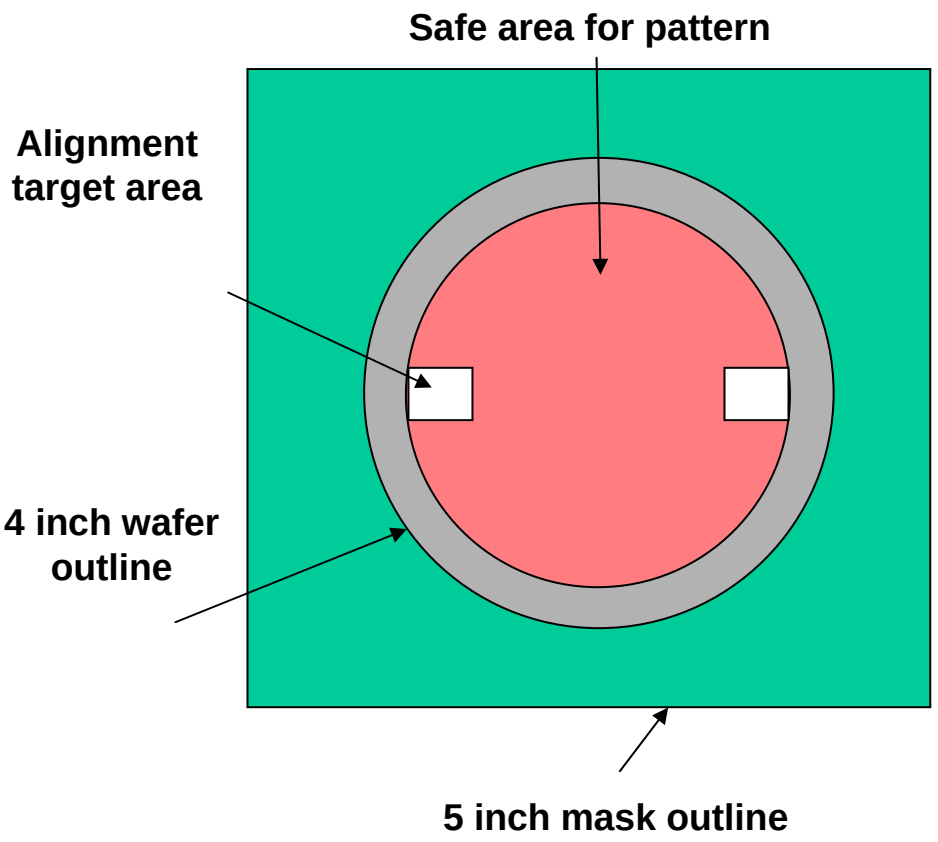
Mask layout: Before you start drawing

1. Outline your process
2. Prioritize your die list
3. Sketch global layout
   - Identify ‘no-pattern’ zones
   - Alignment mark areas
   - Test areas
4. Sketch die outlines, estimate die counts
5. Re-prioritize your die list
6. Then, start drawing your die patterns



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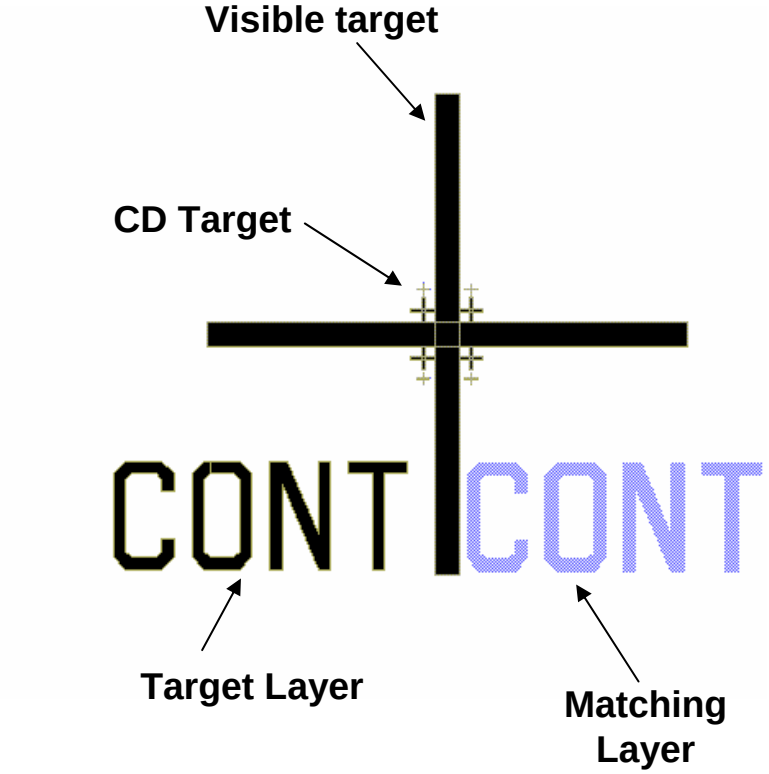
Alignment marks and strategies

- Alignment mark design
  - For contact aligners, whatever you like! (http://snf.stanford.edu/Process/Masks/ContactAlignMks.html)
  - Steppers have defined marks, see SNF website
- Sizing
  - Helpful to have one mark visible to naked eye
  - Smallest mark should be same size as Critical Dimension (CD)
- Labeling
  - Good idea for multiple layers
- Check your process: make sure a process step won't remove your marks!



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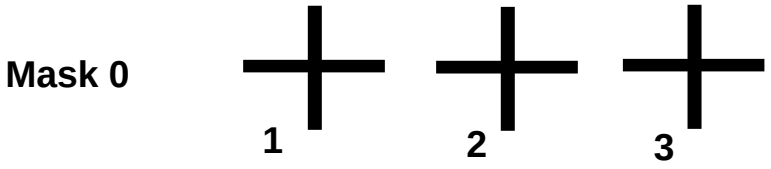
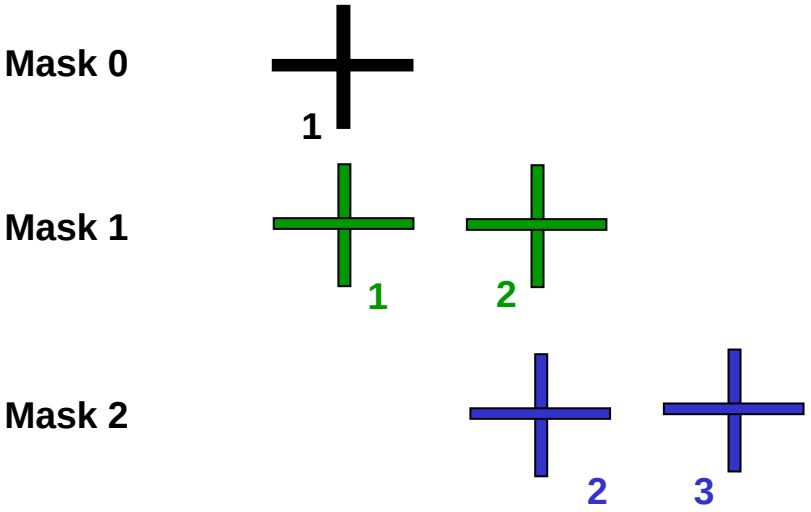
Alignment marks and strategies

- Layer to layer registration
  - All targets on one mask – convenient



  - If Layers 1 and 2 must be well-aligned, have Layer 1 provide the target for Layer 2



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Drawing software

- Tanner L-edit Pro
  - Available at SNF on CAD room comptuers – free to lab users
  - Student version available for download (limited features)
- AutoCAD
- Coventorware
- DW2000
- Any software that can produce DXF, CIF, or GDSII format

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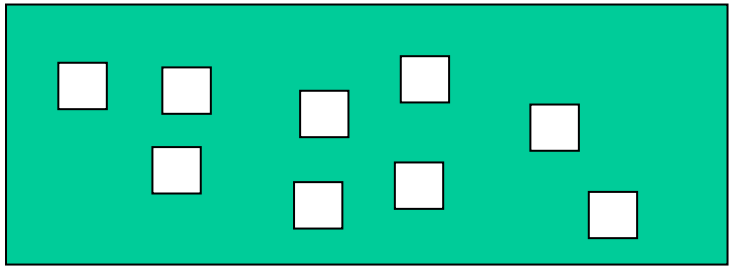
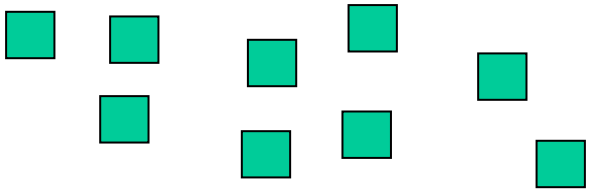
Drawing tips and tricks: Keeping your sanity

- The mask writer computer can easily manipulate your data:
  - Mirroring patterns (right vs. wrong reading)
  - Polarity change (clear vs. dark field)

Dark field with many cutouts



Easier to draw the inverse and let the mask writer flip the polarity



Don't bend your brain drawing mirror images

Draw this instead

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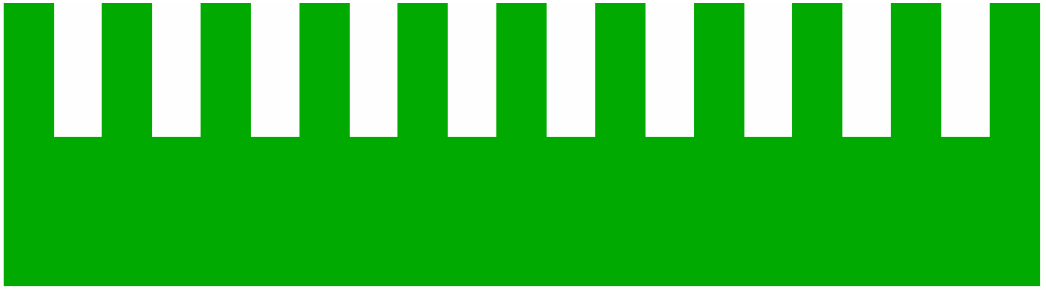
Drawing tips and tricks: Saving time

- (L-Edit) Instances and arrays: fast and accurate way to construct complicated patterns
  - Changes to cells propagate instantly up the hierarchy

Cell

Instance of cell arrayed into a row of 10



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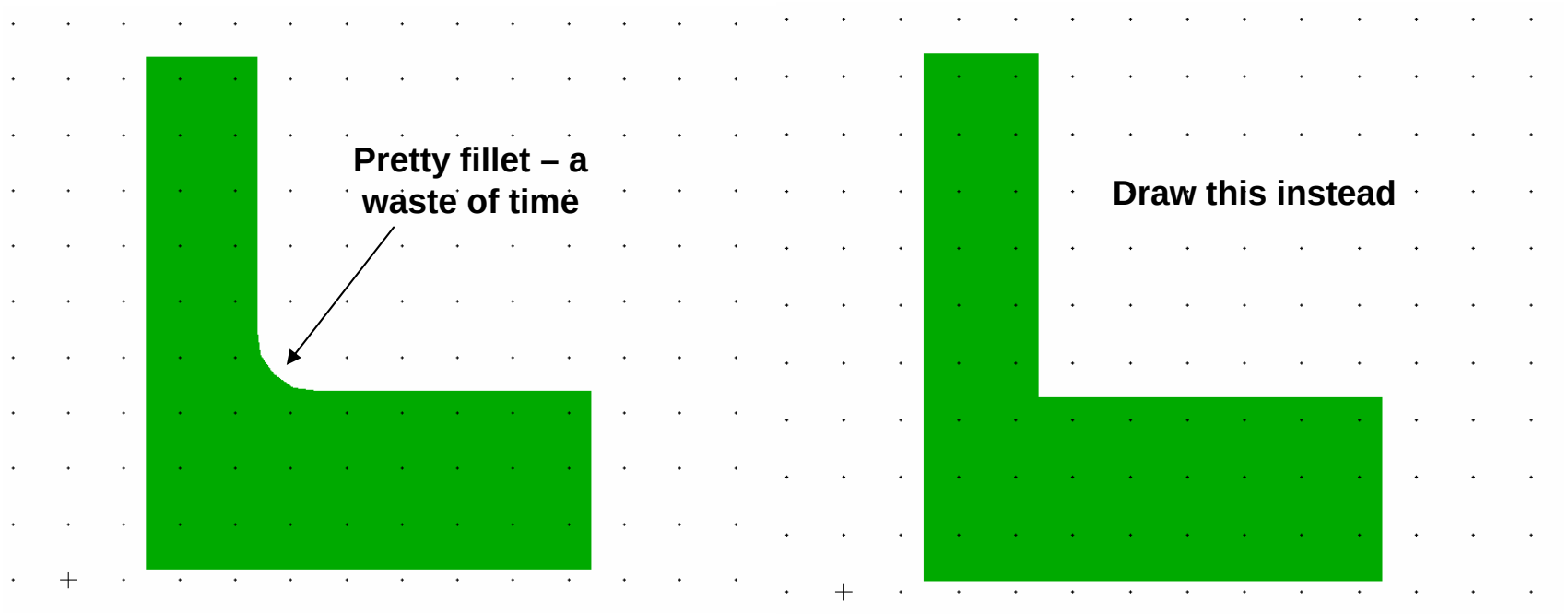
Drawing tips and tricks: Saving time

- Don’t waste time rounding corners or prettying rough edges unless they are > 10 um
  - Resist reflow will round sharp corners
  - Etch will smooth out patterns



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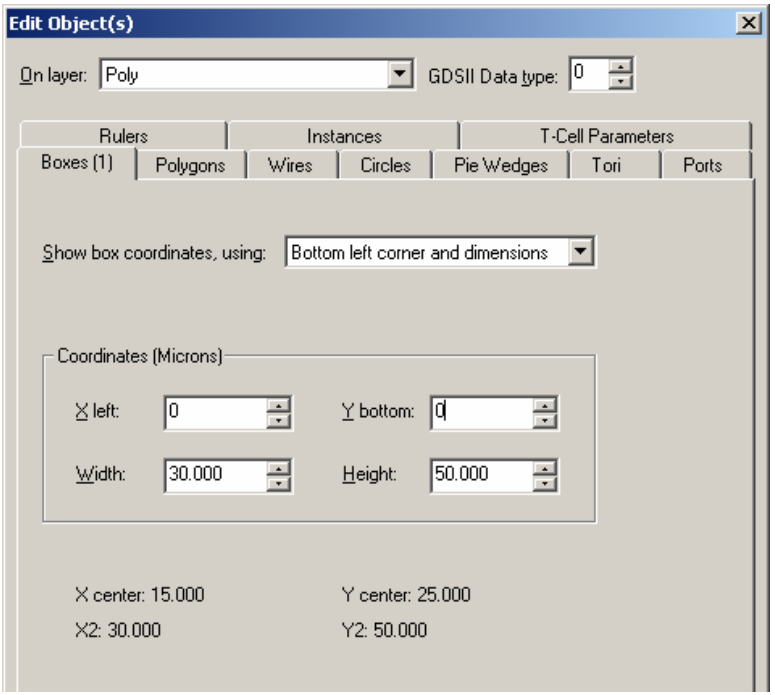
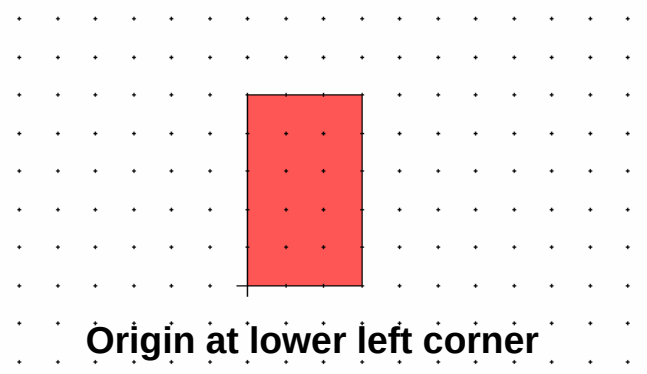
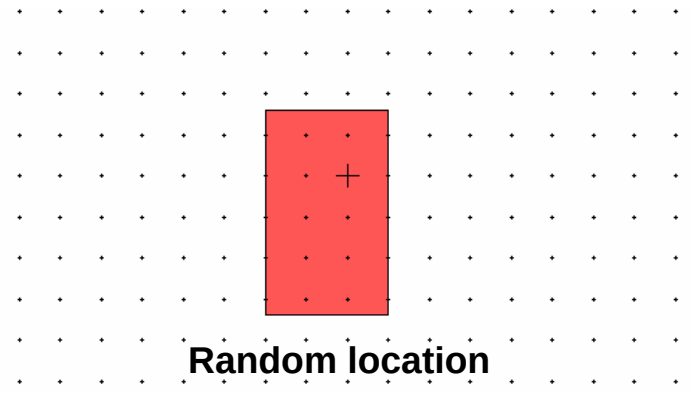
Drawing tips and tricks: Keeping your sanity

- Use round numbers: 5, 10, 50, etc.
  - Easy math for design by x,y coordinates



- Put the origin in a meaningful location





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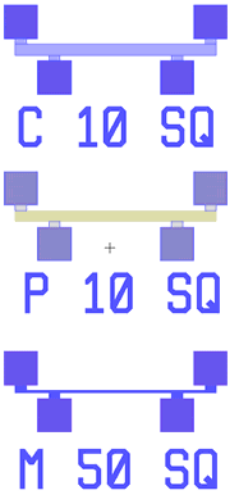
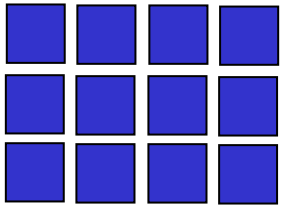
Drawing tips and tricks: Nice details

- Label your die so you know what you're looking at through the microscope
  - Metal layer is best for labels
- Consistent bond pad pitch

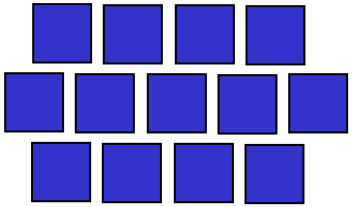


- Align die patterns for easier dicing and testing

5 saw cuts



10 saw cuts



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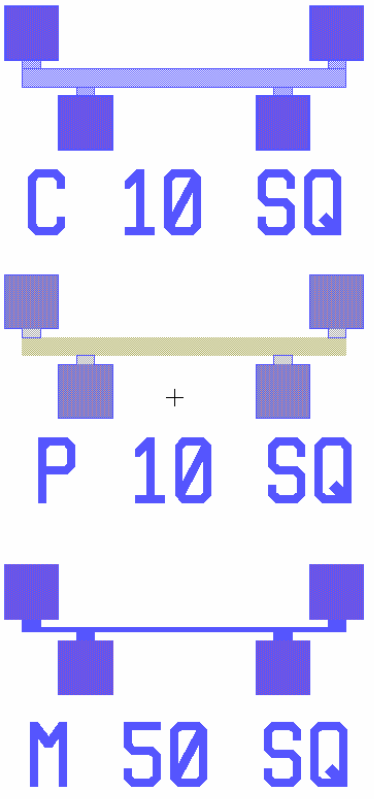
Wafer Test Areas

- Special devices and patterns solely used to debug your process and your device
  - Etch completion
  - Layer thickness
  - Layer resistivity
  - Capacitance
  - Etc.
- Tight for space? Put test areas in the dicing lanes



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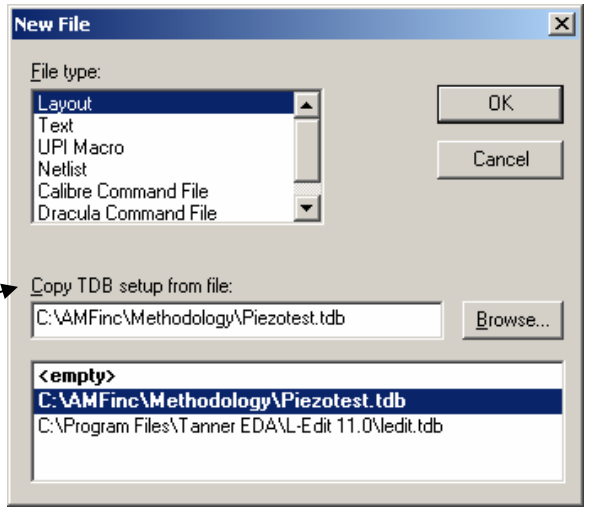
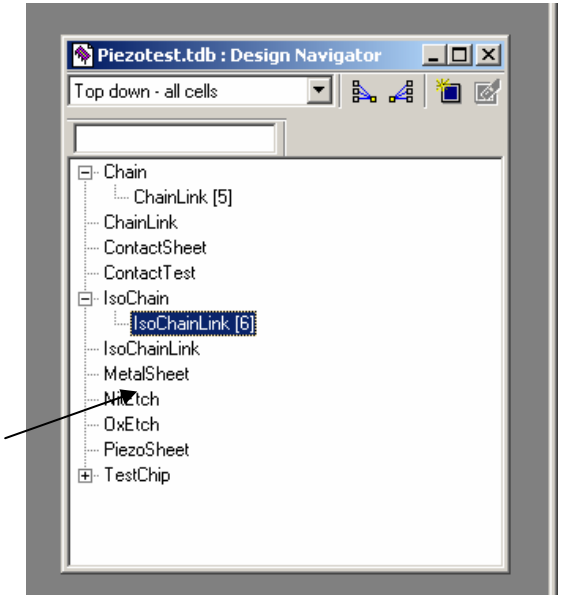
Drawing tips and tricks: Saving time

- Use layout templates
  - Beginners: borrow from your colleagues
  - Experts: create your own macros
  - L-edit: use setup files



- Develop your own design library
  - Use cells as much as possible
    - Easily copied to new design files
  - Use meaningful cell names



Any of these cells can be easily pasted to a new file

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Design Rules: the basics

- No linewidths or spacings < 2 um
- Stay on grid
- Avoid polygons as much as possible
- Dicing lanes = 100 um
- Bondpads min size: 200 um x 200 um
- Avoid feature size disparity

- Develop a design rule set that makes sense for your process and goals!
  - Parasitic capacitance
  - Positional tolerances
  - Undercut compensation
- Utilize automatic Design Rule Checks in CAD software

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Avoiding Common Data File Disasters*

*thanks to Paul Jerabek and Mahnaz Mansourpour for input

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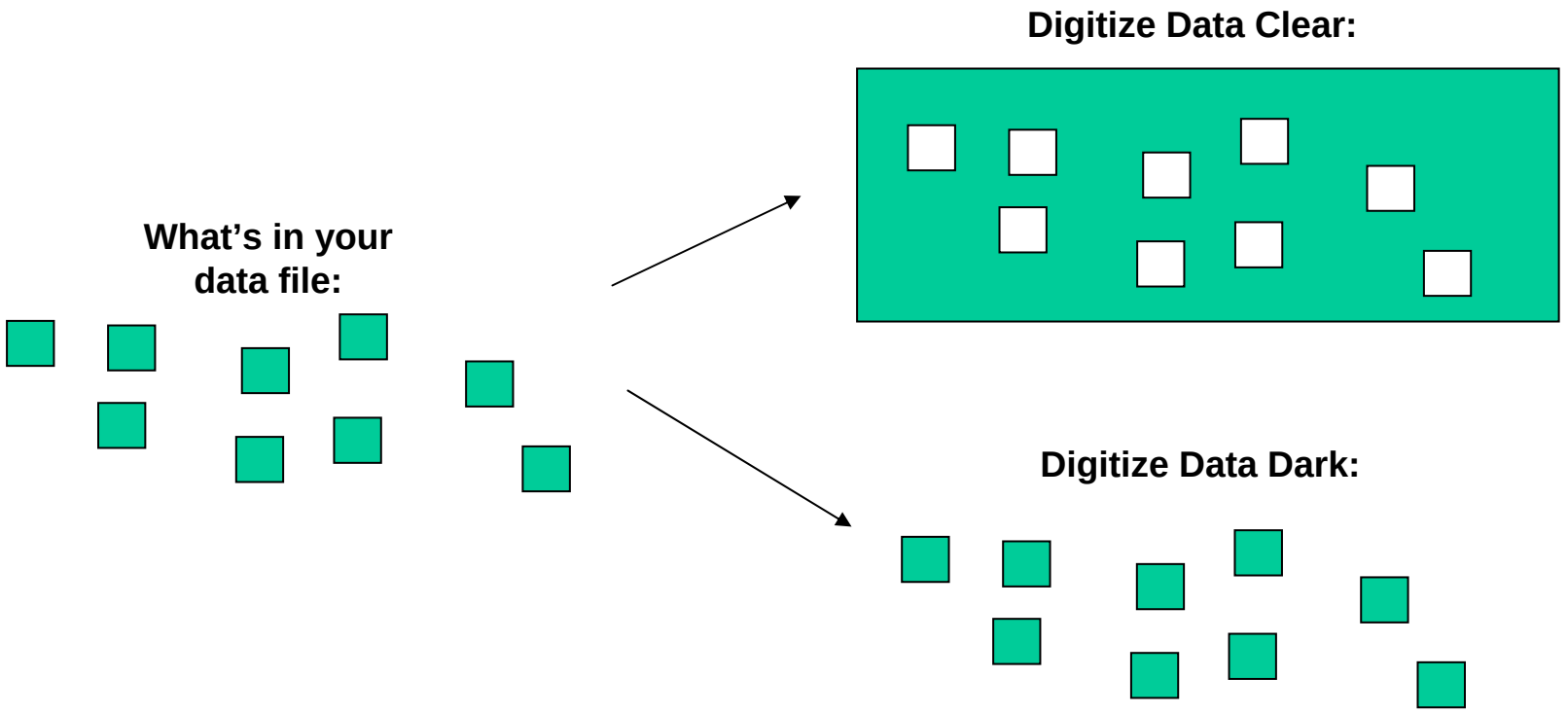
Disaster #1: “Ack! Wrong polarity!!”

Symptom: Your mask is perfect, but it should have been clear (dark) field

- Confusion about whether to digitize data “Clear” or “Dark”



- Still confused? Ask Paul Jerabek, your mask vendor, or an experienced user to look over your data and request form

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Disaster #2: “This isn’t what I wanted”

Symptom: Your mask file looks fine, but the mask is wrong

- Commonly caused by conversion and fracturing problems:
  - Stay on grid
  - AutoCAD users: close all shapes and lines – indeterminate features will cause serious problems
  - Make sure each layer has a unique GDSII number
  - Less sophisticated GDSII converters will eliminate confusing or conflicting data
    - You won’t always get a warning in the log

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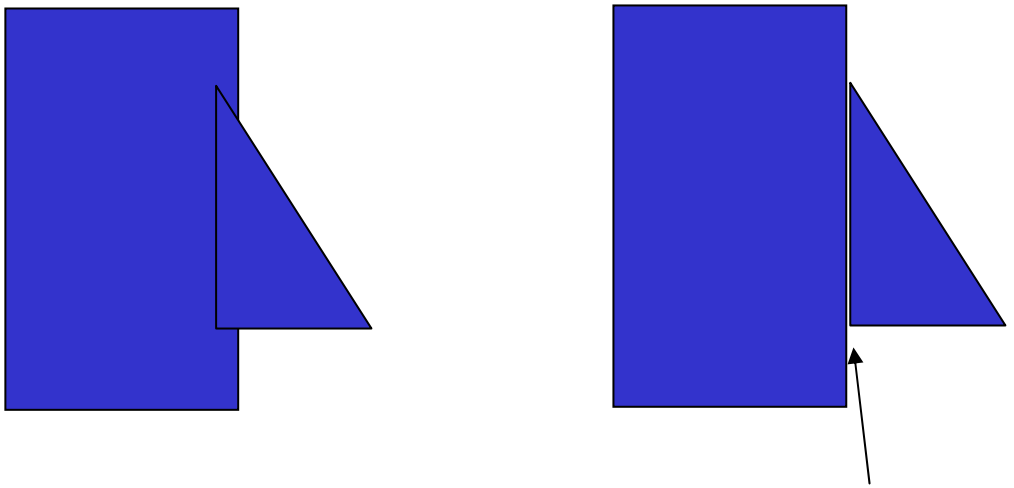
Disaster #3: Open circuits

Symptom: Occurrence of gaps in mask pattern

- When drawing shapes, overlap or “and” data areas to guarantee closed patterns



Nice overlap

Open circuit

- GDSII only allows square-ended wires
  - Rounded or beveled wires will be truncated to squares – this can create opens in your pattern

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Disaster #4: “Hmm, this doesn’t look right”

Symptom: Printed wafer looks perfect, but why do all the text labels look wrong?

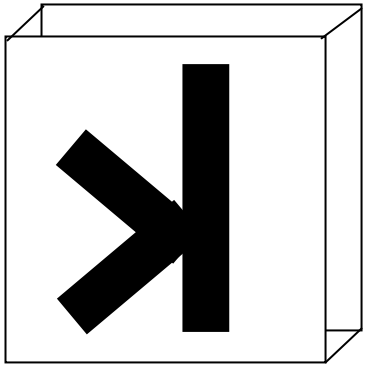
- Draw your data as you intend it to look on the wafer
- “Reading” is defined as how the mask looks when **chrome side is up**
  - Frontside masks are typically “Wrong” reading
  - Backside masks need to be “Right” reading

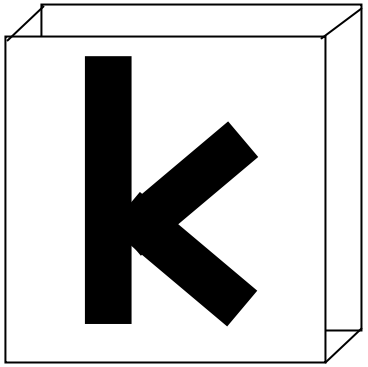
What’s in your data file:

Wrong reading:

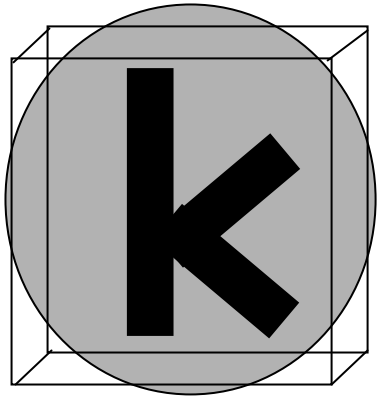
Right reading:

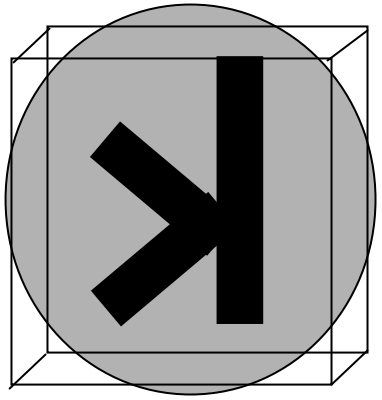
Chrome side up





Chrome side down, against wafer





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Disaster #5: “Why did it cost so much?!”

Symptom: Racing heartbeat upon receipt of bill

- Avoid polygons as much as possible
  - If you have a huge number of polygons, check with your mask vendor first
  - Get a vendor estimate on mask write time to avoid sticker shock

- Don’t “flatten” your data! (L-edit)
  - Flattening removes cell hierarchy
  - Data file becomes huge

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Final Notes

- Check your file (prior to GDSII conversion)
  - Have a colleague review your work
  - Sleep on it
  - Review design rules

- Check after GDSII conversion, too
  - Use a free GDSII viewer: http://www.dolphin.fr/medal/socgds/socgds_free_overview.html
  - Make sure everything is there!

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Need Help?

- A. M. Fitzgerald & Associates does end-to-end MEMS development, including photomask design
  - Knowledgeable about SNF exposure tools, as well as local commercial vendors
  - We use Tanner EDA L-edit
  - Custom L-edit templates
  - Custom test chip patterns
  - Macros
  - Get it done quickly and accurately!

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