**CS4100 HW4 Answer Key**

1. 題目問 ld, sd, add, sub, beq 五個指令，(a)(b)(c)一個指令算一分
   (a) (5%) ld, sd
   (b) (5%) add, sub
   (c) (5%) beq

2.
   (a) (7%) $00CE3623_{hex} = 0000\ 0000\ 1100\ 1110\ 0011\ 0110\ 0010\ 0011_2$

| imm[11:5] | rs2 | rs1 | func3 | imm[4:0] | opcode |
|---|---|---|---|---|---|
| 0000000 | 01100 | 11100 | 011 | 01100 | 0100011 |

   sd x12, 12(x28)
   Branch 0
   MemRead 0
   MemtoReg, X
   ALUOp 00
   MemWrite 1
   ALUSrc 1
   RegWrite 0
   (1個signal算1分)
   (b) (3%) Reg[28], $12_{10} (= 0000\ 0000\ 0000\ 000C_{hex})$ (錯一個扣2分)

3. 有寫出要加上哪些項目但數字抄錯或計算錯誤扣2分，其餘全錯
   (a) (4%) add: 20(PC Read) + 230(I-Mem) + 130(Register File) + 20(Mux) + 180(ALU) + 20(Writing Mux) + 10(Register Setup) = **610 ps**
   (b) (3%) ld: 20(PC Read) + 230(I-Mem) + 130(Register File) + 180(ALU) + 230(D-Mem) + 20(Mux) + 10(Register Setup) = **820 ps**
   (c) (3%) sd: 20(PC Read) + 230(I-Mem) + 130(Register File) + 180(ALU) + 230(D-Mem) = **790 ps**

4.
   (a) (3%) No. (1分)
   (紅色部分如果是有提到ALU本來就有slt的功能的話也給分)
   slt is an R-type instruction and the current design can handle R-type instructions already. Only the ALU needs to be modified, i.e., add the set-less-than operation. There is no need to add new blocks or wires. (理由2分)

   (b) (3%) No. (1分)
   The "Control" unit takes the op code of the instruction as the input and generates the control signals for that instruction. Since the op code of each R-type instruction, including slt, is the same, the "Control" unit does not need to change for slt. (理由2分，需要寫到因為跟R-type是一樣的，沒提到扣1分)
   (c) (4%) Yes, (1分)
   The "ALU control" unit needs to output 0111 if the ALUop is 10 and func3 field is 010. (理由3分，要說利用到 func3，沒提到扣 2分 )

5.

(a) (4%)
five-stage pipelined: 450 ps (2%, 寫錯0分)
single-cycle processor: 1750 ps (2%, 計算錯誤扣1分)

(b) (4%)
five-stage pipelined: 2250 ps (2%, 計算錯誤扣1分)
single-cycle processor: 1750 ps (2%, 計算錯誤扣1分)

(c) (2%)
Split the EX stage. New clock period: 400 ps
(Split其他stage直接0分, 如果 split EX 但是 new clock period算錯扣1分)

6. Clock period = 2 ns ((a), (b) 都各占1分)

(a) (5%)
(4-1) + S = 50/2 (clock cycles) => S = 22 (2分)
(4-1) +4S = 3 + 4*22 = 91 (clock cycles) => 91*2 = 182 (ns) (2分)
182ns

(b) (5%)
(N-1) + S = 100/2 = 50 (clock cycles) (1)
(N-1) + 4S = 340/2 = 170 (clock cycles) (2)
(2)- (1) => 3S = 120 => S =40
(1) and S = 40 => N = 11
S = 40, N = 11 (每個答案各2分)

7.

(a) (4%)
and x28, x11, x29
NOP
NOP
ld x14, 8(x28)
ld x11, 4(x12)
NOP
NOP
ld x28, 0(x11)
NOP
NOP
sub x14, x28, x14
NOP
NOP
sd x11, 4(x14)
共需要insert 8個NOP。
共有4組(每組有2個連續NOP), 每組占1分(少插一個就不給分)

(b) (12%)
(i) (4%) 5, 7 (各2分)
(ii) (4%) 4, 10 (各2分)
(iii) (4%) 7, 9 (各2分)

(c) (4%)
12 cycles

8.

(a) (4%)

always taken: $\frac{3}{7}$ (or 42.86%)

always not taken: $\frac{4}{7}$ (or 57.14%)

每個答案兩分

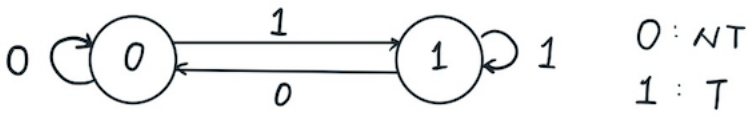
**(b)** (3%)

**Accuracy:** $\frac{5}{7}$ (or 71.43%)

**T**: taken
**NT**: not taken
**O**: Correct
**X**: Incorrect

| Ground truth | T | T | T | NT | NT | NT | NT |
|---|---|---|---|---|---|---|---|
| State | NT | T | T | T | NT | NT | NT |
| Decision (Predict) | NT | T | T | T | NT | NT | NT |
| Correctness | X | O | O | X | O | O | O |

如果過程寫對，但結果(accuracy)計算錯誤，扣1 分，其餘錯誤0 分




(c) (3%)

**Accuracy:** $\frac{5}{7}$ (or 71.43%)

**ST**: Strongly taken
**WT**: Weakly taken
**WNT**: Weakly not taken
**SNT**: Strongly not taken
**O**: Correct
**X**: Incorrect

| Ground truth | T | T | T | NT | NT | NT | NT |
|---|---|---|---|---|---|---|---|
| State | ST | ST | ST | ST | WT | WNT | SNT |
| Decision (Predict) | T | T | T | T | T | NT | NT |
| Correctness | O | O | O | X | X | O | O |

答案對就給分

如果過程寫對，但結果(accuracy)計算錯誤，扣1 分，其餘錯誤0 分

9. (5%)

| IF | ID | EX | MEM | WB |
|---|---|---|---|---|
| The first instruction of the exception handler | NOP | NOP | sub x6, x31, x28 | add x10, x28, x29 |

寫對1格得1分，全對得5分