

109062320 朱季葳 , discuss with 109062233, 109062306, 109062123,109062323

1.

(a) (6 points) Record the results for the two programs using CycC and InsC for “add_recur” function of “ADD_recursive” and for “add_iter” function of “ADD_iterative”. Based on your understanding of the characteristics of the two programs, compare the differences in their profiles.

Simulator Profiling

Total Self Cycle Count: 900

Name	Calls	Self InsC	Self CycC	Total InsC	Total CycC	Time Percentage
do_printf	1	209	464	285	599	51.56%
add_iter	1	66	105	66	105	11.67%
strlen	1	27	50	27	50	5.56%
vprintf_help	3	27	45	27	45	5.00%
__riscv_save_12	1	22	40	22	40	4.44%
memset	1	26	38	35	51	4.22%
_start	1	24	36	477	900	4.00%
vprintf	1	25	35	317	652	3.89%
printf	1	15	21	332	673	2.33%
main	1	12	20	410	798	2.22%
_write	1	7	18	7	18	2.00%
_exit	1	8	15	8	15	1.67%
memset + 84	1	9	13	9	13	1.44%

result of ADD_iterative

add_iter :InsC 66 CycC 105

Simulator Profiling

Total Self Cycle Count: 1171

Name	Calls	Self InsC	Self CycC	Total InsC	Total CycC	Time Percentage
do_printf	1	209	468	285	600	39.97%
add_recur	1	276	375	276	375	32.02%
strlen	1	27	50	27	50	4.27%
vprintf_help	3	27	42	27	42	3.59%
__riscv_save_12	1	22	40	22	40	3.42%
memset	1	26	39	35	51	3.33%
_start	1	24	36	687	1,171	3.07%
vprintf	1	25	35	317	653	2.99%
printf	1	15	21	332	674	1.79%
main	1	12	20	620	1,069	1.71%
_write	1	7	18	7	18	1.54%
_exit	1	8	15	8	15	1.28%
memset + 84	1	9	12	9	12	1.02%

result of ADD_recursive

add_recur :InsC 276 CycC 375

By the above graph, we can see that the instruction count and clock cycle count of recursion are bigger than the ones of iteration

and the CPI of recursion is $375/276 = 1.358$, the CPI of iteration is $105/66 = 1.59$

As a result, we can see that the CPI of iteration is bigger

Furthermore, as we know about recursion, it calls it self until the terminal condition, and it is far more time-consuming than iteration in which just run a loop.

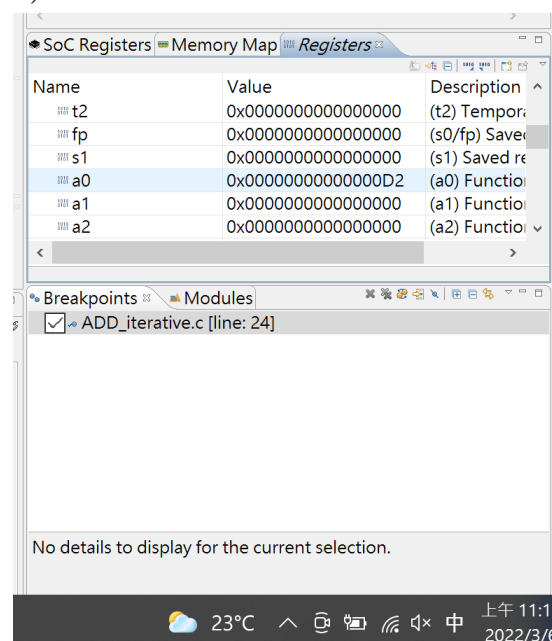
(b) (6 points) RISC-V has 32 general purpose registers, whereas X86 (a CISC architecture) only has 8. Why does RISC have more registers than CISC?

The primary goal of CISC architecture is to complete a task in as few lines of assembly code as possible while RISC architecture only use simple instructions that can be executed within 1 clock cycle.

As a result, RISC need more registers to store the instructions.

I take reference on <https://cs.stanford.edu/people/eroberts/courses/soco/projects/risc/riscisc/>

When executing “ADD_iterative” , which register stores the return value for add_iter function? (You can select debug icon to view the contents of all registers. Note that you should set breakpoints at the right spots.)



By the above image, after set breakpoint in the line after calling function,we can see the register “a0” store the return value for add_iter function

a0	function argument 0 / return value 0
a1	function argument 1 / return value 1

Besides, by the description of a0 and a1, we can see that a1 also store the return value

(c) (6 points) What are the average CPI for “add_recur” function in ADD_recursive.c and “add_iter” function in ADD_iterative.c, respectively?

CPI of recursion is $375/276 = 1.36$, the CPI of iteration is $105/66 = 1.59$

(d) (6 points) What are the CPU execution time for “add_recur” function in ADD_recursive.c and “add_iter” function in ADD_iterative.c, respectively, on a processor with a clock rate of 1GHz?

execution time of recursion is $375/(1 \times 10^9) = 0.000000375 = 0.375\text{ms} \approx 0.38\text{ms}$

execution time of iteration is $105/(1 \times 10^9) = 0.000000105 = 0.105\text{ms} \approx 0.11\text{ms}$

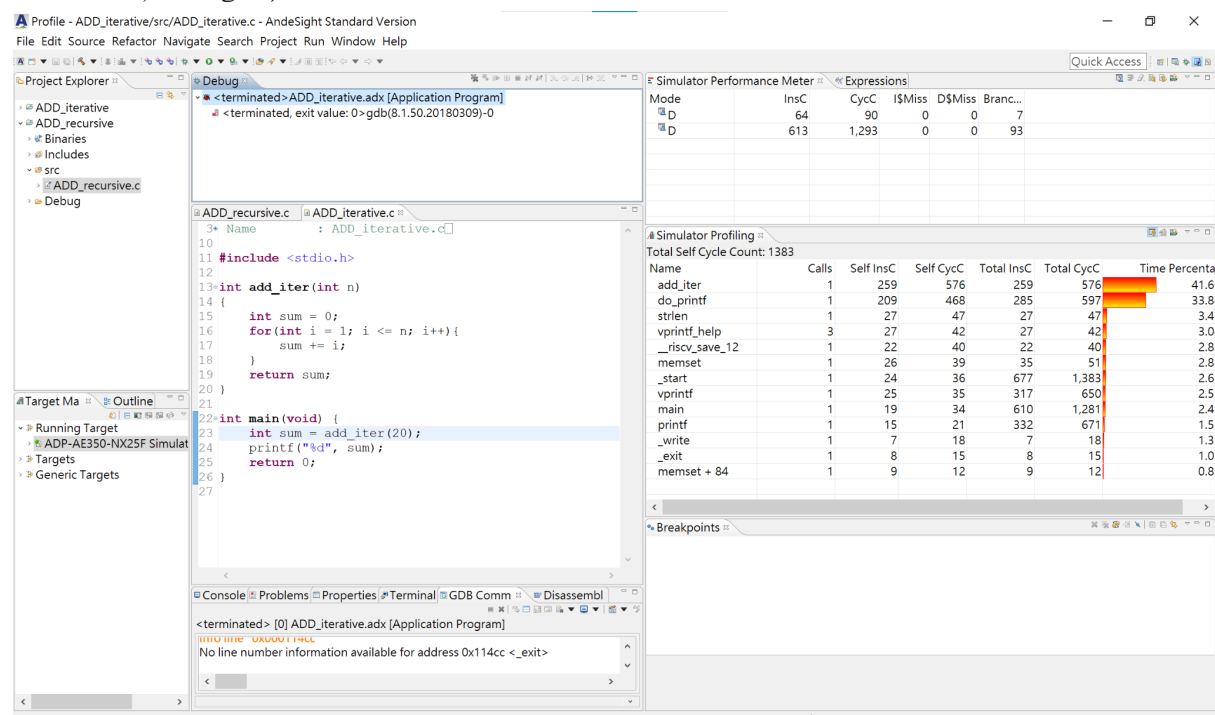
(e) (6 points) Assume we execute ADD_iterative.c in (d) but with a 4-core multiprocessor instead and also employ parallelization techniques on add_iter function to equally allocate computation to each core. But, the parallelization increases 50 communication cycles on the multiprocessor. What is the program execution time now? (Hint: Only add_iter can be parallelized.)

total cycle = 900

clock cycle count = $900 - 105 + 50 + 105/4 = 872$

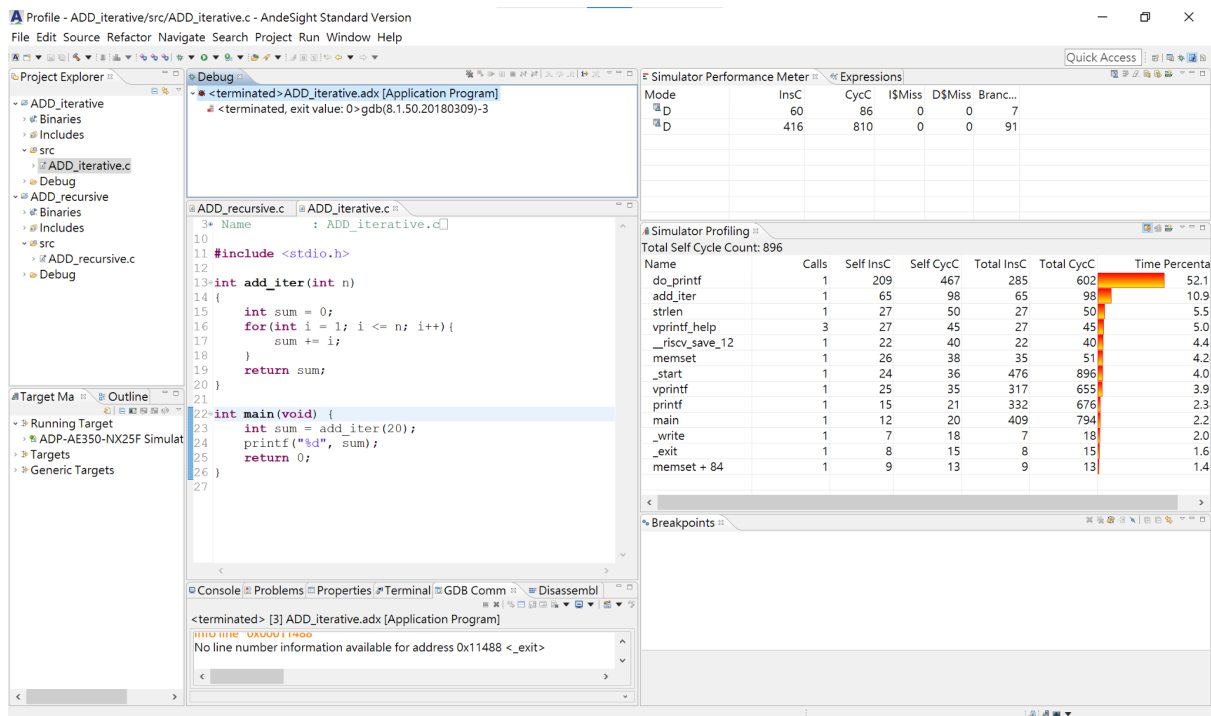
execution time = $872 / 10^9 = 0.872 \text{ ms} \approx 0.87\text{ms}$

(f) (20 points) Compiler will affect program performance. Compile ADD_recursive.c and ADD_iterative.c with two optimization levels, -O0 and -O1, respectively. Compare the performance of “add_recur” and “add_iter” function in ADD_recursive.c and ADD_iterative.c for different optimization levels (-O0 and -O1). You should report CycC, InsC and CPI and explain the differences in their profiles. (To change optimization level, see Fig. 1.)



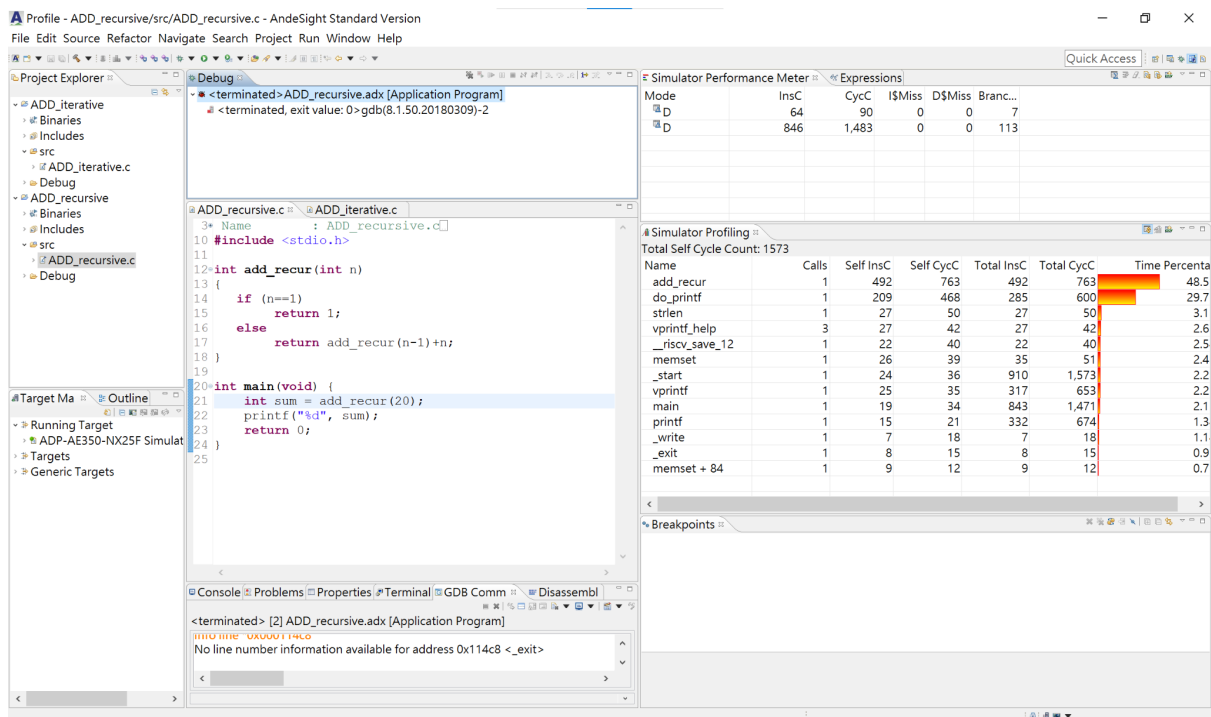
result of iteration with -O0

CycC: 576, InsC: 259, CPI: $576/259 = 2.2239 \approx 2.22$



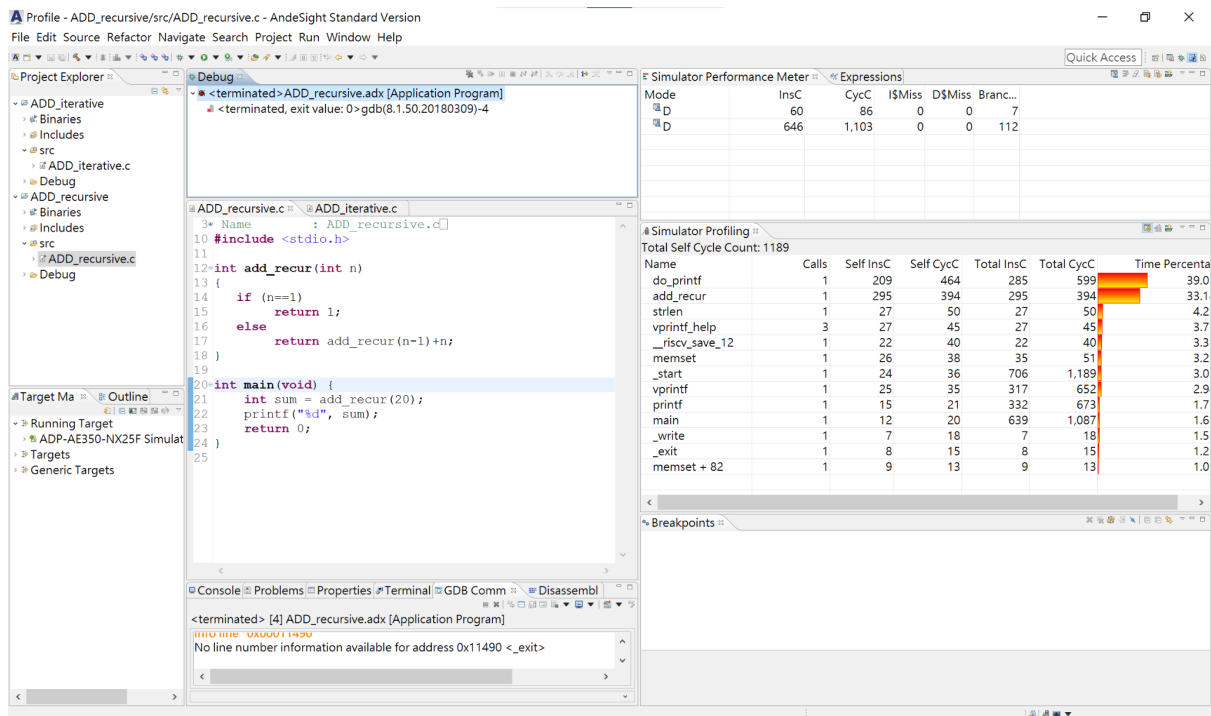
result of iteration with -O1

CycC: 98, InsC: 65, CPI: $98/65 = 1.5076 \approx 1.51$



result of recursion with -O0

CycC: 763, InsC: 492, CPI: $763/492 = 1.5508 \approx 1.55$



result of recursion with -O1

CycC: 394, InsC: 295, CPI: $394/295 = 1.3355 \approx 1.34$

By the above images, we can see that O1 has less CycC, InsC and CPI than O0.

I take reference on the official website: <https://gcc.gnu.org/onlinedocs/gcc/Optimize-Options.html>

O0 compiler is the original one which doesn't have any optimization, while O1 compiler optimizes compilations that take more time and more memory for a large function.

Besides, O1 compiler will try to reduce code size and execution time without performing the optimizations that take lots of compilation time.

As for the original setting --> -Og

Optimize debugging experience. -Og should be the optimization level of choice for the standard edit-compile-debug cycle, offering a reasonable level of optimization while maintaining fast compilation and a good debugging experience.

It is a better choice than -O0 for producing debuggable code because some compiler passes that collect debug information are disabled at -O0

2. (20 points) Go to SPEC Benchmarks website and search for the benchmarks of the following systems: • Intel DH87MC Motherboard (Intel Core i3-4340) • Intel DH87MC Motherboard (Intel Core i5-4430) • Intel DH87MC Motherboard (Intel Core i7-4770)

We want to compare the performance of the three computer systems using different methods to normalize the performance.

(a) (5 points) Compare the hardware and software specifications of these three motherboards and identify their differences.

Hardware CPU Name: Intel Core i3-4340 CPU Characteristics: 3600 CPU MHz: Integrated FPU: 2 cores, 1 chip, 2 cores/chip, 2 threads/core CPU(s) enabled: 1 chip CPU(s) orderable: 32 KB I + 32 KB D on chip per core Primary Cache: 256 KB I+D on chip per core Secondary Cache: 4 MB I+D on chip per chip L3 Cache: None Other Cache: 8 GB (2 x 4 GB 2Rx4 PC3-12800U-11) Memory: 1 TB Seagate SATA HDD, 7200 RPM Disk Subsystem: None Other Hardware:	Software Operating System: Microsoft Windows 8.1 Pro 6.3.9600 N/A Build 9600 Compiler: C/C++: Version 14.0.1.139 of Intel C++ Studio XE for Windows; Libraries: Version 16.00.30319.01 of Microsoft Visual Studio 2010 Professional SP1 Auto Parallel: Yes File System: NTFS System State: Default Base Pointers: 32/64-bit Peak Pointers: 32/64-bit Other Software: SmartHeap Library Version 10.0 from http://www.microquill.com/
Hardware CPU Name: Intel Core i5-4430 CPU Characteristics: Intel Turbo Boost Technology up to 3.20 GHz CPU MHz: 3000 FPU: Integrated CPU(s) enabled: 4 cores, 1 chip, 4 cores/chip CPU(s) orderable: 1 chip Primary Cache: 32 KB I + 32 KB D on chip per core Secondary Cache: 256 KB I+D on chip per core L3 Cache: 6 MB I+D on chip per chip Other Cache: None Memory: 8 GB (2 x 4 GB 2Rx4 PC3-12800U-11) Disk Subsystem: 1 TB Seagate SATA HDD, 7200 RPM Other Hardware:	Software Operating System: Microsoft Windows 8.1 Pro 6.3.9600 N/A Build 9600 Compiler: C/C++: Version 14.0.1.139 of Intel C++ Studio XE for Windows; Libraries: Version 16.00.30319.01 of Microsoft Visual Studio 2010 Professional SP1 Auto Parallel: Yes File System: NTFS System State: Default Base Pointers: 32/64-bit Peak Pointers: 32/64-bit Other Software: SmartHeap Library Version 10.0 from http://www.microquill.com/
Hardware CPU Name: Intel Core i7-4770 CPU Characteristics: Intel Turbo Boost Technology up to 3.90 GHz CPU MHz: 3400 FPU: Integrated CPU(s) enabled: 4 cores, 1 chip, 4 cores/chip, 2 threads/core CPU(s) orderable: 1 chip Primary Cache: 32 KB I + 32 KB D on chip per core Secondary Cache: 256 KB I+D on chip per core L3 Cache: 8 MB I+D on chip per chip Other Cache: None Memory: 8 GB (2 x 4 GB 2Rx4 PC3-12800U-11) Disk Subsystem: 1 TB Seagate SATA HDD, 7200 RPM Other Hardware:	Software Operating System: Microsoft Windows 8.1 Pro 6.3.9600 N/A Build 9600 Compiler: C/C++: Version 14.0.1.139 of Intel C++ Studio XE for Windows; Libraries: Version 16.00.30319.01 of Microsoft Visual Studio 2010 Professional SP1 Auto Parallel: Yes File System: NTFS System State: Default Base Pointers: 32/64-bit Peak Pointers: 32/64-bit Other Software: SmartHeap Library Version 10.0 from http://www.microquill.com/

Firstly, we compare the differences in software. We can see that there is no difference in software among these three motherboards.

As for the differences in hardware, there are four differences:

1. Turbo-Boost, i3 doesn't have turbo-boost enabled, while i5 and i7 have; besides, i7's speed is faster than i5.

2. cores, i3 has 4 cores, i5 has at least 4 cores while i7 has at least 6 cores

3. cache memory, the storage of cache memory in i7 > i5 > i3

4. the running frequency, the running frequency in i3 > i7 > i5

(b) (5 points) Consider the three benchmarks: 464.h264ref, 471.omnetpp, and 473.astar in the results table.

Please use the first column of "seconds" (check Fig. 4) to calculate the relative performance of the three computer systems based on the three benchmarks.

Fill out the following table, which uses each of the three computers as the reference for comparison.

Summarize the performance results with the arithmetic mean of the performance ratios of the three benchmark programs. Please show the calculation procedure.

464.h264ref

	performance ratio		
reference	intel core i3-4340	intel core i5-4430	intel core i7-4770
intel core i3-4340	1	$323/373=0.87$	$323/323=1$
intel core i5-4430	$373/323=1.16$	1	$373/323=1.16$
intel core i7-4770	$323/323=1$	$323/373=0.87$	1

471.omnetpp

	performance ratio		
reference	intel core i3-4340	intel core i5-4430	intel core i7-4770
intel core i3-4340	1	$257/251=1.02$	$257/223=1.15$
intel core i5-4430	$251/257=0.98$	1	$251/223=1.13$
intel core i7-4770	$223/257=0.87$	$223/251=0.89$	1

473.astar

	performance ratio		
reference	intel core i3-4340	intel core i5-4430	intel core i7-4770
intel core i3-4340	1	$233/247=0.94$	$233/200=1.17$
intel core i5-4430	$247/233=1.06$	1	$247/200=1.24$
intel core i7-4770	$200/233=0.86$	$200/247=0.81$	1

Arithmetic mean

	performance ratio		
reference	intel core i3-4340	intel core i5-4430	intel core i7-4770
intel core i3-4340	1	$(1.02+0.87+0.94)/3$ =0.94	$(1.15+1+1.17)/3$ =1.11
intel core i5-4430	$(0.98+1.16+1.06)/3$ =1.07	1	$(1.13+1.16+1.24)/3$ =1.18
intel core i7-4770	$(0.87+1+0.86)/3$ =0.91	$(0.89+0.87+0.81)/3$ =0.86	1

(c) (5 points) Repeat (b) with the geometric mean of the performance ratios of the three benchmark programs.

	performance ratio		
reference	intel core i3-4340	intel core i5-4430	intel core i7-4770
intel core i3-4340	1	$(1.02*0.87*0.94)^{(1/3)}$ =0.94	$(1.15*1*1.17)^{(1/3)}$ =1.10
intel core i5-4430	$(0.98*1.16*1.06)^{(1/3)}$ =1.06	1	$(1.13*1.16*1.24)^{(1/3)}$ =1.18
intel core i7-4770	$(0.87*1*0.86)^{(1/3)}$ =0.91	$(0.89*0.87*0.81)^{(1/3)}$ =0.86	1

(d) (5 points) Which observations can you make from (b) and (c)? How are these results compared with SPECint_base2006 ratio?

We can see that there is little difference between geometric mean and arithmetic mean; what's more, it shows that the performance of $i7 > i3 > i5$.

But the result of arithmetic mean looks more changeable than geometric mean.

After comparing with the result of SPECint_base2006, we can also see that the performance of

$i7 > i3 > i5$ (The SPECint_base2006 is $i3 : 52.3$ $i5 : 48.3$ $i7 : 59.6$)

3. (10 points) Assume a program requires the execution of 90×10^6 FP instructions, 110×10^6 INT instructions, 100×10^6 L/S instructions, and 25×10^6 branch instructions. The CPI for each type of instruction is 2, 1, 5, and 2, respectively. Assume that the processor has a 4GHz clock rate.

1. (a) (5 points) By how much must we improve the CPI of FP instructions if we want the program to run two times faster? Please show the calculation procedure.

$$\text{clock cycles} = (90 \times 10^6 \times 2) + (110 \times 10^6 \times 1) + (100 \times 10^6 \times 5) + (25 \times 10^6 \times 2)$$

$$= (180 + 110 + 500 + 50) \times 10^6 = 840 \times 10^6$$

$$\text{run two times faster} \rightarrow \text{clock cycles} / 2 \text{ (clock rate is fixed)} = 420 \times 10^6$$

$$\text{new CPI of FP instruction} = (420 - 110 - 500 - 50) \times 10^6 / (90 \times 10^6)$$

$$= -240 / 90 \rightarrow \text{it is impossible!}$$

2. (b) (5 points) By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 31% and the CPI of L/S and Branch is reduced by 7%? Please show the calculation procedure.

$$\text{clock cycles} = \{0.69 \times [(90 \times 10^6 \times 2) + (110 \times 10^6 \times 1)]\}$$

$$+ \{0.23 \times [(100 \times 10^6 \times 5) + (25 \times 10^6 \times 2)]\}$$

$$= (290 \times 0.69 + 550 \times 0.23) \times 10^6 = 326.6 \times 10^6$$

$$\text{because clock rate is fixed: } 326.6 / 840 = 0.388 \approx 39\% \text{ improved}$$

so the improvement is 61%

4. (10 points) Processor P1 has a clock rate of 5GHz and a voltage of 1.25V. Assume that, on average, it consumes 60W of static power and 90W of dynamic power. Assume that the dynamic power and static power are respectively calculated by the following equations:

$$\text{dynamic power} = 1/2 \times \text{capacitive load} \times \text{voltage}^2 \times \text{clock frequency}$$

$$\text{static power} = \text{voltage} \times \text{leakage current}$$

- (a) (2 points) Find the average capacitive load.

$$\text{capacitive load} = 2 \times \text{dynamic power} / (\text{voltage}^2 \times \text{clock frequency})$$

$$P1: \text{capacitive load} = 2 \times 90 / (1.25^2 \times 5 \times 10^9)$$

$$= 2.30 \times 10^{-8}$$

- (b) (2 points) Find the percentage of the total dissipated power comprised by dynamic power and the ratio of static power to dynamic power.

$$\begin{aligned} \text{percentage of total dissipated power comprised by dynamic power} \\ 90 / (90 + 60) = 0.6 \end{aligned}$$

$$\text{ratio of static power to dynamic power} = 60/90 = 0.67$$

- (c) (6 points) If the total dissipated power is to be reduced by 35%, how much should the voltage be reduced to maintain the same leakage current?

abbreviate Static power, dynamic power, voltage, capacitive load,

clock frequency, leakage current to S, D, V, C, F, L

$$(S_{\text{new}} + D_{\text{new}}) / (S_{\text{old}} + D_{\text{old}}) = 0.65, \quad V_{\text{new}} = \frac{(2 \times D_{\text{new}} / (C \times F))^{1/2}}{1}, \quad D_{\text{new}} = 0.65 \times (S_{\text{old}} + D_{\text{old}}) - S_{\text{new}}$$

$$S_{\text{new}} = V_{\text{new}} \times L, \quad S_{\text{old}} = V_{\text{old}} \times L \rightarrow S_{\text{new}}/V_{\text{new}} = S_{\text{old}}/V_{\text{old}}$$

$$L = 60 / 1.25 = 48$$

$$D_{\text{new}} = 0.65 \times (60 + 90) - V_{\text{new}} \times 48 = 97.5 - V_{\text{new}} \times 48$$

$$V_{\text{new}} = [(2 \times 97.5 - V_{\text{new}} \times 96) / (2.3 \times 10^{-8} \times 5 \times 10^9)]^{1/2} = 0.95$$

$$V_{old} = 60 / 48 = 1.25$$

$$V_{new}/V_{old} = 0.95/1.25 = 0.76, \text{ the voltage reduced by } 24\%$$

5. (10 points) Assume that a 25 cm diameter wafer has a cost of 15, contains 120 dies, and has 0.02 defects/cm².

(a) (3 points) Find the yield for this wafer using the equation on page 28 of the textbook

(or page 28 of the lecture notes of Chapter 1).

$$\text{Die area} = \pi \times 12.5^2 / 120 = 4.09$$

$$\text{Yield} = 1 / ((1 + \text{Defects per area} \times \text{Die area} / 2))^2$$

$$= 1 / ((1 + 0.02 \times 4.09 / 2))^2$$

$$= 0.92$$

(b) (3 points) Find the cost per die for this wafer.

$$15 / (120 \times 0.92) = 0.14$$

(c) (4 points) If the number of dies per wafer is increased by 20% and the defects per area unit increases by 35%, find the die area and yield.

$$\text{number of dies per wafer} = 120 \times 1.2 = 144$$

$$\text{die area} = \pi \times 12.5^2 / 144 = 3.41$$

$$\text{Yield} = 1 / ((1 + 0.02 \times 1.35 \times 3.41 / 2))^2 = 0.91$$