Department of Computer Science
National Tsing Hua University
CS4100 Computer Architecture
Spring 2022 Homework 4

Deadline: 2022/05/19 10:00

1. (15 points) A common defect in silicon chips is for one signal wire to always get a constant logic value 0 (1, respectively); it is called a stuck-at-0 (stuck-at-1, respectively) fault. Consider the single-cycle processor for the following instructions: `ld`, `sd`, `add`, `sub` and `beq`.
   (a) (5 points) Which instruction(s) could fail to operate correctly if the ALUSrc wire is stuck at 0?
   (b) (5 points) Which instruction(s) could fail to operate correctly if the MemtoReg wire is stuck at 1?
   (c) (5 points) Which instruction(s) could fail to operate correctly if the ALUop0 wire is stuck at 0?

2. (10 points) Consider the execution of the machine instruction $00CE3623_{hex}$ on the single-cycle processor.
   (a) (7 points) What are the values of the signals: Branch, MemRead, MemtoReg, ALUOp, MemWrite, ALUSrc and RegWrite?
   (b) (3 points) What are the input values of the ALU? You can use Reg[x] to denote the value of register x.

3. (10 points) Assume that the positive edge-triggered clocking methodology is adopted and the logic blocks used to implement the single-cycle processor have the following delay values:

I-Mem/ D-Mem	Register File	Mux	ALU	Adder	Single Gate	PC Read	Register Setup	Sign Extend	Control
230 ps	130 ps	20 ps	180 ps	130 ps	5 ps	20 ps	10 ps	30 ps	30 ps

   "I-Mem/D-Mem" is the amount of time to access the Instruction or Data Memory.
   "Register File" is the amount of time to read rs1 and rs2.
   "PC Read" is the amount of time for the new PC value to appear on the output after a rising clock edge; this delay value applies to the PC only.
   "Register Setup" is the amount of time a register's data input must be stable before a rising clock edge; this delay value applies to both the PC and Register File.

   (a) (4 points) What is the latency of an `add` instruction (i.e., what is the minimum clock period to ensure that this instruction works correctly)?
   (b) (3 points) What is the latency of an `ld` instruction (i.e., what is the minimum clock period to ensure that this instruction works correctly)?
   (c) (3 points) What is the latency of an `sd` instruction (i.e., what is the minimum clock period to ensure that this instruction works correctly)?

4. (10 points) Recall that the ALU introduced in Chapter 3 can support the set-less-than (slt) operation by setting the ALU operation to 0111. Now consider how to modify the single-cycle processor such that it can also execute the R-type instruction: slt rd, rs1, rs2.
   (a) (3 points) Are additional logic blocks or wires needed? Justify your answer.
   (b) (3 points) Does the "Control" unit need any change? Justify your answer.
   (c) (4 points) Does the "ALU control" unit need any change? Justify your answer.

5. (10 points) Assume that individual stages of a datapath have the following latencies:

IF	ID	EX	MEM	WB
300 ps	400 ps	450 ps	350 ps	250

   (a) (4 points) What are the clock periods in a five-stage pipelined processor and a single-cycle processor, respectively?
   (b) (4 points) What are the latencies of an sd instruction in a five-stage pipelined processor and a single-cycle processor, respectively?
   (c) (2 points) If you can split one stage of the five-stage pipelined processor into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock period? Note that the new clock period must be minimum among all possible ways of splitting.

6. (10 points) Answer the following questions by assuming the clock rate is 500 MHz and no pipeline stalls occur.
   (a) (5 points) If a 4-stage pipelined processor takes 50 ns to execute S instructions, how long will it take to execute 4S instructions?
   (b) (5 points) Consider a pipelined processor which has N stages. If it takes 100 ns to execute S instructions and 340 ns to execute 4S instructions. What are N and S, respectively?

7. (20 points) Consider the following sequence of instructions executed on the five-stage pipelined processor. Assume that the execution starts in clock cycle 1.

```
and x28, x11, x29
ld x14, 8(x28)
ld x11, 4(x12)
ld x28, 0(x11)
sub x14, x28, x14
sd x11, 4(x14)
```

   (a) (4 points) Assume both forwarding unit and hazard detection unit are not present in the processor. Insert a minimum number of `NOP` (no operation) instructions to ensure correct execution.
   (b) (12 points) Assume the processor has the forwarding unit and hazard detection unit. For each of the following three conditions, indicate in which clock cycle, it is true for the processor.
      (i) (4 points) All control signals to be stored in the ID/EX register are set to 0.
      (ii) (4 points) The correct data is forwarded from the EX/MEM register to one ALU input.
      (iii) (4 points) The correct data is forwarded from the MEM/WB register to one ALU input.
   (c) (4 points) Assume the processor has the forwarding unit and hazard detection unit. How many clock cycles does the processor take to complete the execution of the code?

8. (10 points) Consider the sequence of branch outcomes: T, T, T, NT, NT, NT, NT, for a branch instruction that has been executed 7 times in a program, where T denotes taken and NT denotes not-taken.
   (a) (4 points) What are the accuracy rates of the always-taken and always-not-taken predictors for this sequence of branch outcomes, respectively?
   (b) (3 points) Consider a 1-bit dynamic predictor which starts at the NT state. What is the accuracy rate of the predictor for this sequence of branch outcomes?
   (c) (3 points) Consider a 2-bit dynamic predictor which starts at the "strongly predict taken" state. What is the accuracy rate of the predictor for this sequence of branch outcomes?

9. (5 points) Consider the execution of the following sequence of instructions on the five-stage pipelined processor:

```
add x10, x28, x29
sub x6, x31, x28
beq x28, x29, LABEL
sd x28, 0(x29)
```

   Suppose the third instruction is detected to have an invalid target address and cause an exception in the ID stage (i.e., in clock cycle 4). What instructions will appear in the IF, ID, EX, MEM, and WB stages, respectively, in clock cycle 5? Note that each instruction in your answer should be one chosen from the given instructions, the NOP instruction (or bubble), and the first instruction of the exception handler.