VHDL calculator project BEL3

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Contents

Chapter 1

Design Unit Index

1.1 Design Unit List

Here is a list of all design unit members with links to the Entities they belong to:

Chapter 2

File Index

2.1 File List

Here is a list of all documented files with brief descriptions:

Chapter 3

Class Documentation

3.1 io_ctrl Entity Reference

IO Control Unit Testbench Entity.

Entities

- rtl architecture

  IO Control Unit Architecture.
- sim architecture

  IO Control Unit Testbench Architecture.

Libraries

- IEEE

Use Clauses

- std_logic_1164

Ports

- clk_i **in std_logic**
- reset_i **in std_logic**
- dig0_i **in std_logic_vector(7 downto 0)**
- dig1_i **in std_logic_vector(7 downto 0)**
- dig2_i **in std_logic_vector(7 downto 0)**
- dig3_i **in std_logic_vector(7 downto 0)**
- led_i **in std_logic_vector(15 downto 0)**
- sw_i **in std_logic_vector(15 downto 0)**
- pb_i **in std_logic_vector(15 downto 0)**
- ss_o **out std_logic_vector(7 downto 0)**
- ss_sel_o **out std_logic_vector(3 downto 0)**
- swsync_o **out std_logic_vector(15 downto 0)**
- pbsync_o **out std_logic_vector(3 downto 0)**

3.1.1 Detailed Description

IO Control Unit Testbench Entity.

IO Control Unit Entity.

The IO Control uniti part of the calculator project.

The documentation for this class was generated from the following files:

- tb/tb_io_ctrl_.vhd
- vhdl/io_ctrl_.vhd

3.2 rtl Architecture Reference

IO Control Unit Architecture.

Processes

- p_slowen**(clk_i , reset_i)**
  IO Control Unit Architecture.
- p_debounce**(clk_i , reset_i)**
  IO Control Unit Architecture.
- p_display_ctrl**(clk_i , reset_i)**
  IO Control Unit Architecture.

Libraries

- IEEE

Use Clauses

- std_logic_1164
- std_logic_arith

Constants

- C_ENCOUNTVAL **std_logic_vector(16 downto 0):=" 11000011010100000 "**

Signals

- s_enctr **std_logic_vector(16 downto 0)**
- s_1khzen **std_logic**
- swsync **std_logic_vector(15 downto 0)**
- pbsync **std_logic_vector(3 downto 0)**
- s_ss_sel **std_logic_vector(3 downto 0)**
- s_ss **std_logic_vector(7 downto 0)**

3.2.1 Detailed Description

IO Control Unit Architecture.

The IO Control uniti part of the calculator project.

3.2.2 Member Function Documentation

3.2.2.1 p_debounce()

```
p_debounce(
              clk_i  ,
              reset_i  )  [Process]
```

IO Control Unit Architecture.

Process for button debounce.

3.2.2.2 p_display_ctrl()

```
p_display_ctrl(
              clk_i  ,
              reset_i  )  [Process]
```

IO Control Unit Architecture.

Process to control 7 segment displays.

3.2.2.3 p_slowen()

```
p_slowen(
              clk_i  ,
              reset_i  )  [Process]
```

IO Control Unit Architecture.

Process for 1kHz signal.

The documentation for this class was generated from the following file:

- vhdl/io_ctrl_rtl.vhd

3.3 sim Architecture Reference

IO Control Unit Testbench Architecture.

Processes

- p_clk( )
- run( )

Libraries

- IEEE

Use Clauses

- std_logic_1164

Components

- io_ctrl

Signals

- clk_i **std_logic**
- reset_i **std_logic**
- dig0_i **std_logic_vector(7 downto 0)**
- dig1_i **std_logic_vector(7 downto 0)**
- dig2_i **std_logic_vector(7 downto 0)**
- dig3_i **std_logic_vector(7 downto 0)**
- led_i **std_logic_vector(15 downto 0)**
- sw_i **std_logic_vector(15 downto 0)**
- pb_i **std_logic_vector(15 downto 0)**
- ss_o **std_logic_vector(7 downto 0)**
- ss_sel_o **std_logic_vector(3 downto 0)**
- swsync_o **std_logic_vector(15 downto 0)**
- pbsync_o **std_logic_vector(3 downto 0)**

3.3.1 Detailed Description

IO Control Unit Testbench Architecture.

The IO Control uniti part of the calculator project.

The documentation for this class was generated from the following file:

- tb/tb_io_ctrl_sim.vhd

Chapter 4

File Documentation

4.1 tb/tb_io_ctrl_.vhd File Reference

IO Control Unit Testbench Entity.

Entities

- io_ctrl entity
  IO Control Unit Testbench Entity.

4.1.1 Detailed Description

IO Control Unit Testbench Entity.

4.2 tb/tb_io_ctrl_cfg.vhd File Reference

IO Control Unit Testbench Configuration.

Configurations

- tb_io_ctrl_cfg **tb_io_ctrl**

4.2.1 Detailed Description

IO Control Unit Testbench Configuration.

4.3 tb/tb_io_ctrl_sim.vhd File Reference

IO Control Unit Testbench Architecture.

Entities

- sim architecture
  IO Control Unit Testbench Architecture.

4.3.1 Detailed Description

IO Control Unit Testbench Architecture.

4.4 vhdl/io_ctrl_.vhd File Reference

IO Control Unit Entity.

Entities

- io_ctrl entity
  IO Control Unit Testbench Entity.

4.4.1 Detailed Description

IO Control Unit Entity.

4.5 vhdl/io_ctrl_cfg.vhd File Reference

IO Control Unit Configuration.

Configurations

- io_ctrl_rtl_cfg **io_ctrl**

4.5.1 Detailed Description

IO Control Unit Configuration.

4.6 vhdl/io_ctrl_rtl.vhd File Reference

IO Control Unit Architecture.

Entities

- rtl architecture
  IO Control Unit Architecture.

4.6.1 Detailed Description

IO Control Unit Architecture.