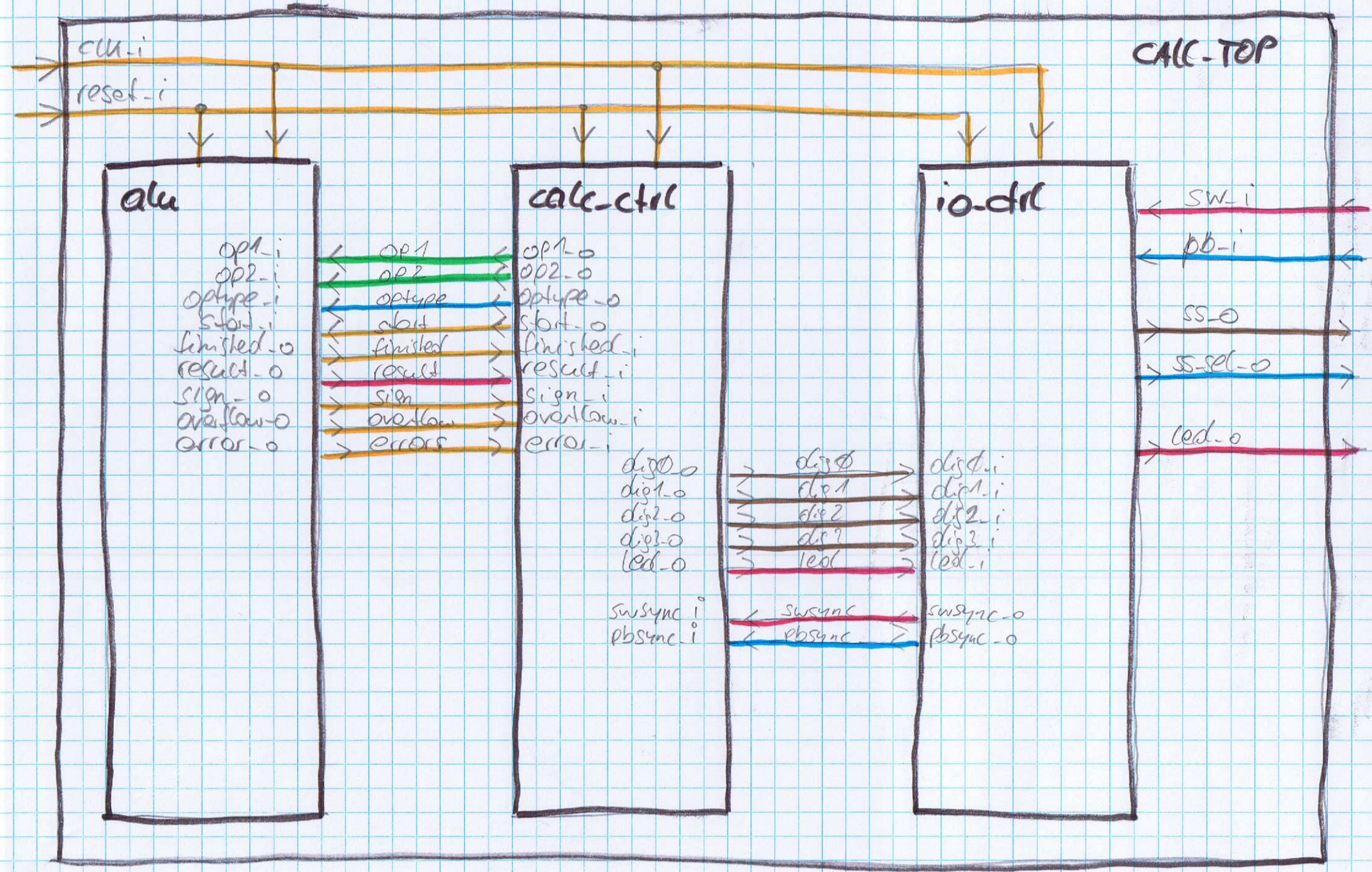
12bit 1bit 8bit
4bit 16bit



```
--------------------------------------------------------------------------------
-- FHTW - BEL3 - DSD - calculator project
--
-- Author:  Helmut Resch
--          el16b005 BEL3 no. 15 in attendance list
--          User interface Type "A", square root, logdual, or, ror
--
-- File:    calc_top_rtl.vhd
--
-- Version history:
--
-- v_0.1    14.11.2017  IO Ctrl + Testbench
-- v_0.2    15.11.2017  Calc Ctrl + Testbench
-- v_0.3    16.11.2017  ALU + Testbench
-- v_0.4    17.11.2017  Top Level Design + Testbench
-- v_0.5    20.11.2017  Synthesis + Implementation
--                      Solve XILINX warnings
-- v_0.6    21.11.2017  Synthesis and check calculations
--                      Solve error square root
-- v_1.0    24.11.2017  Final Specification check and Documentation
--
-- Design Unit: Calculator Top Design
--              Architecture RTL-STRUC
--
-- Description: The IO Control unit is part of the calculator project.
--              The Calculator Top Design links the io_ctrl, calc_ctrl and ALU
--              with internal signals and portmapping
--------------------------------------------------------------------------------

--! @file calc_top_rtl.vhd
--! @brief Calculator Top Architecture RTL-STRUC

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;

--! @brief Calculator Top Architecture RTL-STRUC
--! @details The Calulator Control unit is part of the calculator project.

architecture struc of calc_top is

component io_ctrl

  port
  (
    clk_i : in std_logic;
    reset_i : in std_logic;
    dig0_i : in std_logic_vector(7 downto 0);
    dig1_i : in std_logic_vector(7 downto 0);
    dig2_i : in std_logic_vector(7 downto 0);
    dig3_i : in std_logic_vector(7 downto 0);
    led_i : in std_logic_vector(15 downto 0);
    sw_i : in std_logic_vector(15 downto 0);
    pb_i : in std_logic_vector(3 downto 0);
    ss_o : out std_logic_vector(7 downto 0);
    ss_sel_o : out std_logic_vector(3 downto 0);
    led_o : out std_logic_vector(15 downto 0);
    swsync_o : out std_logic_vector(15 downto 0);
    pbsync_o : out std_logic_vector(3 downto 0)
  );

end component;

component calc_ctrl

  port
```



```
  (
    clk_i : in std_logic;
    reset_i : in std_logic;
    swsync_i : in std_logic_vector (15 downto 0);
    pbsync_i : in std_logic_vector(3 downto 0);
    finished_i : in std_logic;
    result_i : in std_logic_vector(15 downto 0);
    sign_i : in std_logic;
    overflow_i : in std_logic;
    error_i : in std_logic;
    dig0_o : out std_logic_vector(7 downto 0);
    dig1_o : out std_logic_vector(7 downto 0);
    dig2_o : out std_logic_vector(7 downto 0);
    dig3_o : out std_logic_vector(7 downto 0);
    led_o : out std_logic_vector(15 downto 0);
    op1_o : out std_logic_vector(11 downto 0);
    op2_o : out std_logic_vector(11 downto 0);
    optype_o : out std_logic_vector(3 downto 0);
    start_o : out std_logic
  );

end component;

component alu

  port
  (
    clk_i : in std_logic;
    reset_i : in std_logic;
    op1_i : in std_logic_vector(11 downto 0);
    op2_i : in std_logic_vector(11 downto 0);
    optype_i : in std_logic_vector(3 downto 0);
    start_i : in std_logic;
    finished_o : out std_logic;
    result_o : out std_logic_vector(15 downto 0);
    sign_o : out std_logic;
    overflow_o : out std_logic;
    error_o : out std_logic
  );

end component;


signal dig0 : std_logic_vector(7 downto 0);
signal dig1 : std_logic_vector(7 downto 0);
signal dig2 : std_logic_vector(7 downto 0);
signal dig3 : std_logic_vector(7 downto 0);
signal led : std_logic_vector(15 downto 0);
signal swsync : std_logic_vector(15 downto 0);
signal pbsync : std_logic_vector(3 downto 0);
signal finished : std_logic;
signal result : std_logic_vector(15 downto 0);
signal sign : std_logic;
signal overflow : std_logic;
signal errors : std_logic;
signal op1 : std_logic_vector(11 downto 0);
signal op2 : std_logic_vector(11 downto 0);
signal optype : std_logic_vector(3 downto 0);
signal start : std_logic;

begin

  i_io_ctrl : io_ctrl

  port map
  (
```

```
    clk_i => clk_i,
    reset_i => reset_i,
    dig0_i => dig0,
    dig1_i => dig1,
    dig2_i => dig2,
    dig3_i => dig3,
    led_i => led,
    sw_i => sw_i,
    pb_i => pb_i,
    ss_o => ss_o,
    led_o => led_o,
    ss_sel_o => ss_sel_o,
    swsync_o => swsync,
    pbsync_o => pbsync
  );

  i_calc_ctrl : calc_ctrl

  port map
  (
    clk_i => clk_i,
    reset_i => reset_i,
    swsync_i => swsync,
    pbsync_i => pbsync,
    finished_i => finished,
    result_i => result,
    sign_i => sign,
    overflow_i => overflow,
    error_i => errors,
    dig0_o => dig0,
    dig1_o => dig1,
    dig2_o => dig2,
    dig3_o => dig3,
    led_o => led,
    op1_o => op1,
    op2_o => op2,
    optype_o => optype,
    start_o => start
  );

  i_alu : alu

  port map
  (
    clk_i => clk_i,
    reset_i => reset_i,
    finished_o => finished,
    result_o => result,
    sign_o => sign,
    overflow_o => overflow,
    error_o => errors,
    op1_i => op1,
    op2_i => op2,
    optype_i => optype,
    start_i => start
  );

end struc;
```

```
msim
├── 11_compile.do
├── 12_sim.do
├── 21_compile.do
├── 22_sim.do
├── 31_compile.do
├── 32_sim.do
├── 41_compile.do
├── 42_sim.do
├── alu_wave.do
├── calc_ctrl_wave.do
├── calc_top_wave.do
├── io_ctrl_wave.do
├── transcript
├── vsim.wlf
└── work
    ├── _info
    ├── _info_conflict-20171115-214529
    ├── _lib1_193.qdb
    ├── _lib1_193.qpg
    ├── _lib1_193.qtl
    ├── _lib.qdb
    └── _vmake

1 directory, 21 files
```

IO_CTRL
CALC_CTRL
ALU
CALC_TOP

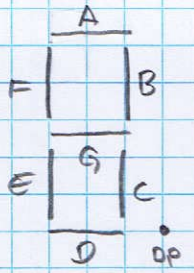
```
vhdl
├── alu_rtl.vhd
├── alu_.vhd
├── calc_ctrl_rtl.vhd
├── calc_ctrl_.vhd
├── calc_top_rtl.vhd
├── calc_top_.vhd
├── io_ctrl_rtl.vhd
├── io_ctrl_.vhd
├── IO-planning.xlsx
├── schematic.pdf
├── WARNINGS_implementation.xls
└── WARNINGS_synthesis.xlsx

0 directories, 12 files
```

```
tb
├── tb_alu_sim.vhd
├── tb_alu_.vhd
├── tb_calc_ctrl_sim.vhd
├── tb_calc_ctrl_.vhd
├── tb_calc_top_sim.vhd
├── tb_calc_top_.vhd
├── tb_io_ctrl_sim.vhd
└── tb_io_ctrl_.vhd

0 directories, 8 files
```

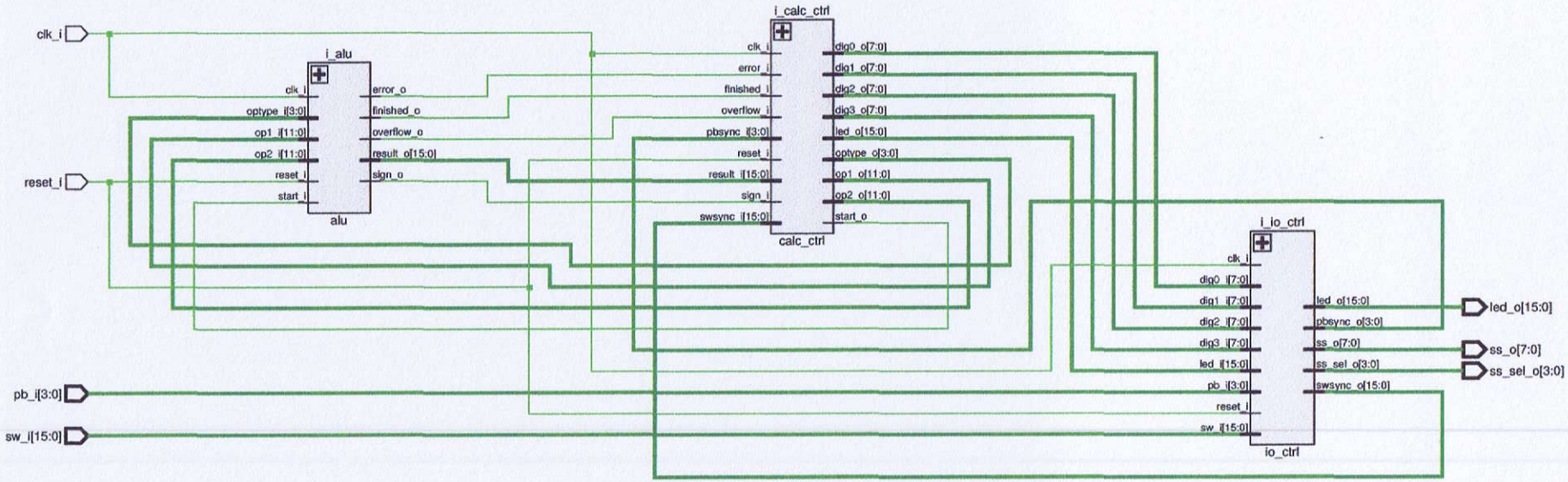
0000	0000	0	0
	0001	1	1
	0010	2	2
	0011	3	3
	0100	4	4
	0101	5	5
	0110	6	6
	0111	7	7
	1000	8	8
	1001	9	9
	1010	10	A
	1011	11	B
	1100	12	C
	1101	13	D
	1110	14	E
	1111	15	F



Ø = active

	A	B	C	D	E	F	G	DP
Ø	0	0	0	0	0	0	1	1
1	1	0	0	1	1	1	1	1
2	0	0	1	0	0	1	0	1
3	0	0	0	0	1	1	0	1
4	1	0	0	1	1	0	0	1
5	0	1	0	0	1	0	0	1
6	0	1	0	0	0	0	0	1
7	0	0	0	1	1	1	1	1
8	0	0	0	0	0	0	0	1
9	0	0	0	1	1	0	0	1
A	0	0	0	1	0	0	0	1
b	1	1	0	0	0	0	0	1
c	1	1	1	0	0	1	0	1
d	1	0	0	0	0	1	0	1
E	0	1	1	0	0	0	0	1
F	0	1	1	1	0	0	0	1
L.	1	0	0	1	1	1	1	0
2.	0	0	1	0	0	1	0	0
0.	1	1	0	0	0	1	0	0
-	1	1	1	1	1	1	0	1
O	1	1	0	0	0	1	0	1
E	0	1	1	0	0	0	0	1
n	1	1	1	1	1	0	1	0
S	0	1	0	0	1	0	0	1
L	1	1	1	0	0	0	1	1

OPTYPE 15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	HEX	DEC	REMARK
X X X X	1 0 1 0	1 0 1 0	1 0 1 0	AAA	2730	OP1
X X X X	0 1 0 1	0 1 0 1	0 1 0 1	555	1365	OP2 (Only)
0 1 1 0	X X X X	X X X X	X X X X	SRO ✓		OPTYPE
0 0 0 0	0 0 0 0	0 0 1 1	0 1 0 0	34	52	RESULT ✓
0 1 1 1	X X X X	X X X X	X X X X	LOG_2 ✓		OPTYPE
0 0 0 0	0 0 0 0	0 0 0 0	1 0 1 1	B	11	RESULT ✓
1 0 1 0	X X X X	X X X X	X X X X	OR		OPTYPE
0 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1	FFF	4095	RESULT ✓
1 1 0 1	X X X X	X X X X	X X X X	ROR		OPTYPE
0 0 0 0	0 1 0 1	0 1 0 1	0 1 0 1	555	1365	RESULT ✓
X X X X	1 1 0 0	1 1 1 0	1 1 0 1	CE0	3309	OP1
X X X X	X X X X	X X X X	X X X X			OP2
0 1 1 0	X X X X	X X X X	X X X X	SRO		OPTYPE
				39	57	RESULT ✓
X X X X	0 0 0 0	0 0 0 0	0 0 0 0	000	0	OP1
X X X X	X X X X	X X X X	X X X X			OP2
0 1 1 1	X X X X	X X X X	X X X X			OPTYPE
				ERROR		RESULT ✓
X X X X	X X X X	X X X X	X X X X			
X X X X	X X X X	X X X X	X X X X			
0 1 0 0	X X X X	X X X X	X X X X			
				ERROR		RESULT ✓
X X X X	0 0 1 0	0 0 1 1	0 0 1 0	266	614	OP1
X X X X	1 0 0 1	1 1 1 0	0 1 1 0	9EE	2508	OP2
1 0 1 0	X X X X	X X X X	X X X X	OR		OPTYPE
0 0 0 0	1 0 1 1	1 1 1 1	1 0 1 1	BEE	3059	RESULT ✓
X X X X	0 0 1 0	0 0 1 1	0 0 1 0	266	614	OP1
X X X X	X X X X	X X X X	X X X X			OP2
1 1 0 1	X X X X	X X X X	X X X X	ROR		OPTYPE
0 0 0 0	0 0 0 0	1 0 0 1	1 0 0 1	133	207	RESULT ✓


clk_i
reset_i
pb_i[3:0]
sw_i[15:0]
i_alu
clk_i
optype_i[3:0]
op1_i[11:0]
op2_i[11:0]
reset_i
start_i
error_o
finished_o
overflow_o
result_o[15:0]
sign_o
alu
i_calc_ctrl
clk_i
error_i
finished_i
overflow_i
pbsync_i[3:0]
reset_i
result_i[15:0]
sign_i
swsync_i[15:0]
dig0_o[7:0]
dig1_o[7:0]
dig2_o[7:0]
dig3_o[7:0]
led_o[15:0]
optype_o[3:0]
op1_o[11:0]
op2_o[11:0]
start_o
calc_ctrl
i_io_ctrl
clk_i
dig0_i[7:0]
dig1_i[7:0]
dig2_i[7:0]
dig3_i[7:0]
led_i[15:0]
pb_i[3:0]
reset_i
sw_i[15:0]
led_o[15:0]
pbsync_o[3:0]
ss_o[7:0]
ss_sel_o[3:0]
swsync_o[15:0]
io_ctrl
led_o[15:0]
ss_o[7:0]
ss_sel_o[3:0]

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco
All ports (50)							
led_o (16)	OUT			true	(Multiple)	LVCMOS33	3,30
led_o[15]	OUT		L1	true	35	LVCMOS33	3,30
led_o[14]	OUT		P1	true	35	LVCMOS33	3,30
led_o[13]	OUT		N3	true	35	LVCMOS33	3,30
led_o[12]	OUT		P3	true	35	LVCMOS33	3,30
led_o[11]	OUT		U3	true	34	LVCMOS33	3,30
led_o[10]	OUT		W3	true	34	LVCMOS33	3,30
led_o[9]	OUT		V3	true	34	LVCMOS33	3,30
led_o[8]	OUT		V13	true	14	LVCMOS33	3,30
led_o[7]	OUT		V14	true	14	LVCMOS33	3,30
led_o[6]	OUT		U14	true	14	LVCMOS33	3,30
led_o[5]	OUT		U15	true	14	LVCMOS33	3,30
led_o[4]	OUT		W18	true	14	LVCMOS33	3,30
led_o[3]	OUT		V19	true	14	LVCMOS33	3,30
led_o[2]	OUT		U19	true	14	LVCMOS33	3,30
led_o[1]	OUT		E19	true	14	LVCMOS33	3,30
led_o[0]	OUT		U16	true	14	LVCMOS33	3,30
pb_i (4)	IN			true	14	LVCMOS33	3,30
pb_i[3]	IN		W19	true	14	LVCMOS33	3,30
pb_i[2]	IN		U18	true	14	LVCMOS33	3,30
pb_i[1]	IN		T17	true	14	LVCMOS33	3,30
pb_i[0]	IN		U17	true	14	LVCMOS33	3,30
ss_o (8)	OUT			true	34	LVCMOS33	3,30
ss_o[7]	OUT		W7	true	34	LVCMOS33	3,30
ss_o[6]	OUT		W6	true	34	LVCMOS33	3,30
ss_o[5]	OUT		U8	true	34	LVCMOS33	3,30
ss_o[4]	OUT		V8	true	34	LVCMOS33	3,30
ss_o[3]	OUT		U5	true	34	LVCMOS33	3,30
ss_o[2]	OUT		V5	true	34	LVCMOS33	3,30
ss_o[1]	OUT		U7	true	34	LVCMOS33	3,30
ss_o[0]	OUT		V7	true	34	LVCMOS33	3,30
ss_sel_o (4)	OUT			true	34	LVCMOS33	3,30
ss_sel_o[3]	OUT		W4	true	34	LVCMOS33	3,30
ss_sel_o[2]	OUT		V4	true	34	LVCMOS33	3,30
ss_sel_o[1]	OUT		U4	true	34	LVCMOS33	3,30
ss_sel_o[0]	OUT		U2	true	34	LVCMOS33	3,30
sw_i (16)	IN			true	(Multiple)	LVCMOS33	3,30
sw_i[15]	IN		R2	true	34	LVCMOS33	3,30
sw_i[14]	IN		T1	true	34	LVCMOS33	3,30
sw_i[13]	IN		U1	true	34	LVCMOS33	3,30
sw_i[12]	IN		W2	true	34	LVCMOS33	3,30
sw_i[11]	IN		R3	true	34	LVCMOS33	3,30
sw_i[10]	IN		T2	true	34	LVCMOS33	3,30
sw_i[9]	IN		T3	true	34	LVCMOS33	3,30
sw_i[8]	IN		V2	true	34	LVCMOS33	3,30
sw_i[7]	IN		W13	true	14	LVCMOS33	3,30
sw_i[6]	IN		W14	true	14	LVCMOS33	3,30
sw_i[5]	IN		V15	true	14	LVCMOS33	3,30
sw_i[4]	IN		W15	true	14	LVCMOS33	3,30
sw_i[3]	IN		W17	true	14	LVCMOS33	3,30
sw_i[2]	IN		W16	true	14	LVCMOS33	3,30
sw_i[1]	IN		V16	true	14	LVCMOS33	3,30
sw_i[0]	IN		V17	true	14	LVCMOS33	3,30
Scalar ports (2)							
clk_i	IN		W5	true	34	LVCMOS33	3,30
reset_i	IN		T18	true	14	LVCMOS33	3,30

Vivado Warnings

Name	Severity	Details
Synthesis		
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[14]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[13]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[12]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[11]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[10]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[9]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[8]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[7]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[6]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[5]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[4]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[3]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[2]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[1]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/led_o_reg[0]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_alu/workNumber2_s_reg[15]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_alu/workNumber2_s_reg[14]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_alu/workNumber2_s_reg[13]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_alu/workNumber2_s_reg[12]) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_alu/overflow_o_reg) is unused and will be removed from module calc_top.
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/dig2_o_reg[0]) is unused and will be removed from module calc_top. *
Synth 8-3332	Warning	Sequential element (i_calc_ctrl/dig1_o_reg[0]) is unused and will be removed from module calc_top. *

16 not used LED

first 4 bit of 16 bit never used

no overflow possible for sro, lb, or, ror

*

7	6	5	4	3	2	1	0	
1	0	0	1	1	1	1	0	1.
0	0	1	0	0	1	0	0	2.
1	1	0	0	0	1	0	0	0.
-	-	-	-	-	-	-	x	→ dig 1_0/0 never used

0	0	0	0	0	0	1	1	0
0	1	1	0	0	0	0	1	E
0	1	0	0	1	0	0	1	S
1	1	1	0	0	0	1	1	L
1	1	0	0	0	1	0	1	o
1	1	1	1	0	1	0	1	r
-	-	-	-	-	-	-	x	→ dig2_0/0 never used

Σ 22 warnings with reason !