1) Explain what SRAM and DRAM are, how they compare in terms of performance, and what each is used for?

SRAM is cache memory and DRAM is main memory. SRAM is very fast and more expensive that Dram but has a smaller capacity and is higher in the memory hierarchy. Dram is fast and has medium size carrying capacity.

2) How does the Translation Lookaside Buffer (TLB) work with the Page Table to identify and locate a program's memory pages?

The TLB contains page table entries that have been most recently used. The processor looks though this TLB buffer entries with a virtual address if it finds it in the entries it is a hit and becomes a real address. If it is not a hit it checks if the page is already in main memory, then the TLB will update this new page entry.

3a) Explain the operation of the MUX units, and state whether they are combinational or sequential logic elements.

MUX units are combinational because depending on weather the instruction it will give a different output from the mux. In the pipeline data path, the mux will produce a 1 or zero depending on the instruction and send it on that path corresponding with that one or zero. An example of this is the difference between the add instruction and division instruction the MUX determines weather the pipeline will good into the ALU which is need for addition or go into the sign extended which is needed for division instruction. So, the result of the MUX is completely dependent on the Instruction type.

3b) What are the Exception Status Register (ESR) and Exception Link Register (ELR) used for? Which stage of the pipeline do they operate in?

The ESR saves the indication of the problem. The ERL saves the program counter of the offending or interrupted instructions. The stage of the pipeline they operate it is the ID/EX part of the pipeline.

3c) Explain the purpose of the Forwarding Unit and its associated circuitry, in the function of the pipeline.

The Forwarding Unit purpose is to stop some hazards that come up when you are trying to use the same two registers one right after the other. There is a hazard for example if you are adding to registers together then using the written register in the next instruction. How it works is it does not write it register for that instruction instead it forwards the value to the next instruction.

3d) Why does the combinational control logic in the pipeline determine the maximum possible clock rate?

The combination control logic determines the maximum clock rate because those logic units are the circuits that take time to the computations and is what is taking the time to preform the instruction in the pipeline each part has a maximum clock rate for each piece.

4a) How many address bits are required to address one byte within a line?

Log_2(128 bytes) = 7 bits = 2 ^ 7

4b) How many lines are in this cache?

256 KiB / 128-byte lines = 2Ki

4c) If the cache is 8-way set-associative, how many sets are there within the cache?

2Ki = 1024 * 2 = 2048

2048 / 8 = 256 sets

4d) If the cache is direct-mapped, how many address bits are required to select one of the lines?

Log_2(2Ki) = log_2(2) + log_2(1024) = 1 + $log_2$1024) = 11 bits are required

4e) If the cache is 8-way set-associative, how many address bits are required to select one of the lines *within* a set?

Log_2(8) = 3 bits are required