Special support required for this project would consist of access to CHERI-enabled hardware for one or both of the RISC-V and ARM ISAs so that benchmarks can be run. This could be provided through either physical board copies or SSH login. The Terasic DE4 FPGA Board developed by Cambridge to implement and test CHERI-RISC-V would be my first choice, although a SiFive HiFive Unleashed board along with FPGA extensions could also be used. The ARM Morello board has CHERI extensions and is primarily used for research and development of the possible security benefits of CHERI on ARM. Since it is available to be purchased by universities for research purposes, it is also an ideal candidate to provide CHERI-enabled hardware.