CprE 381 Homework 10

[Note: The homework below focuses on the details of caching and cache design. Once you have completed this homework you should be able to motivate the need for caches using specific program examples. You should also be able to configure and hand-simulate a range of caches.]

1. Cache Configuration and Simulation

   In this problem we will consider several cache designs for a processor implementing the MIPS ISA *[Note that this has implications needed to answer the below questions].* Assume that the block offset is four bits and the index is four bits.

   a. What is the cache block size in bytes? words? double words?
   b. How many sets does this cache have? *[Hint: note that both direct-mapped and fully-associative caches can be considered to have sets.]*
   c. Record both the amount of data and meta-data (in bits) this cache holds if it is direct-mapped, two-way set associative, and four-way set associative.
   d. Simulate the direct-mapped and four-way set associative cache with respect to the following series of memory accesses. In the table below, indicate whether each memory access was a hit or a miss and provide the reason for each miss. Assume the caches have no valid entries to begin with and use a least-recently-used (LRU) replacement policy.

Memory Access	Direct-Mapped	4-way Set Associative
0x1001FEA0		
0x1001EFA4		
0x1001FEA8		
0x100100A0		
0x100100B0		
0x100100C0		
0x10011FA1		
0x1001EEA2		
0x1001EFAF		
0x100100A2		

   Write the valid entries in the final state of each cache using the format <set#, way#, tag>. What was the hit rate of each cache?

2. Cache Write Nuances
   a. ZyBooks (Textbook) 5.19.6 all (a-c)
   b. ZyBooks (Textbook) 5.19.7 all (a-b)

3. Cache Hierarchy Performance
   a. ZyBooks (Textbook) 5.19.10 all (a-g)