

# IRF830

## Power Field Effect Transistor

### N-Channel Enhancement Mode Silicon Gate TMOS

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low  $R_{DS(on)}$  to Minimize On-Losses, Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use with Inductive Loads

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	500	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	500	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 20$	Vdc
Drain Current	$I_D$		Adc
Continuous, $T_C = 25^\circ\text{C}$		4.5	
$T_C = 100^\circ\text{C}$		3.0	
Peak, $T_C = 25^\circ\text{C}$		18	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	75 0.6	Watts W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

Thermal Resistance			$^\circ\text{C/W}$
— Junction-to-Case	$R_{\theta JC}$	1.67	
— Junction-to-Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	$T_L$	300	$^\circ\text{C}$



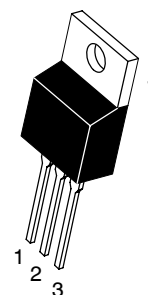
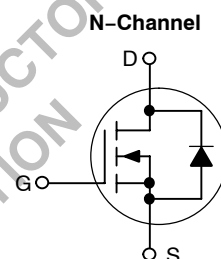
ON Semiconductor

<http://onsemi.com>

#### TMOS POWER FET

##### 4.5 AMPERES, 500 VOLTS

$R_{DS(on)} = 1.5 \Omega$



TO-220AB  
CASE 221A  
STYLE 5

#### PIN ASSIGNMENT

	PIN ASSIGNMENT
1	Gate
2	Drain
3	Source
4	Drain

#### ORDERING INFORMATION

Device	Package	Shipping
IRF830	TO-220AB	50 Units/Rail

See the MTM4N45 Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTP4N45 are applicable for this product.

# IRF830

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 0.25 mAdc)	V <sub>(BR)DSS</sub>	500	—	Vdc
Zero Gate Voltage Drain Current (V <sub>DS</sub> = Rated V <sub>DSS</sub> , V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 0.8 Rated V <sub>DSS</sub> , V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	— —	0.2 1.0	mAdc
Gate-Body Leakage Current, Forward (V <sub>GSF</sub> = 20 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS(f)</sub>	—	100	nAdc
Gate-Body Leakage Current, Reverse (V <sub>GSR</sub> = 20 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS(r)</sub>	—	100	nAdc

### ON CHARACTERISTICS (1)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 0.25 mA)	V <sub>GS(th)</sub>	2.0	4.0	Vdc
Static Drain-to-Source On-Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 2.5 Adc)	R <sub>DS(on)</sub>	—	1.5	Ohm
On-State Drain Current (V <sub>GS</sub> = 10 V) (V <sub>DS</sub> ≥ 6.75 Vdc)	I <sub>D(on)</sub>	4.5	—	Adc
Forward Transconductance (V <sub>DS</sub> ≥ 6.75 Vdc, I <sub>D</sub> = 2.5 Adc)	g <sub>FS</sub>	2.5	—	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	—	800	pF
Output Capacitance		C <sub>oss</sub>	—	200	
Reverse Transfer Capacitance		C <sub>rss</sub>	—	60	

### SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	(V <sub>DD</sub> = 200 Vdc, I <sub>D</sub> = 2.5 Apk, R <sub>G</sub> = 15 Ω)	t <sub>d(on)</sub>	—	30	ns
Rise Time		t <sub>r</sub>	—	30	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	55	
Fall Time		t <sub>f</sub>	—	30	
Total Gate Charge	(V <sub>DS</sub> = 0.8 Rated V <sub>DSS</sub> , V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = Rated I <sub>D</sub> )	Q <sub>g</sub>	22 (Typ)	30	nC
Gate-Source Charge		Q <sub>gs</sub>	12 (Typ)	—	
Gate-Drain Charge		Q <sub>gd</sub>	10 (Typ)	—	

### SOURCE-DrAIN DIODE CHARACTERISTICS (1)

Forward On-Voltage	(I <sub>S</sub> = Rated I <sub>D</sub> , V <sub>GS</sub> = 0)	V <sub>SD</sub>	1.1 (Typ)	1.6	Vdc
Forward Turn-On Time		t <sub>on</sub>	Limited by stray inductance		
Reverse Recovery Time		t <sub>rr</sub>	450 (Typ)	—	ns

### INTERNAL PACKAGE INDUCTANCE

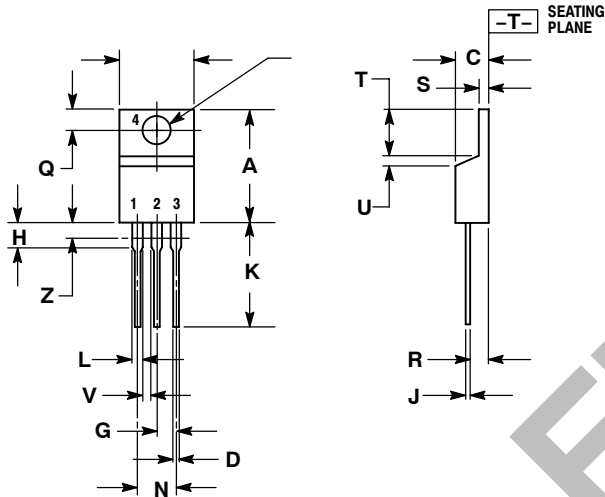
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L <sub>D</sub>	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L <sub>S</sub>	7.5 (Typ)	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

# IRF830

## PACKAGE DIMENSIONS

### TO-220AB CASE 221A-09 ISSUE Z



#### NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

#### STYLE 5:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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