A Study on Thermal Property of TQFP-100L Package via DOE Method

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Abstract

Though Thin-Quad-Flat-Package (TQFP) was developed for years, it is now widely adapted for packaging IC products. For broadening its application to IC product, detail evaluation of the thermal property that is strongly depending on the package structure and the involved materials is necessary. For facilitating product design, this study employs an economic statistical method, DOE, to study the effect of lead frame design, encapsulation compound and mechanical dimensions to the thermal resistance of the package via results from the CAE modeling and the verification experiments. In addition, the influence of application, such as PCB substrate and environment, is included in the analysis as taking customer requirement into consideration.

The results show that the extrinsic parameters during application as, PCB layout and structure, plays the most important roles in the package thermal handling capability which might overrides the contribution from package design. Intrinsically, the results indicate that larger die pad gives better thermal conduction for same package outline. The composition of epoxy molding compound as filler type, volume fraction, ... etc., controls the heat dissipation behavior of the package. It becomes more significant as package thickness increasing. The experimental data have good matching to the results from the CAE simulation model.

Introduction

The power consumption of IC devices increases due to higher integration density and faster operation speed these years. It obviously results in higher chip junction temperature that might degrade reliability performance or even causes catastrophic damage to the device as the extra heat not handling properly. In the case, some thermal management techniques have been developed to improve the package performance in this aspect. These techniques are either reducing the thermal resistance between chip and package surface to facilitate the heat dissipation via package surface or decreasing the thermal resistance between chip and leads allowing more heat conducting to printed circuit board (PCB). For instance, high thermal conductive epoxy molding compound (EMC) and large die pad can help to decrease the thermal resistance.

Although the PCB thermal conductivity doesn¡t affect the internal thermal resistance of packages, it can be considered as a heat sink attached to the package leads. The multi-layer PCB can rapidly carry away heat from package leads to full PCB domain that effectively decreases chip junction temperature. Therefore, the leadframe structure seriously affects the heat flow from chip to PCB. Large die-pad size, small slit between inner leads and die pad, large leadframe area and wide package leads all help heat dissipation from chip to the ambient.

In this paper, the DOE method is employed to find the optimal factors and the parameters of TQFP-100L package taking the junction-to-ambient thermal resistance as the response. EMC, leadframe, and package thickness are the control factors involved in the L_4 experimental setup. The effort is also trying to match the outputs from CAE analytical tool to those from experiments via the factorial analysis method. The CAE modeling technique and thermal resistance measurement of the QFP package is referred to the works by D. Edwards [1] and Tanaka et al. [2].

Measurement Technique

Thermal resistance of an IC package characterizes its heat dissipation capability, i.e., to carry the heat generated inside IC chip to the ambient. The formula is as follows:

$$R_{ja} = \frac{T_j - T_a}{P_H}$$

where

R_{ja}: junction-to-ambient thermal resistance, °C/W
T_j: junction temperature, °C
T_a: ambient temperature, °C
P_H: dissipated power, W

Measurement of junction temperature is carried out on the package with thermal test die. The test device consists of a diffused resistor covering 85% of the device area for heat generating and a bipolar diode as the junction temperature sensor. As illustrated in Fig. 1, the diode exhibits a linear relation between forward voltage and temperature when a constant current acts through the device. Each diode must be calibrated prior to thermal test by immersing the device into a temperature controlled oil bath.

The test package is placed in a 1 ft^3 box under natural convection test and powered on for about 20 minutes to reach environmental stability. The measurement method and environment setup follow JEDEC standards [3-5]. A T-type thermal couple is used to measure the ambient temperature under power on state.

The package is mounted on a 4 x 4 x 1.57 mm, 2- and 4-layer PCB made of FR4 material. The thickness of top and bottom trace layers of PCB starts with 1 oz. copper material and finally is plated to 2 oz. during via-hole plating process. The configuration of PCB follows the specification defined in JC15.1 [6].

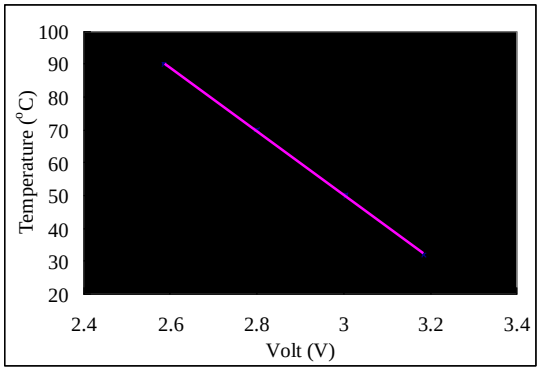

Fig. 1. The relationship of output voltage vs. temperature of the diode within test die.

Modeling Technique

The ANSYS software is employed as the simulation tool for the TQFP-100L thermal analysis. A one forth model with 3-D thermal solid element is built for its symmetric configuration assuming all interfaces perfect, each element defined by eight nodes with one degree of freedom. Fig. 2 shows the meshing configuration and the internal structure of TQFP-100L without molding compound. The symmetric plane is assumed adiabatic and the material is homogeneous and isotropic. Thermal conductivity of the employed PCB is considered as orthotropic.

The ambient temperature is set at 25°C. For natural convection, the heat transfer coefficient as suggested by Ellison [7] is based on the following equation:

$$h_c = 0.83f\left(\frac{\Delta T}{L_{ch}}\right)$$

where

h_c: heat transfer coefficient, W/m^2K

ΔT: the temperature difference, °C
L_{ch}: the characteristic length, m
L_{ch} = WL/2(W+L) for horizontal plate
L_{ch} = H for vertical plate

where, L: the plate length; W: plate width; and H: plate height

f = 1.00 and n = 0.35 for horizontal plate facing upward
f = 0.50 and n = 0.33 for horizontal plate facing downward
f = 1.22 and n = 0.35 for vertical plate

In natural convection, radiation must be taken into consideration and applied to all external surfaces except the symmetric surfaces. The emissivity of FR-4 and EMC is taken as 0.9 here and the formula is as follows:

$$q = \varepsilon\sigma A(T^4 - T_a^4)$$

where

q: heat flow rate, W
T_a: ambient temperature, °C

£ : Stefan-Boltzmann constant, W/m^{2}ϒK^4

£ : surface emissivity

A: surface area, m^2

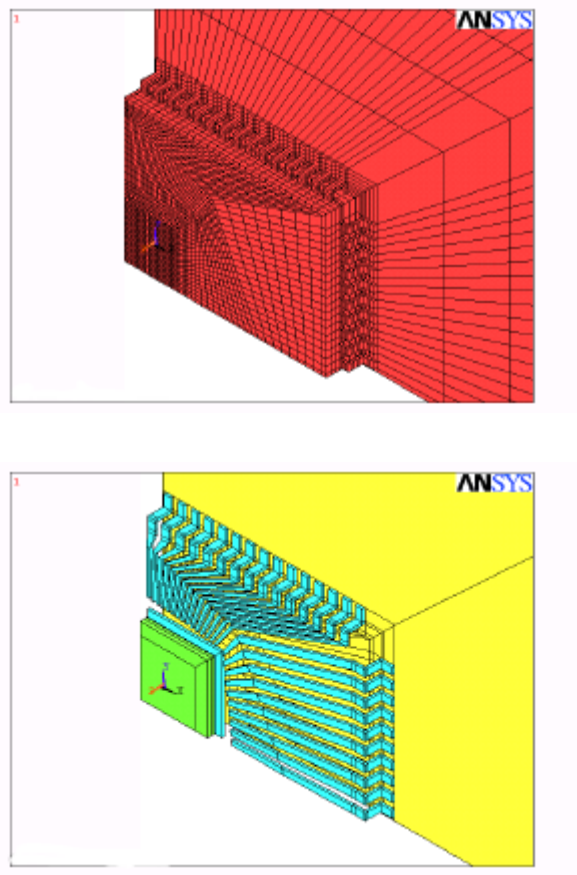

Fig. 2. TQFP model; outline (upper) and internal structure (lower).

Package Information

The mechanical structure of TQFP package is illustrated in Fig. 3. Copper leadframe is employed in the CAE analysis and package preparation. The mechanical dimensions of the packages are listed in Table 1. The die pad size and the package thickness are the two varying factors during evaluation.

Material properties have been summarized in Table 2. Two molding compounds are chosen to evaluate the effect of compound conductivity on the thermal issue.

Table 1. Mechanical dimensions of TQFP package

Package type	TQFP-100L
1. Die pad size	8 ϒ 8 mm^2 or 7 ϒ 7 mm^2
2. Package size	14 ϒ 20 ϒ 1.4 mm^3 or 14 ϒ 20 ϒ 1.0 mm^3
3. Die size	6.35 ϒ 6.35 ϒ 0.31 mm^3
4. Lead-Frame thickness	0.127 mm
5. PCB size	101.6 ϒ 114.3 ϒ 1.57 mm^3
6. Epoxy thickness	0.025 mm

Table 2. Packaging material property

Material	Composition	Thermal conductivity coefficient(W/mϒK)
Chip	Si	148.0
Leadframe	Copper alloy	168.0
EMC	CEL-9200XU EMC-6300HJ	1.00 0.67
Die Attach	Ag epoxy	5.0
PCB	FR4 (4 layers) FR4 (2 layers)	K_{xy} = 17.0, K_z = 0.3 K_{xy} = 1.60, K_z = 0.3

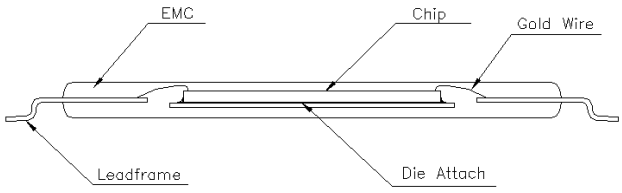

Fig. 3 Cross-section diagram of TQFP

Result and Discussion

The DOE method is used to evaluate contribution of each factor and to determine the optimal setting for lowering the junction-to-ambient thermal resistance of TQFP package under 1 Watt rated power.

A. Results from DOE methods

The factors and levels taken for the DOE analysis have been listed in Table 3. A L_4 orthogonal array has been constructed with the package thermal resistance, R_{ja}, as the response. The quality characteristics for R_{ja} is the smaller the better.

To verify the CAE capability and the accuracy of the experimentation from packages on 4-layer PCB test board, data from both sources are put into the analysis for comparison. Table 4 gives the orthogonal array and results from CAE analysis. The optimal factor setting against to the better thermal management of package is $A_1B_1C_2$ which are identical from analyses of the S/N and mean value, shown in Table 5. It means that the TQFP package with best thermal handling capability in the analysis has to be assembled with 8 x 8 mm^2 die pad, Hitachi CEL-9200XU compound and total package thickness of 1.4 mm.

The analysis of data from experiments, as summarized in Table 6 and 7, gives same conclusion as the CAE part. The response graph for S/N and mean value are illustrated in Fig. 4 and 5, respectively.

Table 3. Factors and levels

Level	1	2
A. Leadframe (Die pad)	8 ϒ 8 mm^2	7 ϒ 7 mm^2
B. EMC	CEL-9200XU	EME-6300HJ
C. Package thickness	1.0 mm	1.4 mm

Table 4. Orthogonal array and CAE results

No.	A	B	C	R_{ja}	£
1	1	1	1	32.80	-30.32
2	1	2	2	36.10	-31.15
3	2	1	2	35.20	-30.93
4	2	2	1	42.50	-32.57
Sum	-	-	-	146.60	-124.97
Mean	-	-	-	36.65	-31.24

R_{ja}: Thermal Resistance £ : S/N ratio

Table 5. The response table of factor effect from S/N ratio and mean value (CAE data)

£	A	B	C
Level 1	-61.47	-61.25	-62.89
Level 2	-63.50	-63.72	-62.08

Optimal setting: $A_1B_1C_2$

Mean value	A	B	C
Level 1	68.9	68.0	75.3
Level 2	77.7	78.6	71.3

Optimal setting: $A_1B_1C_2$

Table 6. Orthogonal array and experimental results

No.	A	B	C	R_{ja}	£
1	1	1	1	32.70	-30.29
2	1	2	2	34.20	-30.67
3	2	1	2	35.10	-30.90
4	2	2	1	41.40	-32.34
Sum	-	-	-	143.40	-124.20
Mean	-	-	-	35.85	-31.05

R_{ja}: Thermal Resistance £ : S/N ratio

Table 7. The response table of factor effect from S/N ratio and mean value (experimental data)

£	A	B	C
Level 1	-60.96	-61.18	-62.63
Level 2	-63.24	-63.01	-61.57

Optimal setting: $A_1B_1C_2$

Mean value	A	B	C
Level 1	66.90	67.80	74.10
Level 2	76.50	75.60	69.30

Optimal setting: $A_1B_1C_2$

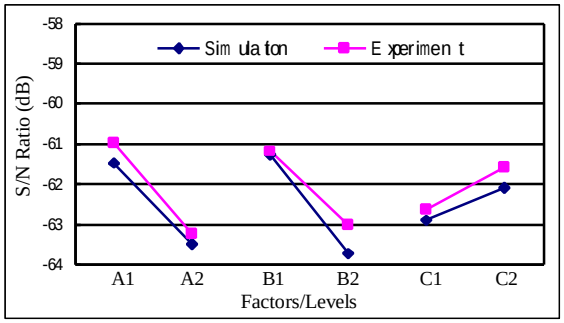

Fig.4. The S/N response graph of CAE and experimental data.

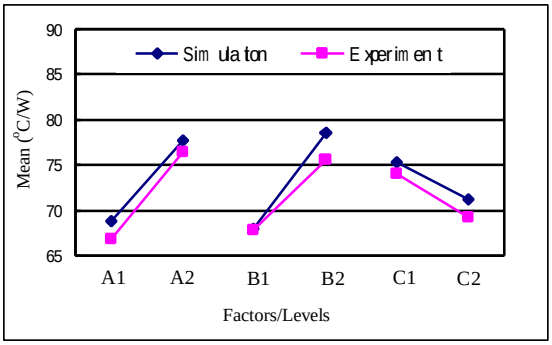

Fig. 5. The mean value response graph of CAE and experimental data.

The R_{ja} value of the optimal setting could be predicted from the CAE and experimental data that give 30.8°C/W and 30.3°C/W, respectively. These figures deviate ~ 1.6 % to each other. However, confirmation experiment with optimal setting obtains the R_{ja} as 31.8°C/W that is about 3.3 % higher than those predicted values.

The delamination phenomenon is found between die pad bottom and molding compound from test products during the scanning acoustic microscope (SAM) investigation. No delamination is found in the products with factor set #1 and #3 and slightly in set #4 products. The set #2 products have the worst delamination as that depicted in Fig. 6. The delamination might be one of the sources influenced the data accuracy. The effect of the delamination on package thermal management is the subject beyond the scope of this study.

Conclusively, data from the CAE modeling is good enough for further evaluations of TQFP package as compared to those from experiments. Hereafter, the discussions are based on outputs from CAE analyses.

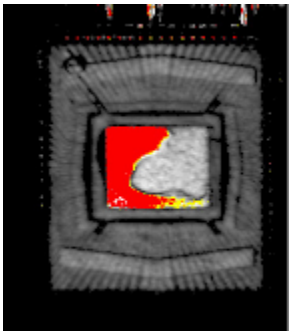

Fig. 6. Delamination observed in test products from SAM.

B. The influence from application

The thermal behavior of the package is influenced heavily by the application situation and environment. As keeping the optimal factor setting for the package, the effect of the rated power on R_{ja} for packages mounted above 2- and 4- layer PCB is plotted in Fig. 7. The R_{ja} decreases with the rated power from 0.2 W to 1.0 W for its larger heat convection and radiation rate from the higher surface temperature at higher rated power.

With the advancing of the IC manufacturing technology, the integration density becomes higher within each single chip. The R_{ja} of the package shows almost linearly decrease with the increase of the chip size under 1 W rated power while taking same package dimension, materials and die thickness, as illustrated in Fig. 8. It indicates that large chip gives better R_{ja} reading from lower integration density.

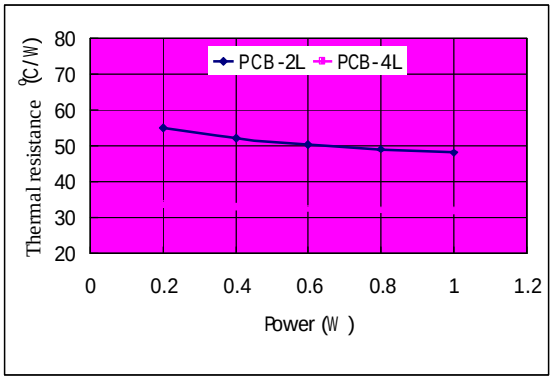

Fig. 7. The relationship of thermal resistance vs. rated power.

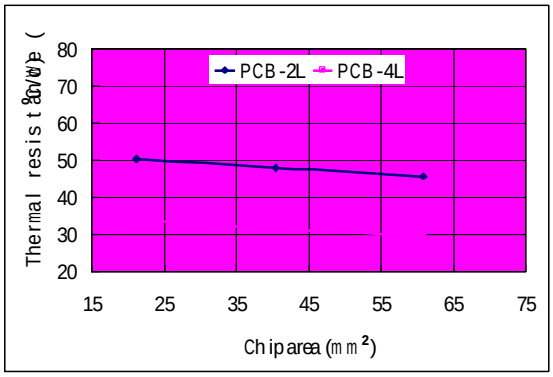

Fig. 8. The relationship of thermal resistance vs. chip area.

The influence of PCB has been shown in both Fig. 7 and Fig. 8 together with rated power and chip area. The contribution from metal layer number within PCB manifests itself from the data. It could also be drawn from the thermal conductivity coefficient, K_{xy}, of PCB that is 10 times higher for 4-layer board, 17.0 W/mK than the 2-layer board, 1.6 W/mK. Under 1 W rated power, the 4-layer PCB reduces the R_{ja} up to ~ 35 % as compared to those from 2-layer PCB. Though extrinsically to package, influence of PCB thermal conduction capability diminished those from other sources.

Conclusion

It is proved that the results from CAE simulation and

experiments match very well to each other via the DOE analytical tool. The predicted R_{ja}s from CAE method are within 5% accuracy as against to the confirmation result, 31.8°C/W.

The TQFP package with best thermal handling capability in the analysis has to be assembled with 8 x 8 mm^2 die pad leadframe, Hitachi CEL-9200XU compound and total package thickness of 1.4 mm. The R_{ja} decreases with the increase of the rated power in the range of 0.2 to 1.0 W. Owing to its heat dissipation capability, increase of chip area decreases almost linearly the R_{ja} for the same TQFP package. However, the contribution from PCB on the thermal handling capability of the package overrides those from other sources.

Conclusively, data from the CAE modeling is good enough for application evaluations of TQFP package as compared to those from experiments.

Reference

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