# **Quad Line Receiver**

The MC10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V<sub>BB</sub>) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

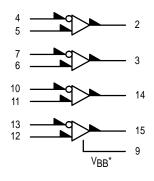
Active current sources provide the MC10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to  $V_{\mbox{\footnotesize{BB}}}$  (pin 9) to prevent upsetting the current source bias network.

 $P_D = 110 \text{ mW typ/pkg (No Load)}$ 

 $t_{pd} = 2.0 \text{ ns typ}$ 

 $t_{\rm f}$ ,  $t_{\rm f} = 2.0$  ns typ (20%–80%)

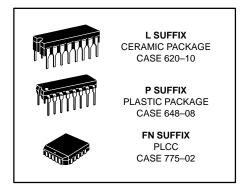
#### **LOGIC DIAGRAM**



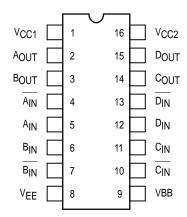
V<sub>CC1</sub> = PIN 1 V<sub>CC2</sub> = PIN 16 V<sub>EE</sub> = PIN 8

When the input pin with the bubble goes positive, the output goes negative.

## MC10115



#### DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion
Tables on page 6–11 of the Motorola MECL Data
Book (DL122/D).

 $<sup>^*</sup>V_{BB}$  to be used to supply bias to the MC10115 only and bypassed (when used) with 0.01  $_\mu F$  to 0.1  $_\mu F$  capacitor to ground (0 V).  $V_{BB}$  can source < 1.0 mA.

### **ELECTRICAL CHARACTERISTICS**

				Test Limits							
		Symbol	Pin Under Test	-30°C		+25°C			+85°C		
Characteristic				Min	Max	Min	Тур	Max	Min	Max	Unit
Power Supply Drain Current		ΙE	8		29			26		29	mAdc
Input Current		linH	4		150			95		95	μAdc
		ICBO	4		1.5			1.0		1.0	μAdc
Output Voltage	Logic 1	Voн	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
Output Voltage	Logic 0	V <sub>OL</sub>	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
Threshold Volta	ge Logic 1	Vона	2	-1.080		-0.980			-0.910		Vdc
Threshold Volta	ge Logic 0	VOLA	2		-1.655			-1.630		-1.595	Vdc
Reference Volta	age	V <sub>BB</sub>	9	1.420	1.280	-1.350		-1.230	1.295	-1.150	Vdc
Switching Times	s (50Ω Load)										ns
Propagation De	lay	t <sub>4-2+</sub> t <sub>4+2-</sub>	2 2	1.0 1.0	3.1 3.1	1.0 1.0		2.9 2.9	1.0 1.0	3.3 3.3	
Rise Time	(20 to 80%)	t <sub>2+</sub>	2	1.1	3.6	1.1		3.3	1.1	3.7	
Fall Time	(20 to 80%)	t <sub>2</sub> _	2	1.1	3.6	1.1		3.3	1.1	3.7	

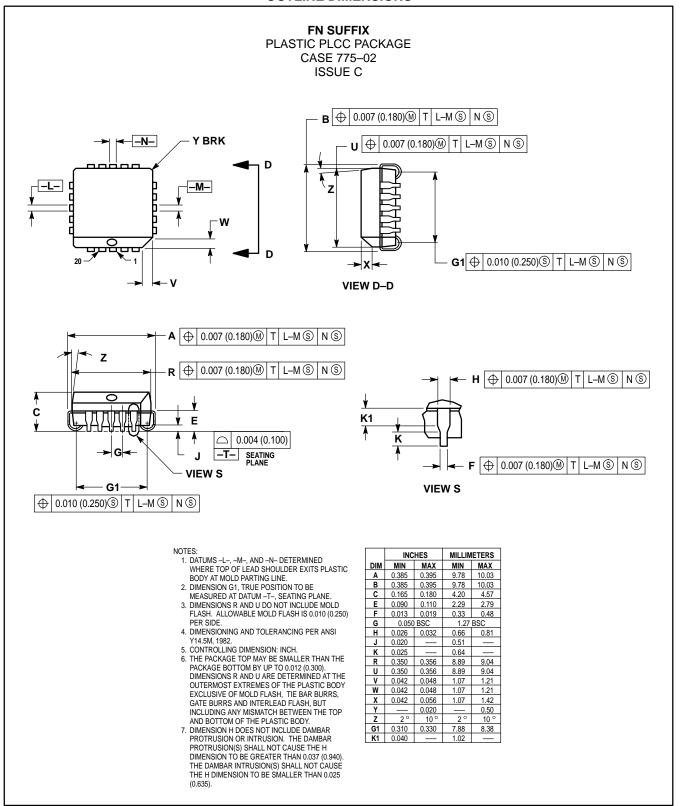
## **ELECTRICAL CHARACTERISTICS** (continued)

					TEST VOLTAGE VALUES (Volts)					
@ Test Temperature				V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>BB</sub>	VEE	
–30°C					-1.890	-1.205	-1.500	From	-5.2	
			+25°C	-0.810	-1.850	-1.105	-1.475	Pin	<b>−</b> 5.2	
			+85°C	-0.700	-1.825	-1.035	-1.440	9	<b>−</b> 5.2	
Pin			TE	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
Characteristic		Symbol	Under Test	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>BB</sub>	VEE	(VCC)
Power Supply Drain C	urrent	ΙE	8		4,7,10,13			5,6,11,12	8	1, 16
Input Current		linH	4	4	7,10,13			5,6,11,12	8	1, 16
		ICBO	4		7,10,13			5,6,11,12	8,4	1, 16
Output Voltage	Logic 1	Vон	2	7,10,13	4			5,6,11,12	8	1, 16
Output Voltage	Logic 0	VOL	2	4	7,10,13			5,6,11,12	8	1, 16
Threshold Voltage	Logic 1	V <sub>OHA</sub>	2		7,10,13		4	5,6,11,12	8	1, 16
Threshold Voltage	Logic 0	VOLA	2		7,10,13	4		5,6,11,12	8	1, 16
Reference Voltage		V <sub>BB</sub>	9					5,6,11,12	8	1, 16
Switching Times	(50Ω Load)			Pu	lse In	Pulse	e Out		–3.2 V	+2.0 V
Propagation Delay		t <sub>4-2+</sub> t <sub>4+2-</sub>	2 2		4 4		<u>2</u> 2	5,6,11,12 5,6,11,12	8 8	1, 16 1, 16
Rise Time	(20 to 80%)	t <sub>2+</sub>	2		4	2	2	5,6,11,12	8	1, 16
Fall Time	(20 to 80%)	t <sub>2-</sub>	2		4	] :	2	5,6,11,12	8	1, 16

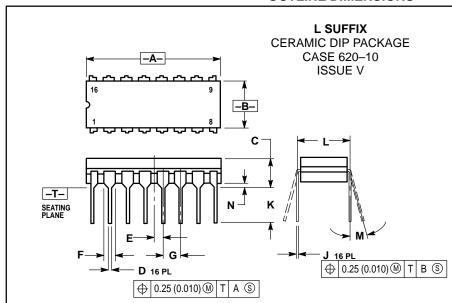
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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#### **OUTLINE DIMENSIONS**



#### **OUTLINE DIMENSIONS**

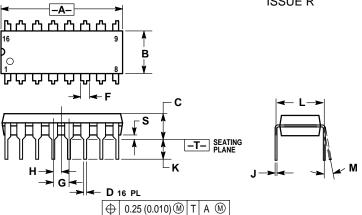


#### NOTES:

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC

			MILL IMPTEDO			
	INC	HES	MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	0.750	0.785	19.05	19.93		
В	0.240	0.295	6.10	7.49		
С		0.200		5.08		
D	0.015	0.020	0.39	0.50		
Е	0.050	BSC	1.27 BSC			
F	0.055	0.065	1.40	1.65		
G	0.100	BSC	2.54 BSC			
Н	0.008	0.015	0.21	0.38		
K	0.125	0.170	3.18	4.31		
L	0.300	BSC	7.62 BSC			
М	0°	15°	0 °	15°		
N	0.020	0.040	0.51	1.01		





- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	0.740	0.770	18.80	19.55		
В	0.250	0.270	6.35	6.85		
С	0.145	0.175	3.69	4.44		
D	0.015	0.021	0.39	0.53		
F	0.040	0.70	1.02	1.77		
G	0.100	BSC	2.54 BSC			
Н	0.050	BSC	1.27 BSC			
J	0.008	0.015	0.21	0.38		
K	0.110	0.130	2.80	3.30		
L	0.295	0.305	7.50	7.74		
M	0°	10 °	0°	10 °		
S	0.020	0.040	0.51	1.01		

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