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LAB 14 Manual

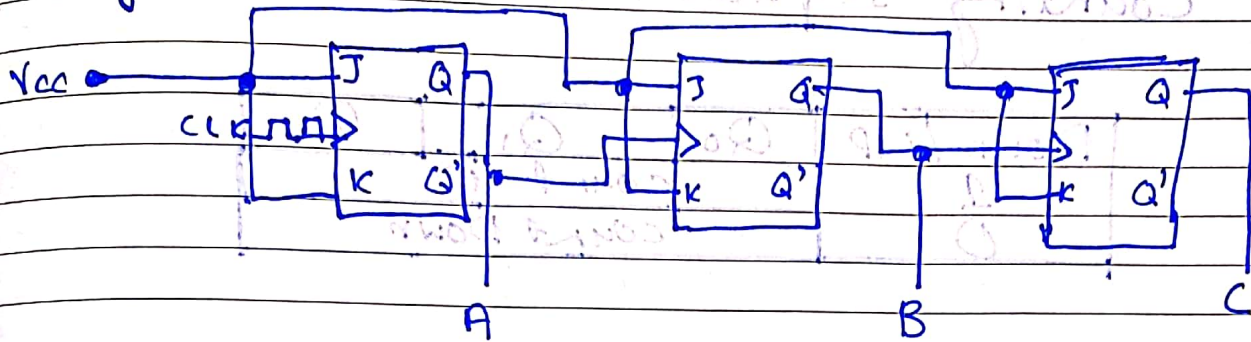
Counters:-

A registers that goes through or prescribed sequence of states upon the application of input pulses is called a counter and they may occur at fixed intervals of ~~the sequence~~ time or random intervals. The sequence of states may follow the binary number sequence or any other sequence of states. A counter that follow the binary number sequence is called binary counter. Counters are available in two categories: ripple counter and synchronous counters. In a ripple counter, the flip flop output transition series as a source for triggering other flip flops. In other words, the clock inputs of some or all of the flip flop are triggered not by the common clock pulses but rather by the transition that occurs in other flip flop outputs. In synchronous counters the clock inputs of all the flip flops receive the common clock pulse and the change of state is determined by the present state of the counter.



8.00 am

Asynchronous Counter:-



10.30

11.00

11.30

Noon

12.30

1.00

1.30

2.00

High

CLK

FF0

FF1

FF2

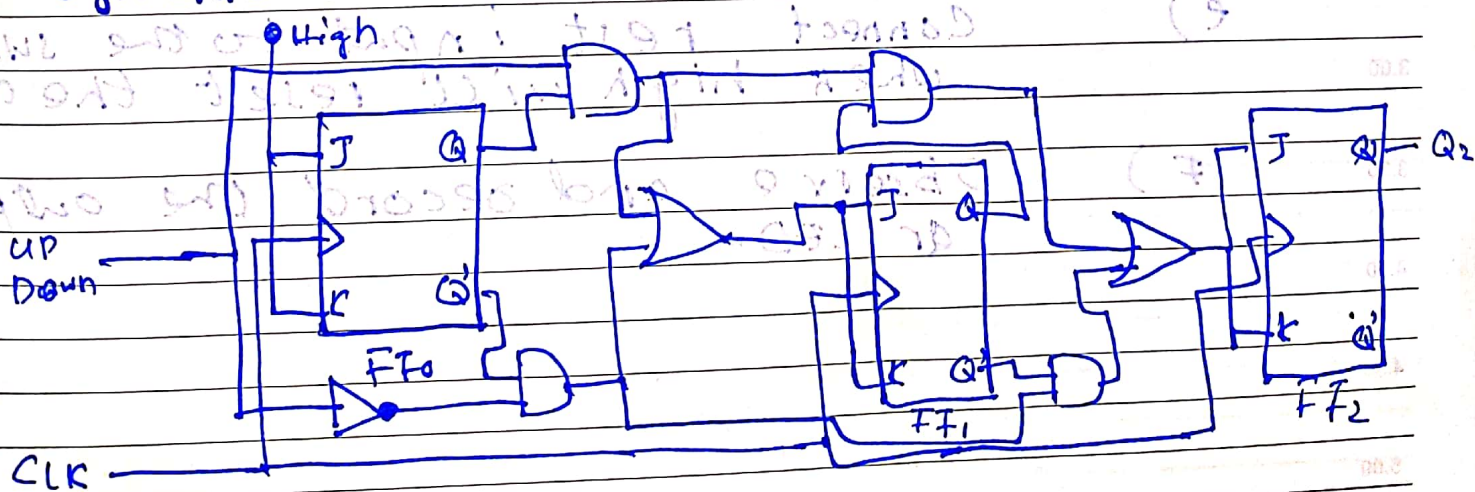
Q0

Q1

Q2

0 1 2 3 4 5 6 7 8 9 0

Synchronous Counter



5.00

Counting Sequence: $2^3 = 8$ words

Down / UP	Q ₀	Q ₁	Q ₂
1	count up		
0	count down		

Procedure

- Connect the trainer with the power supply
- Supply the VCC and GND in the pin 14/16 and 8, 7 -
- Wire the Pin of FCC according to the diagram refer to pin configuration of FCS
- Drive up/down with the input switch in the trainer board and CP input from the clock on the trainer board, connect output Q₁ to LED.
- Connect reset input to the switch when high will reset the counter
- Observe and record the output or LED.

Background Theory:-

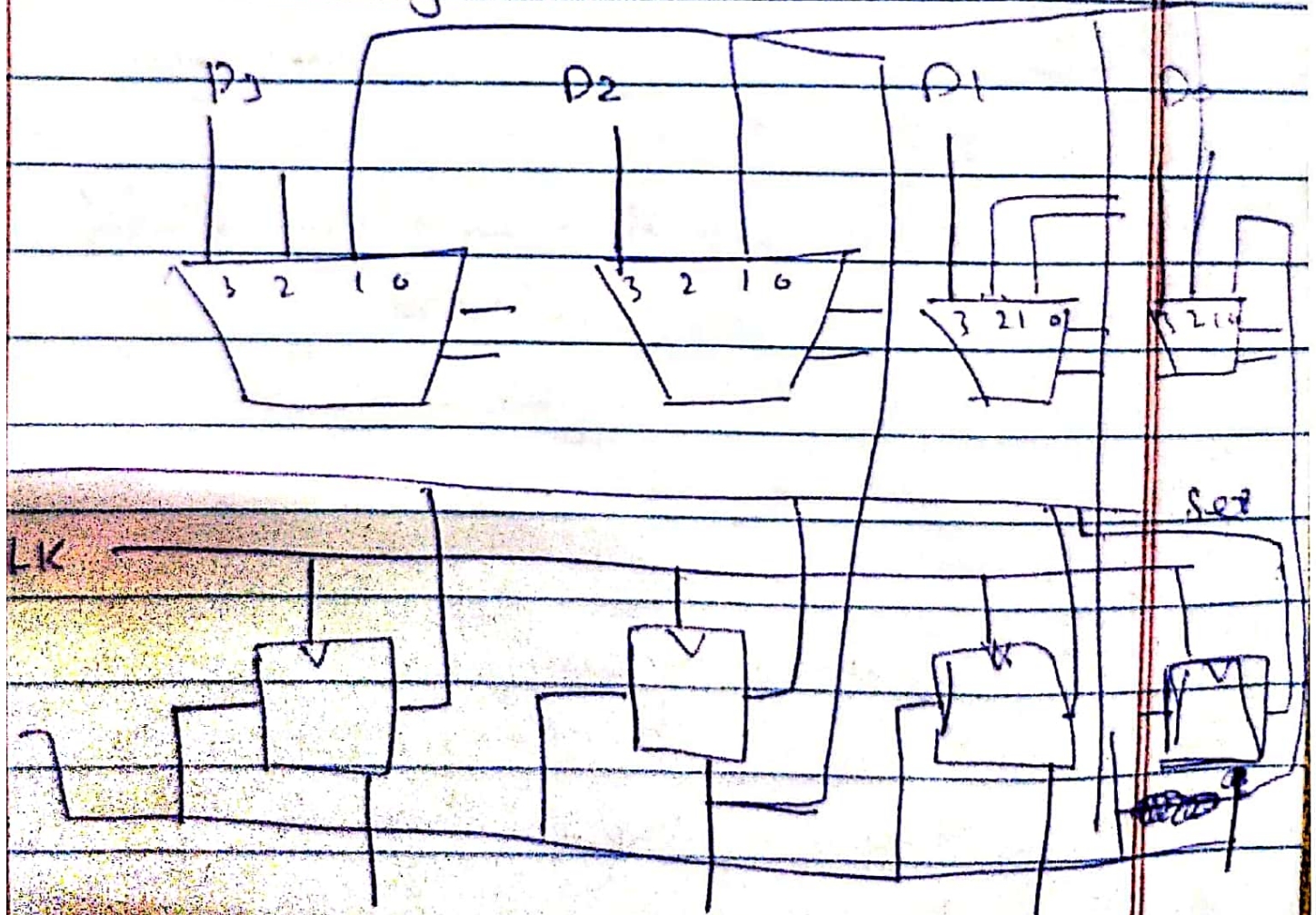
A register is used to store n bits of information where n is number of flipflops

A register consist of a set of flip flops, together with gates that performs data processing tasks. The flip flop hold data and the gates determine the new or transformed data to be transferred

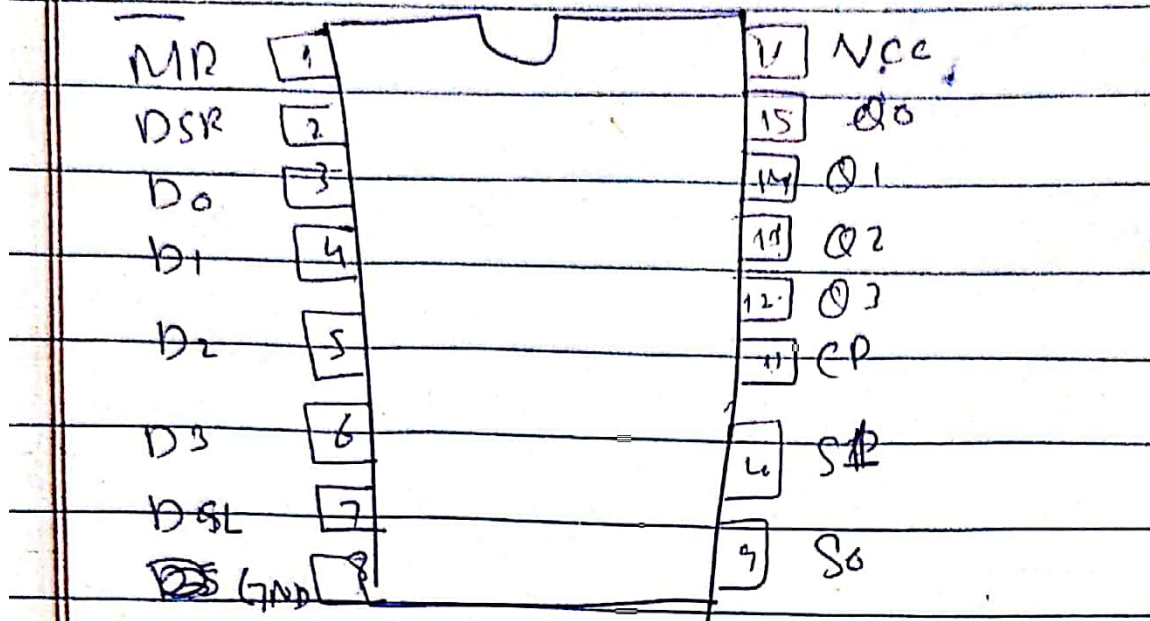
into the flip flops. The registers have two types, one simple register and other register with parallel loads. The register with parallel load is the register in which we can easily store the value of our own choice. The ability of register is controlled by a control input, If control input is 1 then the data which store in the register remain store in the register. Another type of register is known as shift register.

The shift register is capable of shifting its stored bit laterally in one or both directions.

The logical configuration of a shift register consists of a chain of flip-flops in cascade, with the output of one flip-flop connected to the input of another flip-flop. All flip-flops receive a common clock pulse which activates the shift from each stage to the next.



(UNIVERSAL Shift Register)



(Characteristic Table)

S ₁	S ₀	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Parallel Load Operation

S ₁	S ₀	D ₀ D ₁ D ₂ D ₃	Q ₀ Q ₁ Q ₂ Q ₃
0	0		
0	1		
1	0		
1	1		

Procedure:

Connect the trainer with Power supply.
For clock, connect function generator with the power supply. Keep frequency knob on minimum, press the button for function of square wave and keep the frequency range on minimum rotate the amplitude knob to max and get the output from it.

Connect the red alligator clip with the CP pin of the IC and ground the black alligator clip.

Mount the IC 74LS194 on the trainer board.

Supply the VCC and GND to the pin 16 and 8 respectively.

Wire the pins of IC, refer to the pin configuration.

Drive the D's, Dsr, Dsl, S0, S1 inputs with input switches on the trainer board. and CP input from the clock on the trainer board.

Connect the master Qs to the LED.