



FAST

الذى علم بالقلم. علم الانسان ما لم يعلم.

National University of Computer and Emerging Sciences

DEPARTMENT OF COMPUTER SCIENCE

Digital Logic Design Lab

Assignment-01

DLD-LAB ASSIGNMENT-01

Assignment Due Date: 13th April, 2021

Max. Marks: 60

Engr. Khuram Shahzad
(Instructor)

Guidelines for the submission of assignment

- ✓ **You must have to follow these guidelines for the submission of assignment.**
 - ☐ **No late submissions will be entertained.**
 - ☐ **All submissions should be made on Google Class Room.**
 - ☐ **Emailed assignment will be marked as 0.**
 - ☐ **An individual/group may be assigned a **straight-forward 0** if the submitted assessed Task is copied/cheated from another individual/group.**
 - ☐ **Individual viva can be held before finalization of this assignment marks.**
 - ☐ **Upload only a **PDF/MS word** file including all tasks.**

Assignment-01: Task-01(10 marks)

Use [Logic.ly](https://logic.ly) to design circuit diagrams

1. $F1 = A'B'C + A'B'C + A'BC + ABC' + ABC + A'B' + BC' + AB$
 2. $F4 = C + S$ where $C = xy + xz + yz$ and $S = C'(x + y + z) + xyz$
- ✓ Your Task are:
1. Design Truth tables for all the above Boolean Functions.
 2. Design Circuit Diagrams for all the Boolean Functions using basic gates (OR, AND, NOT).
List down how much IC's will be used(with their name & number) in circuit diagram.
 3. Design Circuit Diagrams for all the Boolean Functions using Universal Gate (NAND).
List down how much IC's will be used(with their name & number) in circuit diagram.

Assignment-01: Task-02(15 marks)

Use [Logic.ly](https://logic.ly) to design circuit diagrams

1. $F3 = AB + A'B'D + A'B + AB'C'D$
2. $F4 = C + S$ where $C = xy + yz$ and $S = C'(x + y) + xyz$

Your Task are:

1. Design Truth tables for all the above Boolean Functions.
2. Design Circuit Diagrams for all the Boolean Functions using basic gates (OR, AND, NOT).
List down how much IC's will be used(with their name & number) in circuit diagram.
4. Design Circuit Diagrams for all the Boolean Functions using Universal Gate (NOR).
List down how much IC's will be used(with their name & number) in circuit diagram.

Assignment-01: Task-04 (15 marks)

Use [Logic.ly](https://logic.ly) to design circuit diagrams

- ✓ Using K-maps, find the minimal Boolean expression of the following SOP and POS representations.

List down how much IC's will be used(with their name & number) in circuit diagram.

- a. $f(w,x,y,z) = \sum(7,13,14,15)$
- b. $f(w,x,y,z) = \prod(1,4,5,6,11,12,13,14,15)$
- c. $f(w,x,y,z) = \sum(1,3,4,5,7,8,9,11,15)$
- d. $f(w,x,y,z) = \prod(0,4,5,7,8,9,13,15)$

Assignment-01: Task-05 (05 marks)

Use [Logic.ly](https://logic.ly) to design circuit diagrams

- ✓ Use a Karnaugh map to generate a simple Boolean expression for this truth table, and draw a gate circuit equivalent to that expression:
- ✓ *List down how much IC's will be used*
- ✓ *(with their name & number) in circuit diagram.*

| A | B | C | D | Output |
|---|---|---|---|--------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

GOOD LUCK ☺