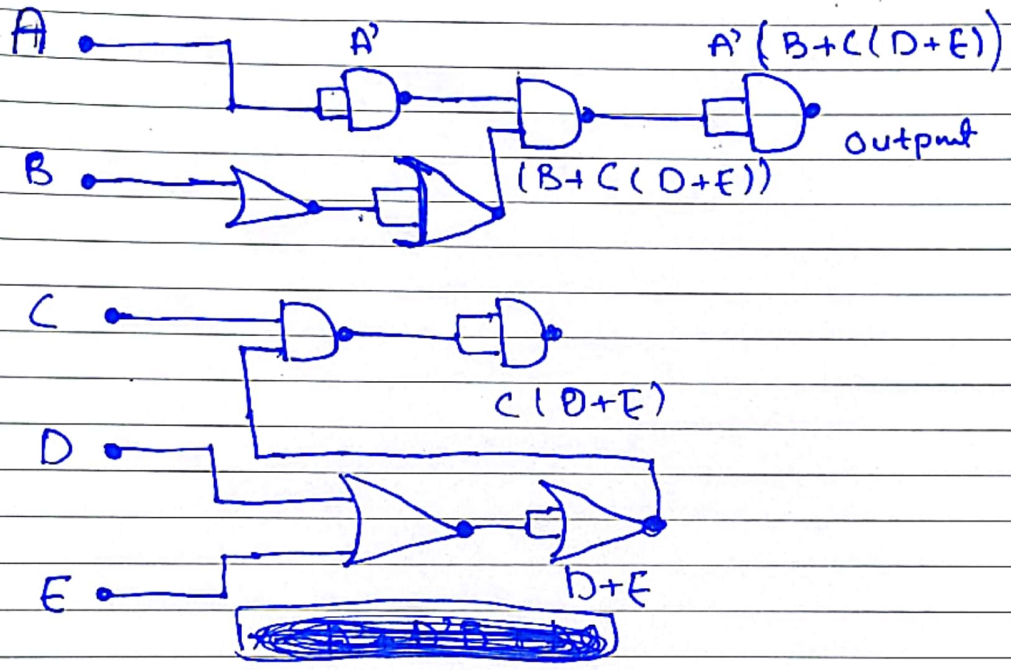
Name: Hassan Ali
Roll No: 20P-0149
Section: "C"

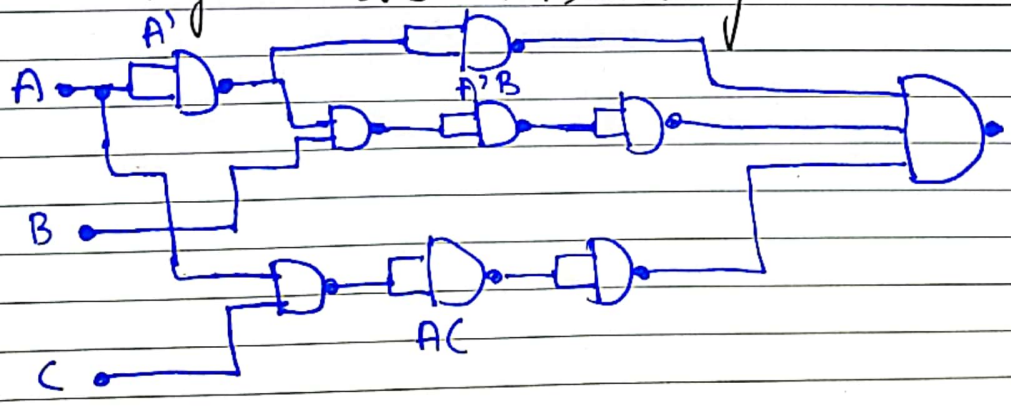
Q 1

Ans:



Q2 $x = A' + A'B + AC$

Figure 5:54 (a) using NAND



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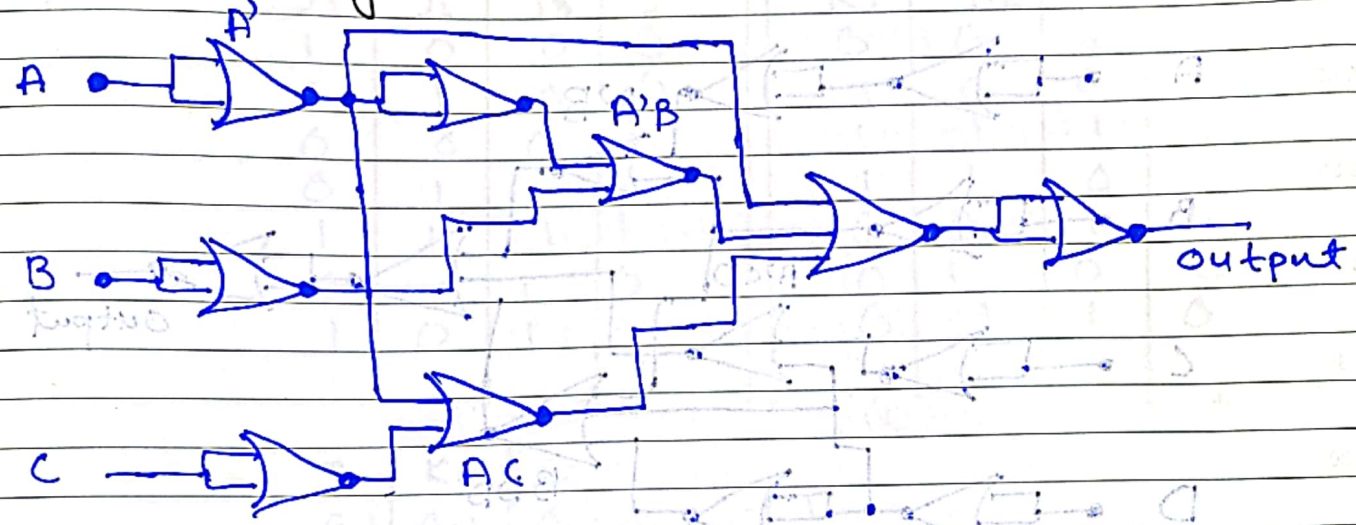
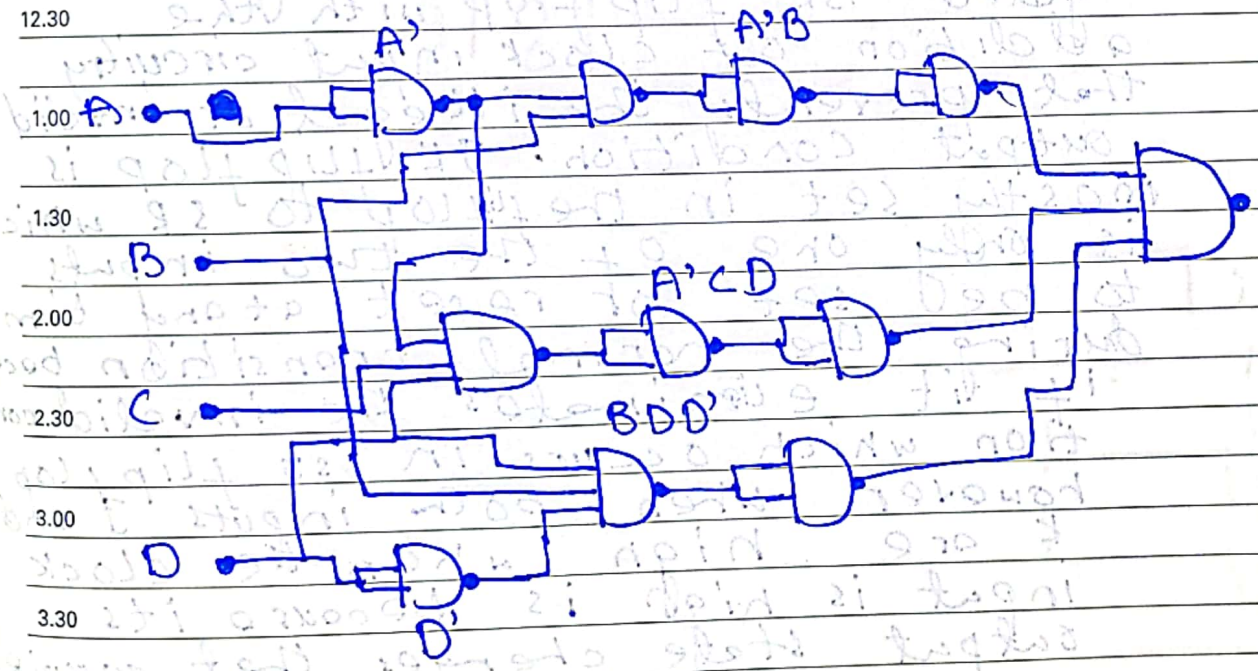
Now Using NOR



B) Figure 5.54 Using Nand

$A'B + A'CD + BDD'$



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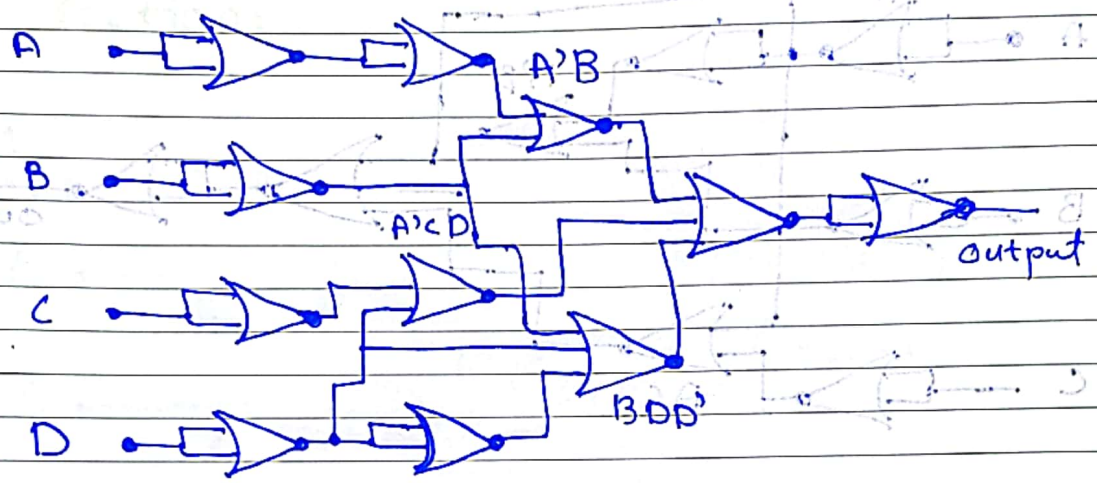
Using NOR



Q3:

Ans The JK flip flop is basically a gated SR flip flop with the addition of clock input circuitry that prevents the illegal or invalid output condition. JK flip flop is mostly set in the flip flop to SR which is only one of the two inputs to be set or reset at any time during the normal transition because it eliminates the invalid condition which occurs in SR flip flop however when both inputs J and K are high when the clock input is high is because its output state changes that complement each other

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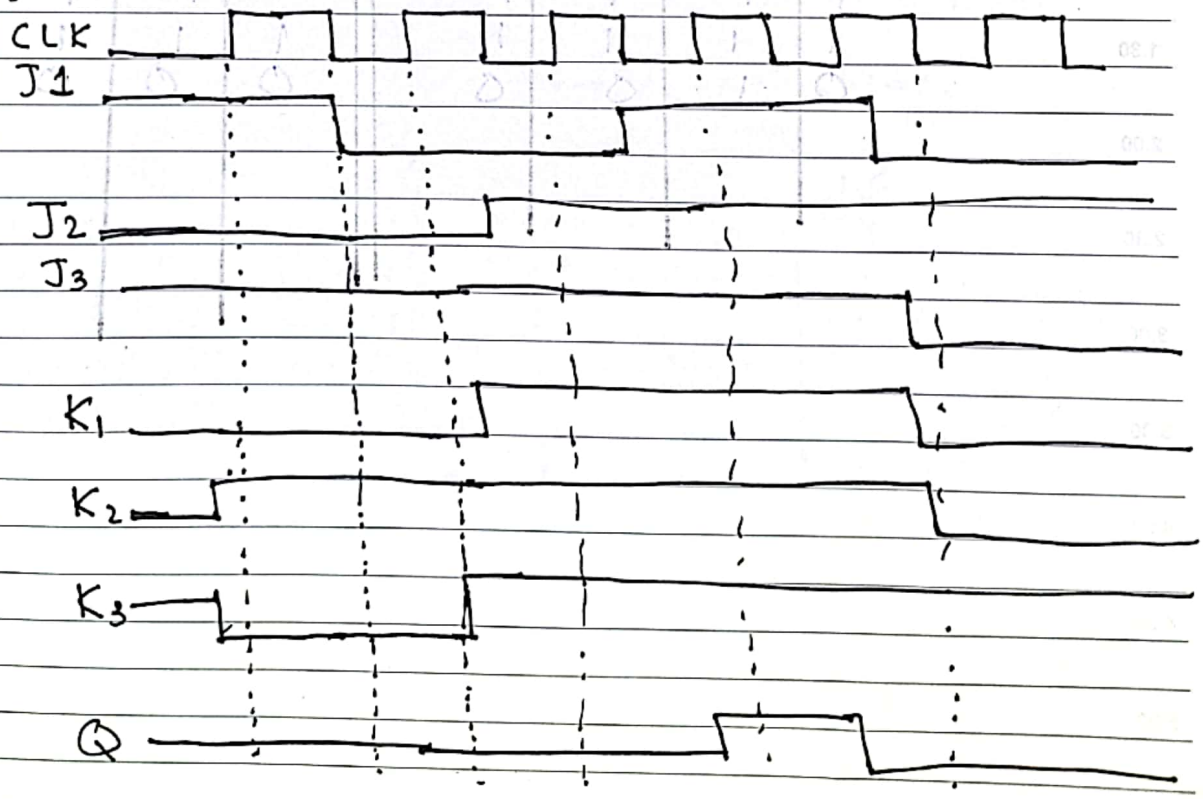
Q16

Ans:

J_1	J_2	J_3	J	K_1	K_2	K_3	K
1	0	0	0	0	0	1	0
1	1	0	0	1	0	0	0
0	0	0	0	1	1	1	1
0	1	1	0	1	1	0	0
1	1	1	0	0	0	1	0
0	1	1	0	0	1	0	0
1	0	1	0	0	1	1	0

J	K	Q
0	0	0
0	0	1
0	1	0
0	0	0
1	0	1
0	0	1
0	0	1

Q17:



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J_1	J_2	J_3	J	K_1	K_2	K_3	K
1	0	1	0	0	0	0	0
0	0	1	0	0	1	0	0
0	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0

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