[Product Folder](#_bookmark68)

[Order Now](#_bookmark68)

[Technical Documents](#_bookmark68)

[Tools & Software](#_bookmark68)

[Support & Community](#_bookmark68)

##### [TPS63020](http://www.ti.com/product/tps63020?qgpn=tps63020), [TPS63021](http://www.ti.com/product/tps63021?qgpn=tps63021)



SLVS916I – JULY 2010 – REVISED OCTOBER 2019

TPS6302x High Efficiency Single Inductor Buck-boost Converter with 4-A Switches

### Features

* Input voltage range: 1.8 V to 5.5 V
* Adjustable output voltage: 1.2 V to 5.5 V
* Output current for VIN > 2.5 V, VOUT = 3.3 V: 2 A
* High efficiency over the entire load range
  + Operating quiescent current: 25 µA
  + Power save mode with mode selection
* Average current mode buck-boost architecture
  + Automatic transition between modes
  + Fixed frequency operation at 2.4 MHz
  + Synchronization possible
* Power good output
* Safety and robust operation features
  + Overtemperature, overvoltage protection
  + Load disconnect during shutdown
* Create a custom design using the
  + TPS63020 with [WEBENCH Power Designer](https://webench.ti.com/wb5/WBTablet/PartDesigner/quickview.jsp?base_pn=TPS63020&origin=PDF_DS%3Flitpdf%3Dslvs916&litsection=device_support)
  + TPS63021 with [WEBENCH Power Designer](https://webench.ti.com/wb5/WBTablet/PartDesigner/quickview.jsp?base_pn=TPS63021&origin=PDF_DS%3Flitpdf%3Dslvs916&litsection=device_support)

### Applications

* Pre-regulation in battery-powered devices: [EPOS](http://www.ti.com/applications/industrial/epos/overview.html) ([portable data terminal](http://www.ti.com/solution/portable-data-terminal), [barcode scanner](http://www.ti.com/solution/barcode-scanner)), [e-](http://www.ti.com/applications/personal-electronics/portable-electronics/overview.html) [cigarette](http://www.ti.com/applications/personal-electronics/portable-electronics/overview.html), [single board computer](http://www.ti.com/solution/single-board-computer), [IP network](http://www.ti.com/solution/ip-network-camera) [camera, video doorbell](http://www.ti.com/solution/ip-network-camera), [land mobile radios](http://www.ti.com/solution/land-mobile-radio)
* Voltage stabilizer: [wired communication](http://www.ti.com/solution/smart-grid-wired-communication), [wireless](http://www.ti.com/solution/smart-grid-wireless-communication) [communication](http://www.ti.com/solution/smart-grid-wireless-communication), [PLC](http://www.ti.com/solution/panel-plc), [optical module](http://www.ti.com/solution/optical-module)
* Backup supercapacitor supply: [electricity meter](http://www.ti.com/solution/electricity-meter), [solid state drive (SSD) - enterprise](http://www.ti.com/solution/solid-state-drive)

### Description

The TPS6302x devices provide a power supply solution for products powered by either a two-cell or three-cell alkaline, NiCd or NiMH battery, a one-cell Li-ion or Li-polymer battery, supercapacitors or other supply rails. Output currents up to 3 A are supported. When using batteries, they can be discharged down to below 2 V. The buck-boost converter is based on a fixed frequency, pulse width modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters power save mode to maintain high efficiency over a wide load current range. The power save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The maximum average current in the switches is limited to a typical value of 4 A. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery.

The TPS6302x devices operate over a free air temperature range of –40°C to 85°C. The devices are packaged in a 14-pin VSON package measuring 3 mm × 4 mm (DSJ).

##### Device Information[(1)](#_bookmark4)

|  |  |  |
| --- | --- | --- |
| **PART NUMBER** | **OUTPUT VOLTAGE** | **PACKAGE** |
| TPS63020 | Adjustable | VSON (14) |
| TPS63021 | 3.3 V |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

##### Simplified Schematic

L1

1.5 µH

100



VIN

1.8 V to 5.5 V

VOUT

3.3 V

C1

2×10 µF

R1

1 Mfi C2

3×22 µF

R3

R2 1 Mfi

180 kfi

Power Good

C3

100 nF

VIN VOUT

TPS63020

FB

VINA EN

PS/SYNC

PG

GND PGND

L2

L1

90

80

70

Efficiency (%)

60

50

40

30

20

10

0

##### Efficiency vs Output Current

VIN = 1.8 V, VOUT = 2.5 V VIN = 3.6 V, VOUT = 2.5 V VIN = 2.4 V, VOUT = 4.5 V VIN = 3.6 V, VOUT = 4.5 V

Power-save mode enabled

100 1m 10m 100m 1

Output Current (A)

D001

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

### Table of Contents

* 1. Features [1](#_bookmark0)
  2. Applications [1](#_bookmark2)
  3. Description [1](#_bookmark0)
  4. Revision History [2](#_bookmark6)
  5. Pin Configuration and Functions [4](#_bookmark7)
  6. Specifications [5](#_bookmark9)
     1. Absolute Maximum Ratings [5](#_bookmark10)
     2. ESD Ratings [5](#_bookmark12)
     3. Recommended Operating Conditions [5](#_bookmark15)
     4. Thermal Information [5](#_bookmark16)
     5. Electrical Characteristics [6](#_bookmark17)
     6. Typical Characteristics [7](#_bookmark20)
  7. Detailed Description [8](#_bookmark21)
     1. Overview [8](#_bookmark22)
     2. Functional Block Diagram [8](#_bookmark23)
     3. Feature Description [9](#_bookmark24)
     4. Device Functional Modes [10](#_bookmark25)
  8. Application and Implementation [13](#_bookmark28)
     1. Application Information [13](#_bookmark29)
     2. Typical Application [13](#_bookmark30)
     3. System Examples [21](#_bookmark52)
  9. Power Supply Recommendations [23](#_bookmark57)
  10. Layout [23](#_bookmark58)
      1. Layout Guidelines [23](#_bookmark59)
      2. Layout Example [23](#_bookmark60)
      3. Thermal Considerations [24](#_bookmark63)
  11. Device and Documentation Support [25](#_bookmark64)
      1. Receiving Notification of Documentation Updates [25](#_bookmark65) 11.2 Device Support [25](#_bookmark66)
  12. Documentation Support [25](#_bookmark67)
  13. Related Links [25](#_bookmark68)
  14. Support Resources [25](#_bookmark69)
  15. Trademarks [26](#_bookmark70)
  16. Electrostatic Discharge Caution [26](#_bookmark71)
  17. Glossary [26](#_bookmark72)
  18. Mechanical, Packaging, and Orderable Information [26](#_bookmark73)

### Revision History

**Changes from Revision H (August 2019) to Revision I Page**

* Changed ESD numbers to reflect latest test insights [5](#_bookmark13)
* Changed Footnotes in order to reflect wording of latest JEP155 and JEP157 specifications [5](#_bookmark14)
* Changed VFB naming and description for better readability [6](#_bookmark19)

**Changes from Revision G (March 2019) to Revision H Page**

* Changed R3 68 kΩ To: R4 68 kΩ in [Figure 28](#_bookmark54) [21](#_bookmark53)

**Changes from Revision F (March 2019) to Revision G Page**

* Changed the Simplified Schematic, removed the connection from VINA to VIN [1](#_bookmark5)
* Changed [Figure 7](#_bookmark32), removed the connection from VINA to VIN [13](#_bookmark31)
* Changed [Figure 28](#_bookmark54), removed the connection from VINA to VIN [21](#_bookmark53)

**Changes from Revision E (May 2017) to Revision F Page**

* Updated Features and Applications on the 1st page [1](#_bookmark0)
* Changed the Body Size column To: Output Voltage in the *Device Information* table [1](#_bookmark3)
* Changed the *Pin Configuration* image [4](#_bookmark8)
* Changed Chapter order in Application Information [13](#_bookmark29)
* Updated output capacitor selection section [15](#_bookmark36)
* Added Table of *Typical Characteristics Curve*s. [17](#_bookmark39)
* Changed [Figure 24](#_bookmark49) and [Figure 25](#_bookmark49) [19](#_bookmark46)
* Added [Figure 26](#_bookmark51) and [Figure 27](#_bookmark51) [20](#_bookmark50)
* Changed [Figure 28](#_bookmark54) [21](#_bookmark53)
* Added system examples *Supercapacitor Backup Power Supply With Active Cell Balancing* and *Low-Power TEC Driver* [22](#_bookmark55)

**Changes from Revision D (October 2015) to Revision E Page**

* Added Voltage AC-spec to [*Absolute Maximum Ratings*](#_bookmark10) table for L1, L2. [5](#_bookmark11)

**Changes from Revision C (February 2013) to Revision D Page**

* Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation*

*Support* section, and *Mechanical, Packaging, and Orderable Information* section [1](#_bookmark1)

**Changes from Revision B (August 2012) to Revision C Page**

* Changed [Figure 7](#_bookmark32) schematic to show correct component values. [13](#_bookmark31)
* Changed [Figure 28](#_bookmark54) schematic to show correct component values. [21](#_bookmark53)

**Changes from Revision A (December 2011) to Revision B Page**

* Changed the Duty cycle in step down conversion values, added MIN = 20%, deleted TYP = 30% and MAX = 40% [6](#_bookmark18)

**Changes from Original (April 2010) to Revision A Page**

* Updated [Figure 31](#_bookmark62) - PCB Layout Suggestion [23](#_bookmark61)

### Pin Configuration and Functions

**DSJ Package**

**14-Pin VSON with Exposed Thermal Pad Top View**

PGND

PGND

PGND

PGND

VINA PG



1

14

2

13

3

12

Thermal Pad

4

11

5

10

6

9

7

8

GND PS/SYNC

FB EN

VOUT VIN

VOUT VIN

L2 L1

L2 L1

Not to scale

PGND

PGND

PGND

PGND

**Pin Functions**

|  |  |  |  |
| --- | --- | --- | --- |
| **PIN** | | **I/O** | **DESCRIPTION** |
| **NAME** | **NO.** |
| EN | 12 | I | Enable input (1 enabled, 0 disabled), must not be left open |
| FB | 3 | I | Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions |
| GND | 2 | – | Control / logic ground |
| L1 | 8, 9 | I | Connection for inductor |
| L2 | 6, 7 | I | Connection for inductor |
| PG | 14 | O | Output power good (1 good, 0 failure; open-drain), can be left open |
| PGND |  | – | Power ground |
| PS/SYNC | 13 | I | Enable / disable power save mode (1 disabled, 0 enabled, clock signal for synchronization), must not be left open |
| VIN | 10, 11 | I | Supply voltage for power stage |
| VINA | 1 | I | Supply voltage for control stage |
| VOUT | 4, 5 | O | Buck-boost converter output |
| Exposed Thermal Pad |  | – | The exposed thermal pad is connected to PGND. |

### Specifications

#### Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | | **MIN** | **MAX** | **UNIT** |
| Voltage (2) | VIN, VINA, VOUT, PS/SYNC, EN, FB, PG | –0.3 | 7 | V |
| L1, L2 (DC) | –0.3 | 7 | V |
| L1, L2 (AC, less than 10 ns)(3) | –3 | 10 | V |
| Operating junction temperature, TJ | | –40 | 150 | °C |
| Storage temperature, Tstg | | –65 | 150 | °C |

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
2. All voltages are with respect to network ground terminal.
3. Normal switching operation

#### ESD Ratings

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | | | **VALUE** | **UNIT** |
| V(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, pins VIN, VINA, L1 (1) | ±500 | V |
| Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins(1) | ±2000 |
| Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1500 |

1. JEDEC document JEP155 states that, with basic ESD control methods applied, 500 V HBM allows a safe manufacturing with proven margin.
2. JEDEC document JEP157 states that, with basic ESD control methods applied, 250 V CDM allows a safe manufacturing.

#### Recommended Operating Conditions

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **MIN** | **NOM** | **MAX** | **UNIT** |
| Supply voltage at VIN, VINA | 1.8 | 5.5 | | V |
| Operating free air temperature, TA | –40 | 85 | | °C |
| Operating junction temperature, TJ | –40 | 125 | | °C |

#### Thermal Information

|  |  |  |  |
| --- | --- | --- | --- |
| **THERMAL METRIC(1)** | | **TPS6302x** | **UNIT** |
| **DSJ (VSON)** |
| **14 PINS** |
| RθJA | Junction-to-ambient thermal resistance | 41.8 | °C/W |
| RθJC(top) | Junction-to-case (top) thermal resistance | 47 | °C/W |
| RθJB | Junction-to-board thermal resistance | 17 | °C/W |
| ψJT | Junction-to-top characterization parameter | 0.9 | °C/W |
| ψJB | Junction-to-board characterization parameter | 16.8 | °C/W |
| RθJC(bot) | Junction-to-case (bottom) thermal resistance | 3.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [*Semiconductor and IC Package Thermal Metrics*](http://www.ti.com/lit/pdf/SPRA953) application report.

#### Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **PARAMETER** | | | **TEST CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNIT** |
| **DC/DC STAGE** | | | | | | | |
| VIN | Input voltage | |  | 1.8 |  | 5.5 | V |
| Minimum input voltage for start-up | | 0°C ≤ TA ≤ 85°C | 1.5 | 1.8 | 1.9 | V |
| Minimum input voltage for start-up | |  | 1.5 | 1.8 | 2.0 | V |
| VOUT | TPS63020 output voltage | |  | 1.2 |  | 5.5 | V |
| Duty cycle in step down conversion | |  | 20% | | |  |
| VFB\_PWM | TPS63020 feedback voltage | | PS/SYNC = VIN | 495 | 500 | 505 | mV |
| TPS63021 output voltage | | 3.267 | 3.3 | 3.333 | V |
| VFB\_PS | TPS63020 feedback voltage / TPS63021 output voltage regulation in PS mode | | PS/SYNC = GND; referenced to VFB\_PWM | 0.6% |  | 5% |  |
|  | Maximum line regulation | |  | 0.5% | | |  |
|  | Maximum load regulation | |  | 0.5% | | |  |
| f | Oscillator frequency | |  | 2200 | 2400 | 2600 | kHz |
|  | Frequency range for synchronization | |  | 2200 | 2400 | 2600 | kHz |
| ISW | Average switch current limit | | VIN = VINA = 3.6 V, TA = 25°C | 3500 | 4000 | 4500 | mA |
|  | High side switch on resistance | | VIN = VINA = 3.6 V | 50 | | | mΩ |
|  | Low side switch on resistance | | VIN = VINA = 3.6 V | 50 | | | mΩ |
| Iq | Quiescent current | VIN and VINA | IOUT = 0 mA, VEN = VIN = VINA = 3.6 V,  VOUT = 3.3 V |  | 25 | 50 | μA |
| VOUT |  | 5 | 10 | μA |
|  | TPS63021 FB input impedance | | VEN = HIGH | 1 | | | MΩ |
| IS | Shutdown current | | VEN = 0 V, VIN = VINA = 3.6 V | 0.1 1 | | | μA |
| **CONTROL STAGE** | | | | | | | |
| UVLO | Under voltage lockout threshold | | VINA voltage decreasing | 1.4 | 1.5 | 1.6 | V |
| Under voltage lockout hysteresis | |  | 200 | | | mV |
| VIL | EN, PS/SYNC input low voltage | |  | 0.4 | | | V |
| VIH | EN, PS/SYNC input high voltage | |  | 1.2 | | | V |
|  | EN, PS/SYNC input current | | Clamped to GND or VINA |  | 0.01 | 0.1 | μA |
|  | PG output low voltage | | VOUT = 3.3 V, IPGL = 10 μA |  | 0.04 | 0.4 | V |
|  | PG output leakage current | |  |  | 0.01 | 0.1 | μA |
|  | Output overvoltage protection | |  | 5.5 7 | | | V |
|  | Overtemperature protection | |  | 140 | | | °C |
|  | Overtemperature hysteresis | |  | 20 | | | °C |

#### Typical Characteristics



Maximum Output Current (A)

Maximum Output Current (A)

|  |  |
| --- | --- |
| 4 | 4 |
| TPS63020 | TPS63021 |
| 3.5 | 3.5 |
| 3 | 3 |
| 2.5 | 2.5 |
| 2 | 2 |
| 1.5 | 1.5 |
| 1 | 1 |
| 0.5 | 0.5 |
| VOUT = 2.5V |  |
| VOUT = 4.5V | VOUT = 3.3V |
| 0 | 0 |
| 1.8 2.2 2.6 3 3.4 3.8 4.2 4.6 5 5.4 | 1.8 2.2 2.6 3 3.4 3.8 4.2 4.6 5 5.4 |
| Input Voltage (V) | Input Voltage (V) |
| **Figure 1. Maximum Output Current Versus Input Voltage,** | **Figure 2. Maximum Output Current Versus Input Voltage,** |
| **TPS63020, VOUT = 2.5 V/4.5 V** | **TPS63021, VOUT = 3.3V** |

### Detailed Description

#### Overview

The control circuit of the device is based on an average current mode topology. The controller also uses input and output voltage feed forward. Changes of input and output voltage are monitored and can immediately change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. At adjustable output voltages, a resistive voltage divider must be connected to that pin. At fixed output voltages, FB must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage will be compared with the internal reference voltage to generate a stable and accurate output voltage.

The device uses four internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range.

To avoid ground shift problems due to the high currents in the switches, two separate ground pins GND and PGND are used. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point, ideally close to the GND pin. Due to the 4-switch topology, the load is always disconnected from the input during shutdown of the converter. To protect the device from overheating an internal temperature sensor is implemented.

#### Functional Block Diagram

L1 L2

VIN VOUT



Current

Sensor

VIN

VOUT

PGND

PGND

Gate

Control

VINA

\_

Modulator

+

+

\_

Oscillator

Device

Control

+ VREF

-

Temperature

Control

PGND

VINA

FB

PG

PS/SYNC

EN

GND

PGND

**Figure 3. Functional Block Diagram (TPS63020)**

#### Functional Block Diagram (continued)

L1 L2

VIN VOUT



Current

Sensor

VIN

VOUT

PGND

PGND

Gate

Control

VINA

\_

Modulator

+

+

\_

Oscillator

Device

Control

+

-

VREF

Temperature

Control

PGND

VINA

FB

PG

PS/SYNC

EN

GND

PGND

**Figure 4. Functional Block Diagram (TPS63021)**

#### Feature Description

##### Dynamic Voltage Positioning

As detailed in [Figure 6](#_bookmark27), the output voltage is typically 3% above the nominal output voltage at light load currents, as the device is in power save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. This allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transient changes.

##### Dynamic Current Limit

To protect the device and the application, the average inductor current is limited internally on the IC. At nominal operating conditions, this current limit is constant. The current limit value can be found in the electrical characteristics table. If the supply voltage at VIN drops below 2.3 V, the current limit is reduced. This can happen when the input power source becomes weak. Increasing output impedance, when the batteries are almost discharged, or an additional heavy pulse load is connected to the battery, can cause the VIN voltage to drop. The dynamic current limit has its lowest value when reaching the minimum recommended supply voltage at VIN. At this voltage, the device is forced into burst mode operation, trying to stay active as long as possible even with a weak input power source.

If the die temperature increases above the recommended maximum temperature, the dynamic current limit becomes active. Similar to the behavior when the input voltage at VIN drops, the current limit is reduced with temperature increasing.

##### Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents flowing from the input.

#### Feature Description (continued)

##### Power Good

The device has a built-in power-good function to indicate whether the output voltage is regulated properly. As soon as the average inductor current limit is reached, the power-good output gets low impedance. The output is open-drain and can be left open if not needed. By connecting a pullup resistor to the supply voltage of the externally connected logic, it is possible to adjust the voltage level within the absolute maximum ratings.

Because it is monitoring the status of the current control loop, the power-good output provides the earliest indication possible for an output voltage break down and leaves the connected application a maximum time to safely react.

##### Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore, overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. The implemented overvoltage protection circuit monitors the output voltage internally as well. In case it reaches the overvoltage threshold, the voltage amplifier regulates the output voltage to this value.

##### Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VINA is lower than approximately its threshold (see [*Electrical Characteristics*](#_bookmark17)). When in operation, the device automatically enters the shutdown mode if the voltage at VINA drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

##### Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see [*Electrical Characteristics*](#_bookmark17)), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

#### Device Functional Modes

##### Soft-start and Short Circuit Protection

After being enabled, the device starts operating. The average current limit ramps up from an initial 400 mA following the output voltage increasing. At an output voltage of about 1.2 V, the current limit is at its nominal value. If the output voltage does not increase, the current limit does not increase. There is no timer implemented. Thus, the output voltage overshoot at start-up, as well as the inrush current, is kept at a minimum. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output. When the output voltage does not increase above 1.2 V, the device assumes a short circuit at the output, and keeps the current limit low to protect itself and the application. At a short on the output during operation, the current limit also is decreased accordingly.

##### Buck-Boost Operation

To regulate the output voltage at all possible input voltage conditions, the device automatically switches from step-down operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step-down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all four switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation when input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum to minimize switching and conduction losses. For the remaining two switches, one is kept permanently on and the other is kept permanently off, thus causing no switching losses.

#### Device Functional Modes (continued)

##### Control Loop

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. [Figure 5](#_bookmark26) shows the control loop.

The non-inverting input of the transconductance amplifier, gmv, is assumed to be constant. The output of gmv defines the average inductor current. The inductor current is reconstructed by measuring the current through the high-side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode, the current is measured during the on-time of the same MOSFET. During the off-time, the current is reconstructed internally starting from the peak value at the end of the on-time cycle. The average current and the feedback from the error amplifier gmv forms the correction signal gmc. This correction signal is compared to the buck and the boost sawtooth ramp giving the PWM signal. Depending on which of the two ramps, the gmc output crosses either the buck or the boost stage is initiated. When the input voltage is close to the output voltage, one buck cycle is always followed by a boost cycle. In this condition, no more than three cycles in a row of the same mode are allowed. This control method in the buck-boost region ensures a robust control and the highest efficiency.

The buck-boost overlap control makes sure that the classical buck-boost function, which would cause two switches to be on every half a cycle, is avoided. Thanks to this block, whenever all switches becomes active during one clock cycle, the two ramps are shifted away from each other. On the other hand, when there is no switching activities because there is a gap between the ramps, the ramps are moved closer together. As a result, the number of classical buck-boost cycles or no switching is reduced to a minimum and high efficiency values has been achieved.





**TM**

**Figure 5. Average Current Mode Control**

#### Device Functional Modes (continued)

##### Power Save Mode and Synchronization

The PS/SYNC pin can be used to select different operation modes. Power save mode is used to improve efficiency at light load. To enable power save mode, PS/SYNC must be set low. If PS/SYNC is set low, then power save mode is entered when the average inductor current gets lower than about 100 mA. At this point, the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency. See [Figure 6](#_bookmark27) for detailed operation of the power save mode.

During the power save mode, the output voltage is monitored with a comparator by the threshold comp low and comp high. When the device enters power save mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the value of output capacitance. As the output voltage falls below the comp low threshold set to 2.5% typical above VOUT, the device ramps up the output voltage again, by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last one or several pulses. The converter continues these pulses until the comp high threshold, set to typically 3.5% above VOUT nominal, is reached and the average inductance current gets lower than about 100 mA. When the load increases above the minimum forced inductor current of about 100 mA, the device automatically switches to pulse width modulation (PWM) mode.

The power save mode can be disabled by programming high at the PS/SYNC. Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency.

Synchronization is done by a phase-locked loop (PLL), so synchronizing to lower and higher frequencies compared to the internal clock works without any issues. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

# Heavy Load transient step



Power save mode at light load

3.5%

3%

2.5%

# Vo

current

Comparator High Comparator low

# PWM mode

Absolute Voltage drop with positioning

**Figure 6. Power Save Mode Thresholds and Dynamic Voltage Positioning**

### Application and Implementation

##### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### Application Information

The TPS6302x are high efficiency, low quiescent current, non-inverting buck-boost converters suitable for applications that need a regulated output voltage from an input supply that can be higher, lower, or equal to the output voltage. Output currents can go as high as 2 A in boost mode and as high as 4 A in buck mode. The average current in the switches is limited to a typical value of 4 A.

#### Typical Application

L1

1.5 µH

L1

L2

VIN



2.5 V to 5.5 V

VOUT

3.3 V at 1.5 A

C1 2×10 µF

C3 100 nF

R1

1 Mfi

VIN VOUT

TPS63020

FB

VINA

EN

PS/SYNC

PG

R2

180 kfi

C2 3×22 µF

R3

1 Mfi

Power Good

PGND

GND

##### Figure 7. Application Circuit

* + 1. **Design Requirements**

The design guideline provides a component selection to operate the device within the recommended operating conditions. See [Table 1](#_bookmark33) for possible inductor and capacitor combinations.

For the fixed output voltage option, the feedback pin needs to be connected to the VOUT pin.

##### Table 1. Matrix of Output Capacitor and Inductor Combinations

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **NOMINAL INDUCTOR VALUE [µH](1)** | **NOMINAL OUTPUT CAPACITOR VALUE [µF](2)** | | | |
| **2×22** | **3×22** | **4×22** | **≥ 100** |
| 1.0 |  | + | + | + |
| 1.5 | + | **+** (3) | + | + |
| 2.2 |  |  | + | + |

1. Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
2. Capacitance tolerance and DC bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
3. Typical application. Other check marks indicate possible filter combinations.

##### Detailed Design Procedure

The TPS6302x series of buck-boost converter has internal loop compensation. Therefore, the external inductor and output capacitors have to be selected to work with the internal compensation. When selecting the external components, a low limit for the inductor value exists to avoid subharmonic oscillation which can be caused by a far too fast ramp up of the inductor current. For the TPS6302x series, the inductor value must be kept at or above 1 µH.

In particular, either 1 µH or 1.5 µH is recommended working at an output current between 1.5 A and 2 A. If operating with a lower load current, it is also possible to use 2.2 µH.

Selecting a larger output capacitor value is less critical because the corner frequency moves to lower frequencies.

###### *Custom Design with WEBENCH Tools*

[Click here](https://webench.ti.com/wb5/WBTablet/PartDesigner/quickview.jsp?base_pn=TPS63020&origin=PDF_DS%3Flitpdf%3Dslvs916&litsection=application) to create a custom design using the TPS63020 device with the WEBENCH® Power Designer.

1. Start by entering your VIN, VOUT and IOUT requirements.
2. Optimize your design for key parameters like efficiency, footprint or cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   * Run electrical simulations to see important waveforms and circuit performance,
   * Run thermal simulations to understand the thermal performance of your board,
   * Export your customized schematic and layout into popular CAD formats,
   * Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at [www.ti.com/webench](http://www.ti.com/lsds/ti/analog/webench/overview.page?DCMP=sva_web_webdesigncntr_en&HQS=sva-web-webdesigncntr-vanity-lp-en).

###### *Inductor Selection*

The inductor selection is affected by several parameters such as the following:

* Inductor ripple current
* Output voltage ripple
* Transition point into Power Save Mode
* Efficiency

See [Table 2](#_bookmark35) for a list of typical inductors.

For high efficiencies, the inductor must have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. Use [Equation 2](#_bookmark34) to avoid saturation of the inductor when calculating the peak current for the inductor in steady state operation. Only the equation which defines the switch current in boost mode is shown because this provides the highest value of current and represents the critical current value for selecting the right inductor.

V - V

Duty Cycle Boost D = OUT IN

V

OUT

Iout Vin  D

(1)

IPEAK =

where

η  (1  D) + 2  *f*  L

* D = duty cycle in boost mode
* f = converter switching frequency (typical 2.5 MHz)
* L = inductor value
* η = estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption) (2)

##### NOTE

The calculation must be done for the minimum input voltage in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to choose an inductor with a saturation current 20% higher than the value calculated using [Equation 2](#_bookmark34). [Table 2](#_bookmark35) lists the possible inductors.

##### Table 2. List of Recommended Inductors (1)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **INDUCTOR VALUE [µH]** | **SATURATION CURRENT [A]** | **DCR [mΩ]** | **PART NUMBER** | **MANUFACTURER** | **SIZE (LxWxH**  **mm)** |
| 1.5 | 5.1 | 15 | XFL4020-152ME | Coilcraft | 4 x 4 x 2.1 |
| 1.5 | 5.4 | 24 | FDV0530S-H-1R5M | muRata | 5 x 5 x 3 |

(1) See [*Third-party Products Disclaimer*](#_bookmark66)*.*

###### *Output Capacitor Selection*

For the output capacitor, it is recommended to use of small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. The recommended nominal output capacitors are three times 22 µF. If, for any reason, the application requires the use of large capacitors that cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. Place the small capacitor as close as possible to the VOUT and PGND pins of the IC.

There are no additional requirements regarding minimum ESR. There is also no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

###### *Input Capacitor Selection*

A 10 µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPS6302x converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

###### *Bypass Capacitor*

To make sure that the internal control circuits are supplied with a stable low noise supply voltage, a capacitor can be connected between VINA and GND. Using a ceramic capacitor with a value of 0.1 µF is recommended. The value of this capacitor must not be higher than 0.22 µF.

##### Setting The Output Voltage

When the adjustable output voltage version TPS63020 is used, the output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB, and GND. The feedback voltage is 500 mV nominal. The low-side resistor R2 (between FB and GND) must be kept in the range of 200 kΩ. Use [Equation 3](#_bookmark37) to calculate the high-side resistor R1 (between VOUT and FB).

R1 = R2 ×  VOUT ⎞

where



⎝ VFB

- 1

⎠

* VFB= 500 mV (3)

##### Table 3. Resistor Selection For Typical Output Voltages

|  |  |  |
| --- | --- | --- |
| **VOUT** | **R1** | **R2** |
| 2.5 V | 750 kΩ | 180 kΩ |
| 3.3 V | 1 MΩ | 180 kΩ |
| 3.6 V | 1.1 MΩ | 180 kΩ |

**Table 3. Resistor Selection For Typical Output Voltages (continued)**

|  |  |  |
| --- | --- | --- |
| **VOUT** | **R1** | **R2** |
| 4.5 V | 1.43 MΩ | 180 kΩ |
| 5 V | 1.6 MΩ | 180 kΩ |

##### Application Curves

**Table 4. Components for Application Characteristic Curves for VOUT = 3.3 V(1)(2)**

|  |  |  |  |
| --- | --- | --- | --- |
| **REFERENCE** | **DESCRIPTION** | **PART NUMBER** | **MANUFACTURER** |
| U1 | High Efficiency Single Inductor Buck-Boost Converter With 4-A Switches | TPS63020 or TPS63021 | Texas Instruments |
| L1 | 1.5 μH, 4 mm x 4 mm x 2 mm | XFL4020-152ML | Coilcraft |
| C1 | 2 × 10 μF 6.3 V, 0603, X5R ceramic | GRM188R60J106ME84D | muRata |
| C2 | 3 × 22 μF 6.3 V, 0603, X5R ceramic | GRM188R60J226MEAOL | muRata |
| C3 | 0.1 μF, X5R or X7R ceramic | Standard | Standard |
| R1 | 1 MΩ at TPS63020, 0 Ω at TPS63021 | Standard | Standard |
| R2 | 180 kΩ at TPS63020, not used at TPS63021 | Standard | Standard |
| R3 | 1 MΩ | Standard | Standard |

1. See [*Third-Party Products Discalimer*](#_bookmark66)*.*
2. For other output voltages, refer to [Table 3](#_bookmark38) for resistor values.

##### Table 5. Typical Characteristics Curves

|  |  |  |
| --- | --- | --- |
| **PARAMETER** | **CONDITIONS** | **FIGURE** |
| **EFFICIENCY** | | |
| Efficiency vs Output Current, TPS63020 (Power save mode enabled) | VIN = 1.8 V, 2.4 V, 3.6 V, VOUT = 2.5 V, 4.5 V, PS/SYNC = Low | [Figure 8](#_bookmark40) |
| Efficiency vs Output Current, TPS63020 (PWM only) | VIN = 1.8 V, 2.4 V, 3.6 V, VOUT = 2.5 V, 4.5 V,  PS/SYNC = High | [Figure 9](#_bookmark40) |
| Efficiency vs Output Current, TPS63021 (Power save mode enabled) | VIN = 2.4 V, 3.6 V, VOUT = 3.3 V, PS/SYNC =  Low | [Figure 10](#_bookmark41) |
| Efficiency vs Output Current, TPS63021 (PWM only) | VIN = 2.4 V, 3.6 V, VOUT = 3.3 V, PS/SYNC =  High | [Figure 11](#_bookmark41) |
| Efficiency vs Input Voltage, TPS63020 (Power save mode enabled) | VOUT = 2.5 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low | [Figure 12](#_bookmark42) |
| Efficiency vs Input Voltage, TPS63020 (Power save mode enabled) | VOUT = 4.5 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low | [Figure 13](#_bookmark42) |
| Efficiency vs Input Voltage, TPS63020 (PWM only) | VOUT = 2.5 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low | [Figure 14](#_bookmark43) |
| Efficiency vs Input Voltage, TPS63020 (PWM only) | VOUT = 2.5 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low | [Figure 15](#_bookmark43) |
| Efficiency vs Input Voltage, TPS63021 (Power save mode enabled) | VOUT = 3.3 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low | [Figure 16](#_bookmark44) |
| Efficiency vs Input Voltage, TPS63021 (PWM only) | VOUT = 3.3 V, Load = 10 mA, 500 mA, 1 A, 2 A, PS/SYNC = Low | [Figure 17](#_bookmark44) |
| **REGULATION ACCURACY** | | |
| Load Regulation, PWM Boost Operation, TPS63020 | VIN = 3.6 V , VOUT = 4.5 V, PS/SYNC = High | [Figure 18](#_bookmark45) |
| Load Regulation, PWM Buck Operation, TPS63020 | VIN = 3.6 V, VOUT = 2.5 V, PS/SYNC = High | [Figure 19](#_bookmark45) |
| Load Regulation, PWM Operation, TPS63021 | VIN = 3.6 V, VOUT = 3.3 V, PS/SYNC = High | [Figure 20](#_bookmark47) |
| Load Transient, TPS63021 | VIN = 2.4 V, VOUT = 3.3 V, Load = 500 mA to  1.5 A | [Figure 21](#_bookmark47) |
| Load Transient, TPS63021 | VIN = 4.2 V, VOUT = 3.3 V, Load = 500 mA to 1.5 A | [Figure 22](#_bookmark48) |
| Line Transient, TPS63021 | VIN = 3.0 V to 3.7 V, VOUT = 3.3 V, Load = 1.5 A | [Figure 23](#_bookmark48) |
| **START-UP** |  |  |
| Start-up Behavior from Rising Enable, TPS63021 | VIN = 2.4 V, VOUT = 3.3 V, Load = 2.2 Ω | [Figure 24](#_bookmark49) |
| Start-up Behavior from Rising Enable, TPS63021 | VIN = 4.2 V, VOUT = 3.3 V, Load = 2.2 Ω | [Figure 25](#_bookmark49) |
| Start-up Behavior from Rising Enable, TPS63021 | VIN = 2.4 V, VOUT = 3.3 V, Load = 2.2 Ω | [Figure 26](#_bookmark51) |
| Start-up Behavior from Rising Enable, TPS63021 | VIN = 4.2 V, VOUT = 3.3 V, Load = 2.2 Ω | [Figure 27](#_bookmark51) |

100 100

90 90

80 80

70 70

60 60

Efficiency (%)

Efficiency (%)

50 50

40 40

30

VIN = 1.8V, VOUT = 2.5V VIN = 3.6V, VOUT = 2.5V VIN = 2.4V, VOUT = 4.5V VIN = 3.6V, VOUT = 4.5V

20

10

TPS63020, Power Save Enabled

0

30

20

VIN = 1.8V, VOUT = 2.5V VIN = 3.6V, VOUT = 2.5V VIN = 2.4V, VOUT = 4.5V VIN = 3.6V, VOUT = 4.5V

10

TPS63020, Power Save Disabled

0

100 1m 10m 100m 1 4

Output Current (A)

**Figure 8. Efficiency Versus Output Current, TPS63020, Power Save Enabled**

100 1m 10m 100m 1 4

Output Current (A)

**Figure 9. Efficiency Versus Output Current, TPS63020, Power Save Disabled**

100 100

90 90

80 80

70 70

60 60

Efficiency (%)

Efficiency (%)

50 50

40 40

30 30

20

VIN = 2.4V

10 VIN = 3.6V

TPS63021, Power Save Enabled

0

20

10

VIN = 2.4V VIN = 3.6V

TPS63021, Power Save Disabled

0

100 1m 10m 100m 1 4

Output Current (A)

**Figure 10. Efficiency Versus Output Current, TPS63021, Power Save Enabled**

100 1m 10m 100m 1 4

Output Current (A)

**Figure 11. Efficiency Versus Output Current, TPS63021, Power Save Disabled**

100 100

90 90

80 80

70 70

60 60

Efficiency (%)

Efficiency (%)

50 50

40 40

30

IOUT = 10mA IOUT = 500mA IOUT = 1A IOUT = 2A

20

10

TPS63020, VOUT = 2.5V, Power Save Enabled

0

30

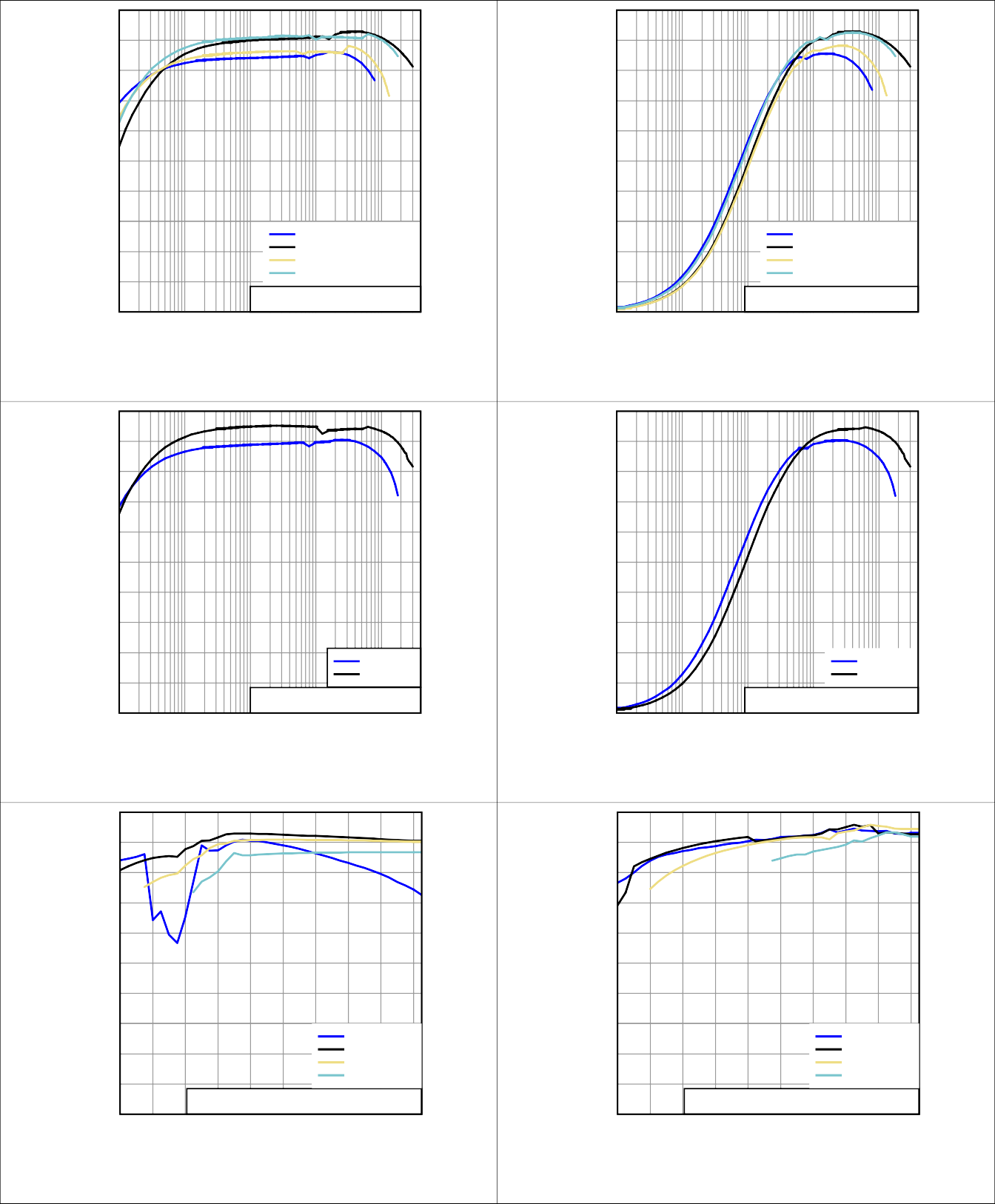
20

IOUT = 10mA IOUT = 500mA IOUT = 1A IOUT = 2A

10

TPS63020, VOUT = 4.5V, Power Save Enabled

0

1.8 2.2 2.6 3 3.4 3.8 4.2 4.6 5 5.4

Input Voltage (V)

**Figure 12. Efficiency Versus Input Voltage, TPS63020, VOUT = 2.5 V, Power Save Enabled**

1.8 2.2 2.6 3 3.4 3.8 4.2 4.6 5 5.4

Input Voltage (V)

**Figure 13. Efficiency Versus Input Voltage, TPS63020, VOUT = 4.5 V, Power Save Enabled**

100 100

90 90

80 80

70 70

60 60

Efficiency (%)

Efficiency (%)

50 50

40 40

30

IOUT = 10mA IOUT = 500mA IOUT = 1A IOUT = 2A

20

10

TPS63020, VOUT = 2.5V, Power Save Disabled

0

30

20

IOUT = 10mA IOUT = 500mA IOUT = 1A IOUT = 2A

10

TPS63020, VOUT = 4.5V, Power Save Disabled

0

1.8 2.2 2.6 3 3.4 3.8 4.2 4.6 5 5.4

Input Voltage (V)

**Figure 14. Efficiency Versus Input Voltage, TPS63020, VOUT = 2.5 V, Power Save Disabled**

1.8 2.2 2.6 3 3.4 3.8 4.2 4.6 5 5.4

Input Voltage (V)

**Figure 15. Efficiency Versus Input Voltage, TPS63020, VOUT = 4.5 V, Power Save Disabled**

100 100

90 90

80 80

70 70

60 60

Efficiency (%)

Efficiency (%)

50 50

40 40

30

IOUT = 10mA IOUT = 500mA IOUT = 1A IOUT = 2A

20

10

TPS63021, Power Save Enabled

0

30

20

IOUT = 10mA IOUT = 500mA IOUT = 1A IOUT = 2A

10

TPS63021, Power Save Disabled

0

1.8 2.2 2.6 3 3.4 3.8 4.2 4.6 5 5.4

Input Voltage (V)

**Figure 16. Efficiency Versus Input Voltage, TPS63021, Power Save Enabled**

1.8 2.2 2.6 3 3.4 3.8 4.2 4.6 5 5.4

Input Voltage (V)

**Figure 17. Efficiency Versus Input Voltage, TPS63021, Power Save Disabled**

4.6 2.6

VIN = 3.6V

VIN = 3.6V

4.55 2.55

4.5 2.5

Output Voltage (V)

Output Voltage (V)

4.45 2.45

4.4

TPS63020, Power Save Disabled

100 1m 10m

100m 1 5

2.4

100 1m 10m

TPS63020, Power Save Disabled

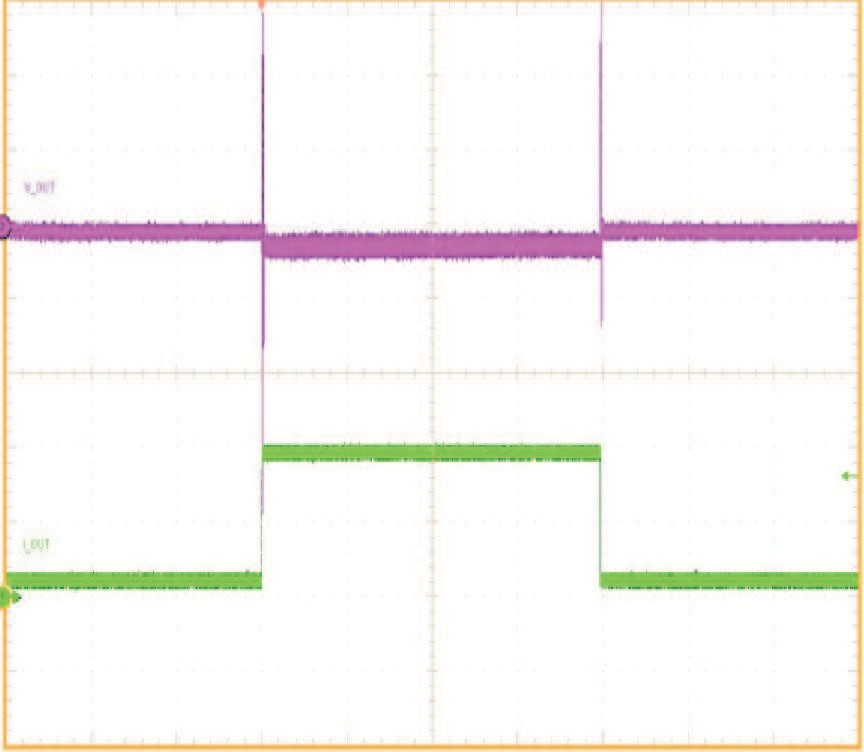
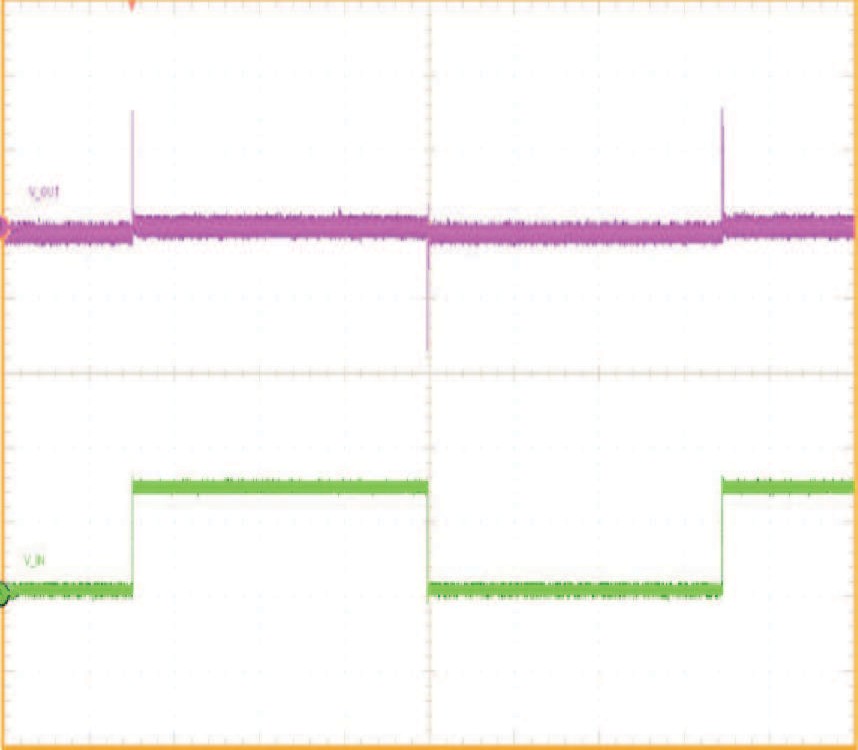
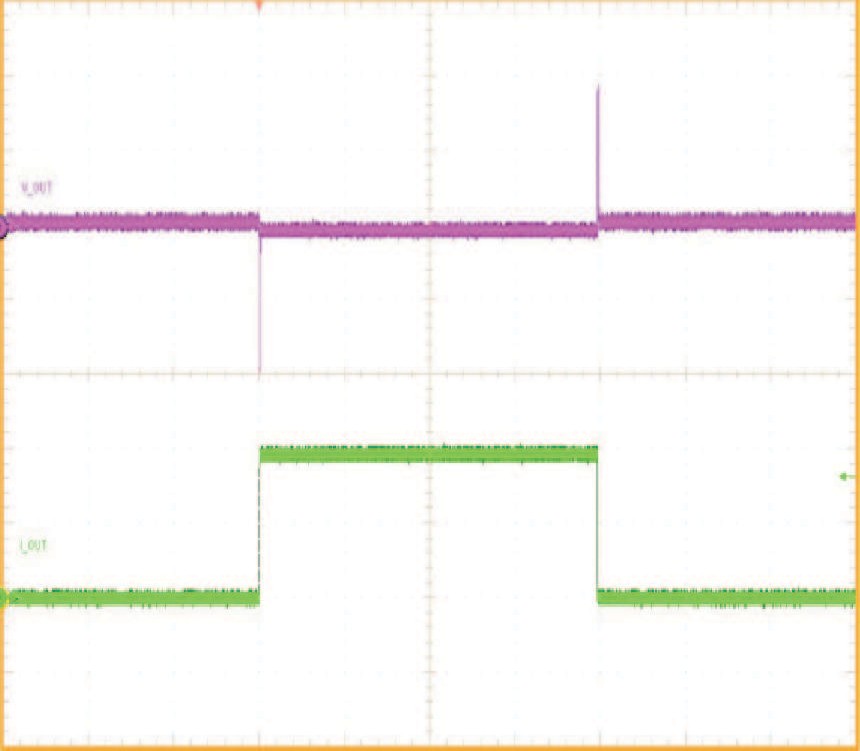
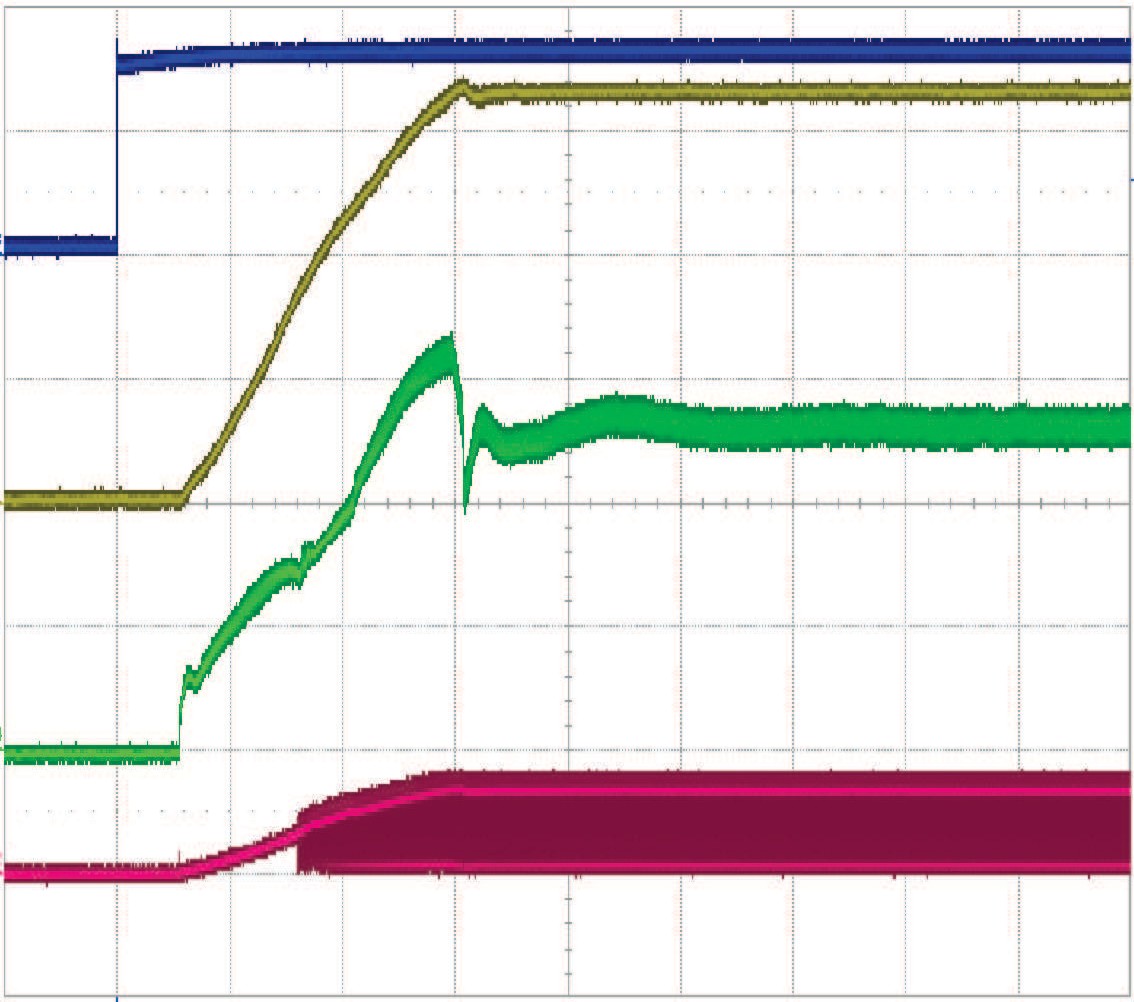
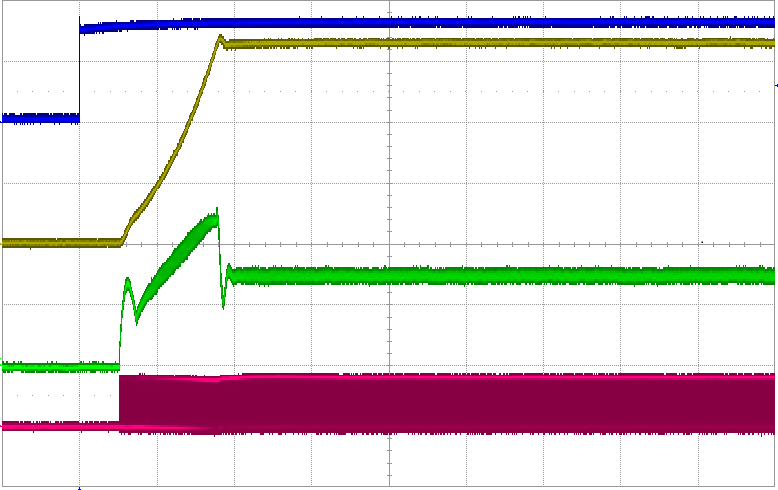
100m 1 5

Output Current (A)

**Figure 18. Output Voltage Versus Output Current, TPS63020, Power Save Disabled**

Output Current (A)

**Figure 19. Output Voltage Versus Output Current, TPS63020, Power Save Enabled**



Output Voltage (V)

|  |  |
| --- | --- |
| 3.4  VIN = 3.6V  3.35  3.3  3.25  TPS63021, Power Save Disabled  3.2  100 1m 10m 100m 1 5  Output Current (A)  **Figure 20. Output Voltage Versus Output Current, TPS63021, Power Save Disabled** | **Output Voltage 50 mV/div, AC**  **Output Current 500 mA/div, DC**  **TPS63021 VIN = 2.4 V, IOUT = 500 mA to 1500 mA**  **Time 2 ms/div**  **Figure 21. Load Transient Response, TPS63021** |
| **Output Voltage 50 mV/div, AC**  **Output Current 500 mA/div, DC**  **TPS63021 VIN = 4.2 V, IOUT = 500 mA to 1500 mA**  **Time 2 ms/div**  **Figure 22. Load Transient Response, TPS63021** | **Output Voltage 50 mV/div, AC**  **Input Voltage 500 mV/div, AC**  **TPS63021 VIN = 3.0 V to 3.7 V, IOUT = 1500 mA**  **Time 2 ms/div**  **Figure 23. Line Transient Response, TPS63021** |
| **Enable**  **2 V/div, DC Output Voltage**  **1 V/div, DC**  **Inductor Current 1 A/div, DC**  **Voltage at L1 5 V/div, DC**  **TPS63020 VIN = 2.4 V, VOUT = 3.3 V, RL = 2.2**   **Time 100** **s/div**  **Figure 24. Start-up Behavior from Rising Enable, TPS63020** | **Enable**  **2 V/div, DC Output Voltage**  **1 V/div, DC**  **Inductor Current 1 A/div, DC**  **Voltage at L2 5 V/div, DC**  **TPS63020 VIN = 4.2 V, VOUT = 3.3 V, RL = 2.2**   **Time 100** **s/div**  **Figure 25. Start-up Behavior from Rising Enable, TPS63020** |

|  |  |
| --- | --- |
| **Enable**  **2 V/div, DC Output Voltage**  **1 V/div, DC**  **Inductor Current 1 A/div, DC**  **Voltage at L2 2 V/div, DC**  **TPS63020 VIN = 2.4 V, VOUT = 3.3 V, RL = 2.2**   **Time 400** **s/div**  **Figure 26. Start-up Behavior from Rising Enable, TPS63020** | **Enable**  **2 V/div, DC Output Voltage 1 V/div, DC**  **Inductor Current 1 A/div, DC**  **Voltage at L2 2 V/div, DC**  **TPS63020 VIN = 4.2 V, VOUT = 3.3 V, RL = 2.2**   **Time 100** **s/div**  **Figure 27. Start-up Behavior from Rising Enable, TPS63020** |

#### System Examples

##### Improved Transient Response for 2 A Load Current

Capacitor C4 and resistor R4 are added for improved load transient performance.

L1

1 µH

2.5 V



VIN

to 5.5 V

VOUT

3.3 V at 2 A

R4

68 kfi

C1

2×10 µF

R1

1 Mfi

C2

4×22 µF

C4 R3

4.7 pF 1 Mfi

R2

180 kfi

Power Good

C3

100 nF

PGND

GND

PG

VINA

EN

PS/SYNC

FB

VIN VOUT

TPS63020

L2

L1

**Figure 28. Application Circuit for 2 A Load Current**

#### System Examples (continued)

##### Supercapacitor Backup Power Supply With Active Cell Balancing

The TPS63020 can be used to charge backup capacitors to a user-defined voltage level while the main power supply is supplying a system, and discharges these capacitors into the system when the main power supply is interrupted. With this design, the system voltage during backup operation keeps constant independent of the voltage reduction on the backup capacitors. Refer to the [*PMP9766 Test Results Application Report*](http://www.ti.com/lit/pdf/SLVA726)for more details.

Normal operation



Main power

Reverse

blocking

System

Pre-charge

operation

Charge operation

**TPS63020**

+

Backup operation

Backup

+ Capacitor

Active Cell Balancing

Main power

System



##### Figure 29. Simplified Block Diagram of a Backup Power System

* + 1. **Low-Power TEC Driver**

Controlling the operating temperature of electronic circuits helps attain the best system performance. For passive control, that is, when heat sinks is not giving the right performance, active cooling using a thermoelectric cooler (TEC) might be able to solve the thermal issue. [Figure 30](#_bookmark56) shows an example driving such a TEC element with the TPS63020. Refer to the [*Low-power TEC Driver Application Report*](http://www.ti.com/lit/pdf/SLVA677).



TEC

V

IN

TPS63020

V

CTRL

**Figure 30. Low-Power TEC Driver Schematic**

### Power Supply Recommendations

The TPS6302x devices have no special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TPS6302x.

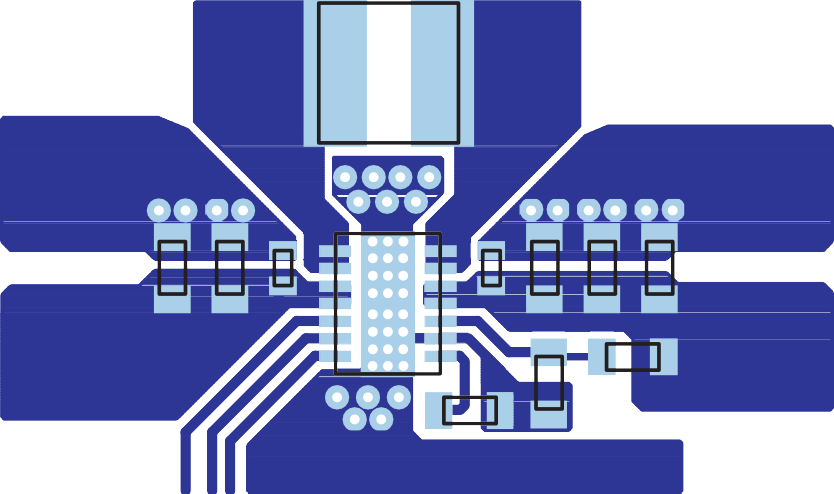
### Layout

#### Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. Place the input capacitor, output capacitor, and the inductor as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider must be placed as close as possible to the control ground pin of the IC. To lay out the control ground, short traces are recommended as well, separation from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

#### Layout Example



L1

**GND**

**GND**

C1 C2

U1

**VIN**

**VOUT**

R2

R1

**GND**

C3

**Figure 31. PCB Layout Suggestion**

EN PS/SYNC

PG

#### Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power- dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

* Improving the power dissipation capability of the PCB design
* Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
* Introducing airflow in the system

Refer to the [*Thermal Characteristics Application Note*](http://www.ti.com/lit/pdf/SZZA017) and the [*Semiconductor and IC Package Thermal Metrics*](http://www.ti.com/lit/pdf/SPRA953)[*Application Note*](http://www.ti.com/lit/pdf/SPRA953) for more details on how to use the thermal parameters.

### Device and Documentation Support

#### Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### Device Support

##### Custom Design with WEBENCH Tools

[Click here](https://webench.ti.com/wb5/WBTablet/PartDesigner/quickview.jsp?base_pn=TPS63021&origin=PDF_DS%3Flitpdf%3Dslvs916&litsection=device_support) to create a custom design using the TPS63021 device with the WEBENCH® Power Designer.

1. Start by entering your VIN, VOUT and IOUT requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   * Run electrical simulations to see important waveforms and circuit performance,
   * Run thermal simulations to understand the thermal performance of your board,
   * Export your customized schematic and layout into popular CAD formats,
   * Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at [www.ti.com/webench](http://www.ti.com/lsds/ti/analog/webench/overview.page?DCMP=sva_web_webdesigncntr_en&HQS=sva-web-webdesigncntr-vanity-lp-en).

##### Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### Documentation Support

##### Related Documentation

For related documentation see the following:

* Texas Instruments, [*Thermal Characteristics Application Note*](http://www.ti.com/lit/pdf/SZZA017)
* Texas Instruments, [*IC Package Thermal Metrics Application Note*](http://www.ti.com/lit/pdf/SPRA953)

#### Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 6. Related Links**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **PARTS** | **PRODUCT FOLDER** | **SAMPLE & BUY** | **TECHNICAL DOCUMENTS** | **TOOLS & SOFTWARE** | **SUPPORT & COMMUNITY** |
| TPS63020 | [Click here](http://www.ti.com/product/TPS63020?dcmp=dsproject&hqs=pf) | [Click here](http://www.ti.com/product/TPS63020?dcmp=dsproject&hqs=sandbuy&&samplebuy) | [Click here](http://www.ti.com/product/TPS63020?dcmp=dsproject&hqs=td&&doctype2) | [Click here](http://www.ti.com/product/TPS63020?dcmp=dsproject&hqs=sw&&desKit) | [Click here](http://www.ti.com/product/TPS63020?dcmp=dsproject&hqs=support&&community) |
| TPS63021 | [Click here](http://www.ti.com/product/TPS63021?dcmp=dsproject&hqs=pf) | [Click here](http://www.ti.com/product/TPS63021?dcmp=dsproject&hqs=sandbuy&&samplebuy) | [Click here](http://www.ti.com/product/TPS63021?dcmp=dsproject&hqs=td&&doctype2) | [Click here](http://www.ti.com/product/TPS63021?dcmp=dsproject&hqs=sw&&desKit) | [Click here](http://www.ti.com/product/TPS63021?dcmp=dsproject&hqs=support&&community) |

#### Support Resources

[TI E2E™ support forums](http://e2e.ti.com/) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](http://www.ti.com/corp/docs/legal/termsofuse.shtml).

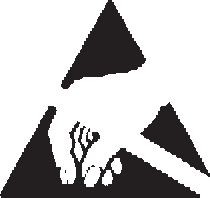
#### Trademarks

E2E is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

#### Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### Glossary

[SLYZ022](http://www.ti.com/lit/pdf/SLYZ022) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

### Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGE OPTION ADDENDUM**

[www.ti.com](http://www.ti.com/) 10-Dec-2020

#### PACKAGING INFORMATION

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Orderable Device** | **Status**  (1) | **Package Type** | **Package Drawing** | **Pins** | **Package Qty** | **Eco Plan**  (2) | **Lead finish/ Ball material**  (6) | **MSL Peak Temp**  (3) | **Op Temp (°C)** | **Device Marking**  (4/5) | **Samples** |
| TPS63020DSJR | ACTIVE | VSON | DSJ | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PS63020 |  |
| TPS63020DSJT | ACTIVE | VSON | DSJ | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PS63020 |  |
| TPS63021DSJR | ACTIVE | VSON | DSJ | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PS63021 |  |
| TPS63021DSJT | ACTIVE | VSON | DSJ | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PS63021 |  |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

Addendum-Page 1

## PACKAGE OPTION ADDENDUM

[www.ti.com](http://www.ti.com/) 10-Dec-2020

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS63020 :**

* Automotive: [TPS63020-Q1](http://focus.ti.com/docs/prod/folders/print/tps63020-q1.html)

NOTE: Qualified Version Definitions:

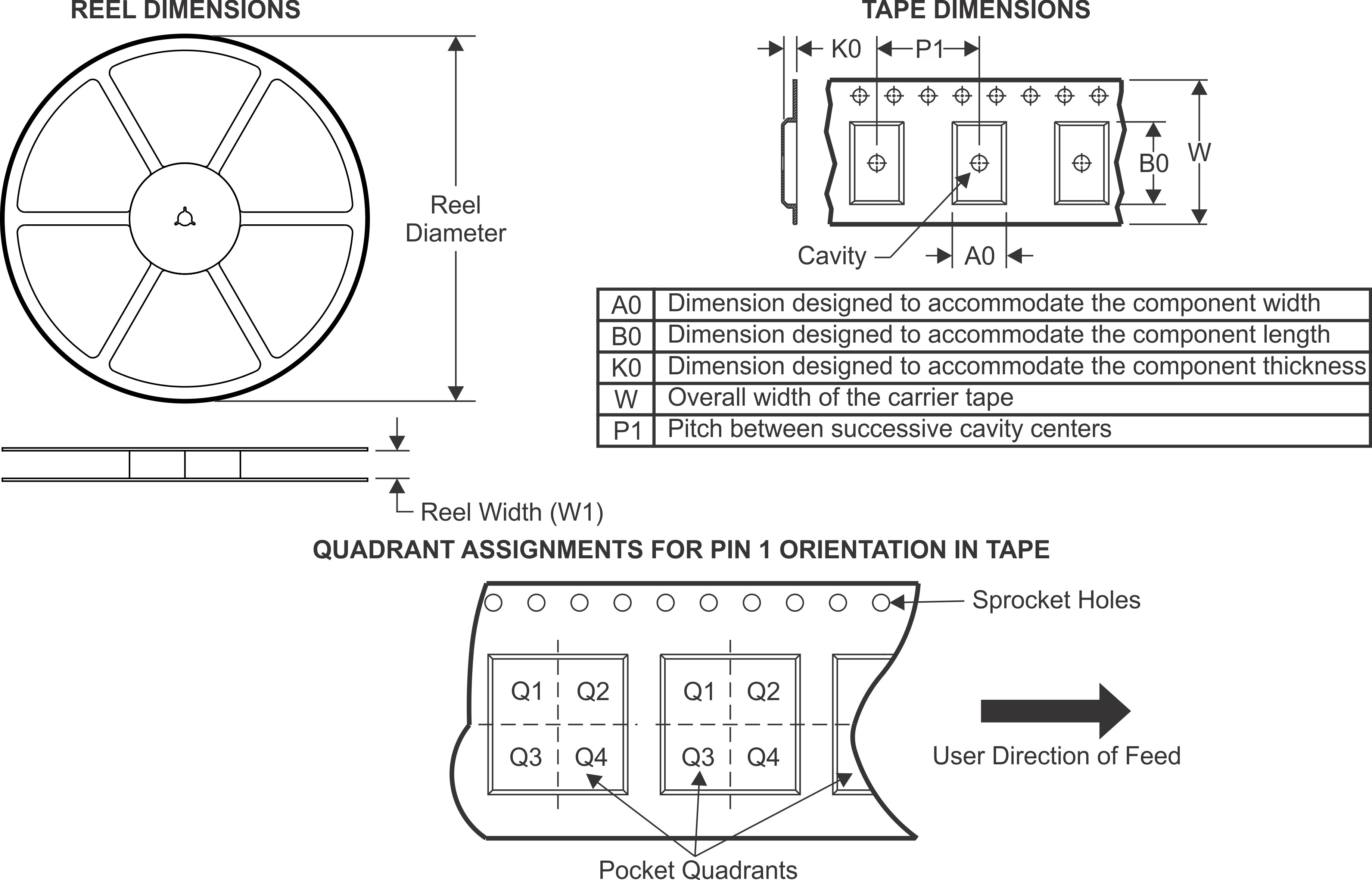
* Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

Addendum-Page 2

## PACKAGE MATERIALS INFORMATION

[www.ti.com](http://www.ti.com/) 16-Oct-2020

#### TAPE AND REEL INFORMATION



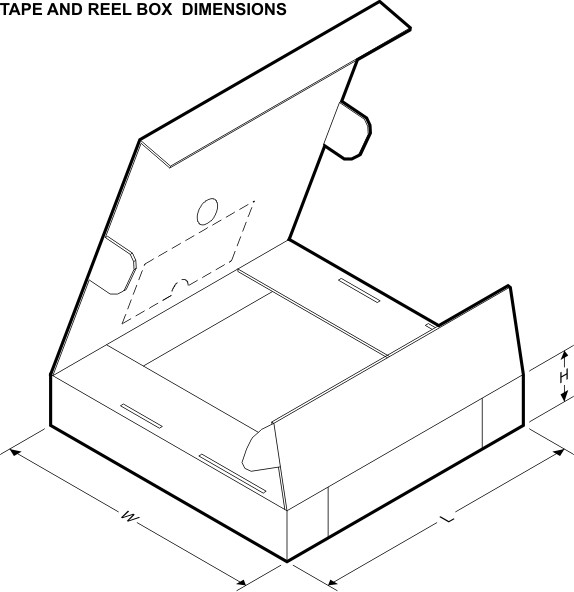
\*All dimensions are nominal

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Device** | **Package Type** | **Package Drawing** | **Pins** | **SPQ** | **Reel Diameter (mm)** | **Reel Width W1 (mm)** | **A0**  **(mm)** | **B0**  **(mm)** | **K0**  **(mm)** | **P1**  **(mm)** | **W**  **(mm)** | **Pin1 Quadrant** |
| TPS63020DSJR | VSON | DSJ | 14 | 3000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS63020DSJR | VSON | DSJ | 14 | 3000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS63020DSJT | VSON | DSJ | 14 | 250 | 180.0 | 12.5 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS63021DSJR | VSON | DSJ | 14 | 3000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS63021DSJR | VSON | DSJ | 14 | 3000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS63021DSJT | VSON | DSJ | 14 | 250 | 180.0 | 12.5 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS63021DSJT | VSON | DSJ | 14 | 250 | 180.0 | 12.4 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |

Pack Materials-Page 1

## PACKAGE MATERIALS INFORMATION

[www.ti.com](http://www.ti.com/) 16-Oct-2020

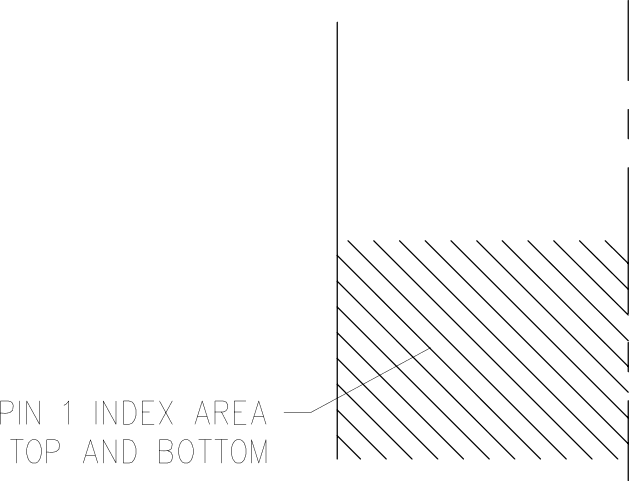


\*All dimensions are nominal

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Device** | **Package Type** | **Package Drawing** | **Pins** | **SPQ** | **Length (mm)** | **Width (mm)** | **Height (mm)** |
| TPS63020DSJR | VSON | DSJ | 14 | 3000 | 338.0 | 355.0 | 50.0 |
| TPS63020DSJR | VSON | DSJ | 14 | 3000 | 853.0 | 449.0 | 35.0 |
| TPS63020DSJT | VSON | DSJ | 14 | 250 | 205.0 | 200.0 | 33.0 |
| TPS63021DSJR | VSON | DSJ | 14 | 3000 | 338.0 | 355.0 | 50.0 |
| TPS63021DSJR | VSON | DSJ | 14 | 3000 | 853.0 | 449.0 | 35.0 |
| TPS63021DSJT | VSON | DSJ | 14 | 250 | 205.0 | 200.0 | 33.0 |
| TPS63021DSJT | VSON | DSJ | 14 | 250 | 210.0 | 185.0 | 35.0 |

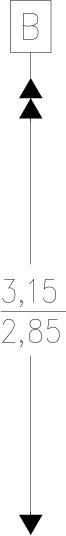
Pack Materials-Page 2

# MECHANICAL DATA



PLASTIC SM ALL OU TL N

0— READ



4,15

0, 20 PER.

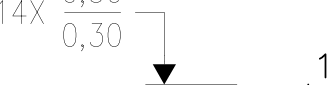
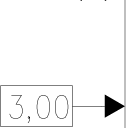
SLATIN PLAN

7

SIZE AND SHAPE W ON PARATE

4208212- /C 06/11

NOTES: A.



B.

C.

D.

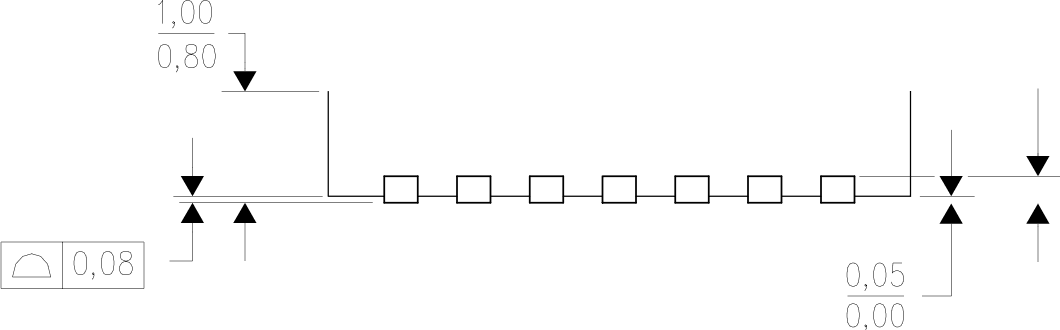
E.

All lineor dimensions ore in millimeters. Dimensioning ond toleroncing per ASME Y14.5M—1994. This drawing is subject to chonge without notice.

Quod Flatpock, No—Leads (QFN) pockoge configuration.

The package thermal pod must be soldered to the boord for thereof ond mechonicol performonce.

See the odditionol figure in the Product Do to Sheet for detoils regarding the exposed thermol pod feotures ond dimensions.



UMEN



INS

[www.ti.com](http://www.ti.com/)

THERMAL PAD MECHANICAL DATA

DSJ (R— PVSON — N14)

# PLASTIC SMALL OUTLINE NO—LEAD



THERMAL INFORMATION

This package incorporates on exposed thermal pod thot is designed to be attached directly to on external heotsink. The thermal pod must be soldered directly to the printed circuit board (PCB). After soldering, the

PCB con be used as a heotsink. In addition, through the use of thermal vios, the thermal pod con be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, con be attached to a special heotsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (Ic).

For information on the Quad Flotpock No—Lead (DFN) package and its advantages, refer to Application Report, DFN/S0N PCB Attachment, Texas Instruments Literature No. [SLUA271.](http://www.ti.com/lit/slua271) This document is available at w\¥w.ti.com.

The exposed thermal pod dimensions for this package ore shown in the following illustration.

Exposed Thermal Pod

1

7

1,5860,10

4X 0,20

14

8

2,8560,10 —+

Bottom View

Exposed Thermal Pod Dimensions

4208549—3/G 04/15

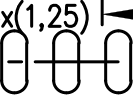
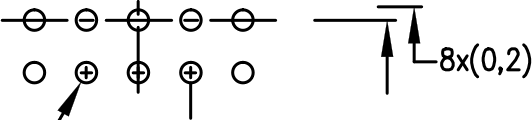
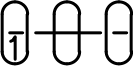
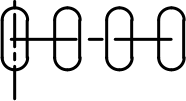
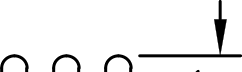
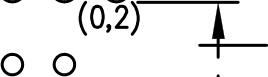
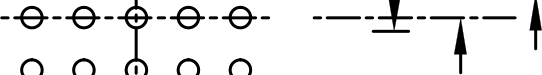
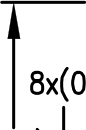
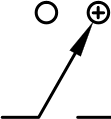
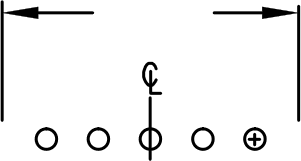
NOTE: All linear dimensions ore in millimeters



LAND PATTERN DATA

DSJ (R— PVSON— N14)

PLASTIC SMALL OUTLINE NO—LE AD



IJOTES: A. B.



Exemple Board Loyout

Example Stencil Design 0.125mm Stencil Thickness (Note D)

Note C

(R0,12)WP.

Exposed uetol

1iñ

4x(0,23)

0 0 @ O O

(2,8) —- -.@.-.@.- -.@.-.@.- -—

8x(0,2)

(2,8)

(4x0,46)

—-

1,25)

4x(0,66)

! !

14x(0,24)

solder coveroge by printed on center thermal pod

Example Via Layout Design vary depending on constraints

(Note C, E)

-

(4,4)

(2,85)

0,5)TrP.

4210895—2/E 02/16

AII lineor dimensions are in millimeters.

This drawing i9 9ubject to change without notice.

* 1. This package is designed to be soldered to o thermal pad on the board. Refer to Application Note, Quod Flot—Pack

Packages, Texas Instruments Literature Flo. [SCBAO17,](http://www.ti.com/lit/SCBA017) [SLUA271,](http://www.ti.com/lit/SLUA271) ond also the Product Data Sheets

for specific thermal information, via requirements, ond recommended board loyout. Thèse documents are ovoiloble at

WWw.ti.COM [http: //wWW.ti.COM>.](http://wWW.ti.COM/)

* 1. Loser cutting opertures with tropezoidal walls ond also roundinq corners will offer better poste release. Customers should contact their board assemblé site for stencil design recommendotions. Refer to IPC 7525 for stencil design considérations.
  2. Customers should contact their board fabrication site for minimum solder mosk web tolérances between signal pads.

TEXAS



-

INSTRUMENTS

[**www.ti.com**](http://www.ti.com/)

##### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://www.ti.com/) or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2020, Texas Instruments Incorporated