TÜRK-ALMAN ÜNİVERSİTESİ
TÜRKISCH-DEUTSCHE UNIVERSITÄT

ETE606 Digital Design II

Term Project Assignment

2023 - 2024

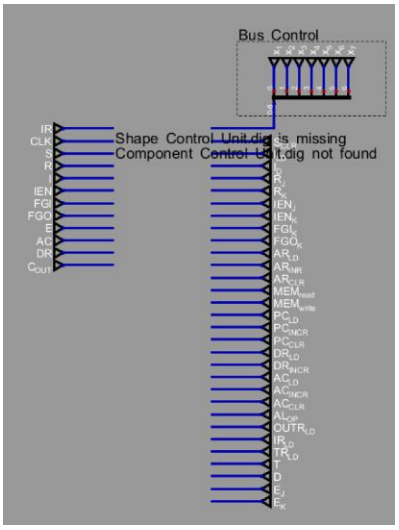
Introduction

This term project involves the design of the **Control Unit** of the theoretical **Mano Computer** as presented in **Chapter 5** of our textbook.

The design will be realized and simulated in the **Digital** simulation tool as we usually use for homeworks and classroom examples (https://github.com/hneemann/Digital).

You are given the following:

1. The datapath of the **Mano Computer** as we studied in our lectures, fully compliant with the description in **Chapter 5**. Unzip the contents of the **Datapath.rar** to a folder and run the file named **Full Picture v1.dig**. Note that you will have an error message near the **Control Unit** as follows:



This is because the **Control Unit.dig** is deleted and excluded from the folder. This file is what you have to create from scratch, and plug in to this area.

2. The **Test Cases** that you need to use to verify the correctness of your design. They are embedded in the file **Full Picture v1.dig**.

3. The computer description in **Chapter 5** of the textbook.

Expected Project Deliverables

1. A running circuit (**.dig**) file in simulatable form, including the Test Cases running successfully.

2. A written project document covering the following details:
   - Design assumptions
   - Design approach
   - Solution Block Diagram
   - Summary of results
   - Lessons learned

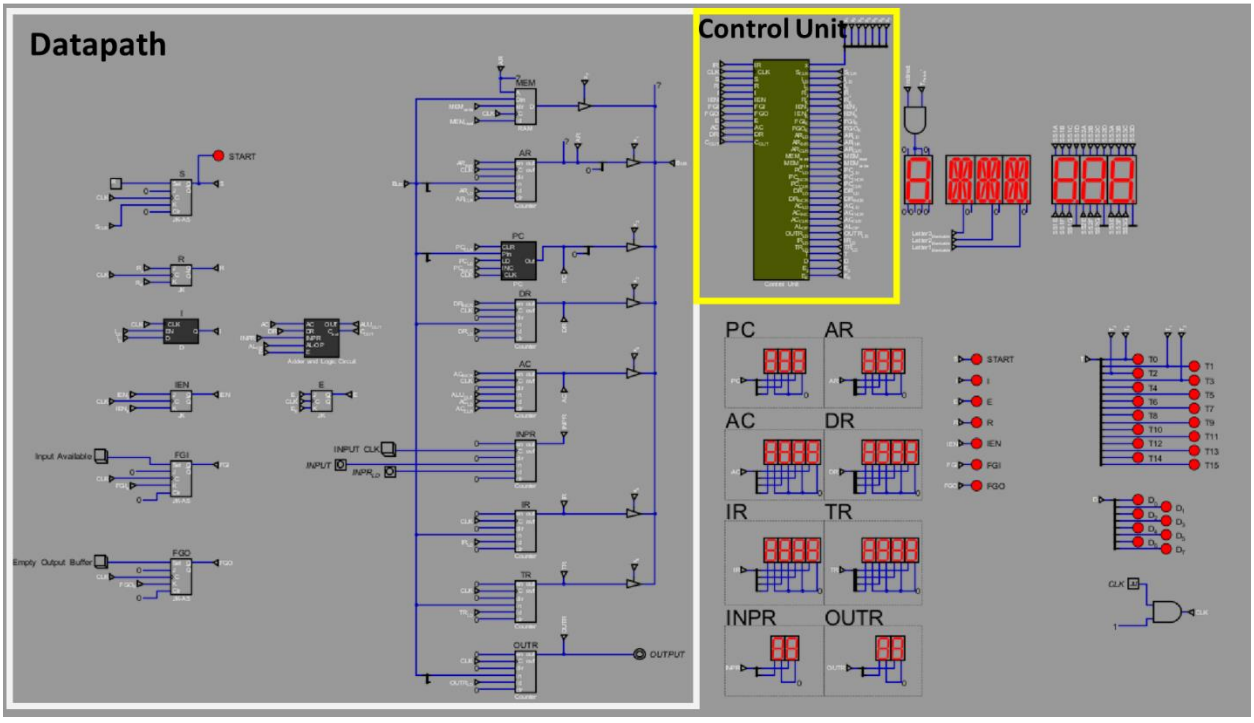


Figure 1: The Datapath and Control Unit

Suggested Approach and Block Diagram

The overall solution approach should follow Figure 1. The design should be composed of a Control Unit and a Data Path, with signals in between.

Figure 2: General approach to design

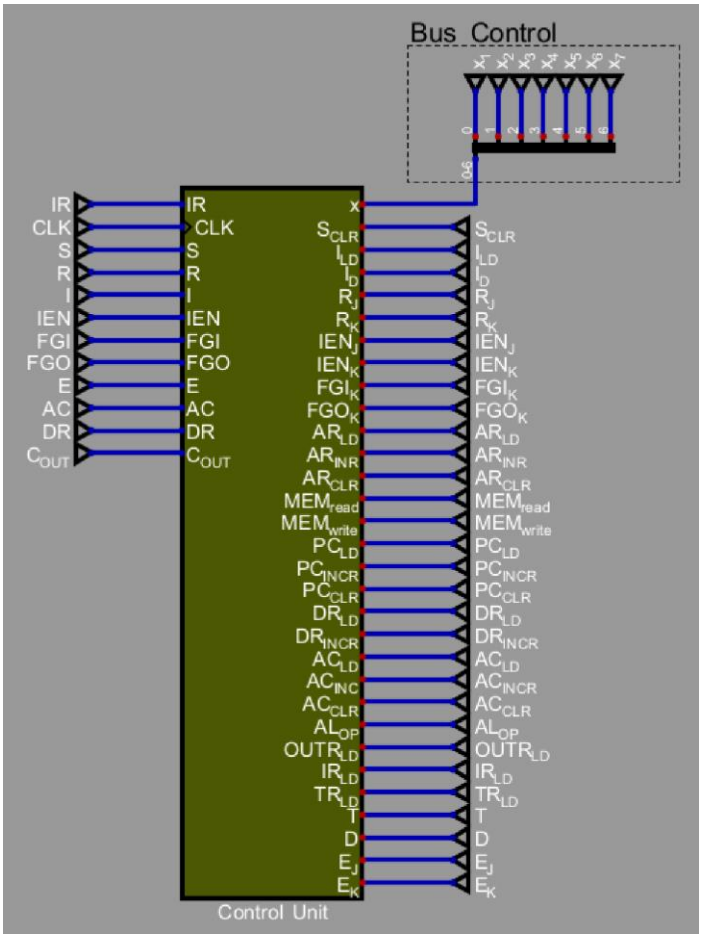


Figure 3: Inputs and outputs of the Control Unit

Assumptions/Facts

- The **Sequence Counter** (**SC**) is inside the Control Unit.
- The **AL_{OP}** control signal to be produced by the Control Unit is a 7-bit signal that describes the operation to be performed by the **Adder and Logic Circuit**. Its format is as follows:

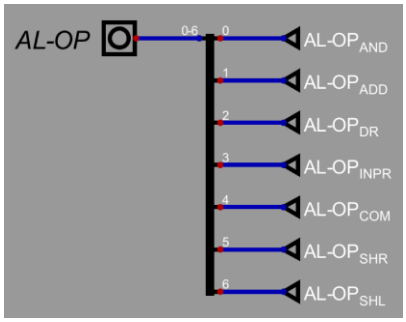


Figure 4:The format of the AL-OP signal

You should ensure that at a given time, only 1 bit of the **AL-OP** should be **1** and the rest **0**. Otherwise, the **Adder and Logic Circuit** may be confused on what operation to perform.

- Interpret the **Control Unit** output signal names as follows:
  - **REG_{LD}**: Parallel Load input of the particular register REG
  - **REG_{INC}**: Increment input of the register
  - **REG_{CLR}**: Clear input of the register

- Some status bits are implemented as **JK Flip Flops**. In such cases, there are two control signals produced for the **J** and **K** inputs of the Flip Flop. Example: **R_J**, **R_K**, **E_J**, **E_K**.

Test Cases

There are one or more test cases per each computer instruction. In the case of **Memory Reference** instructions, the **Direct** and **Indirect** address cases are tested separately. For **SKIP** type of instructions, there are two test cases, one for the **THEN** scenario, and one for the **ELSE** scenario.

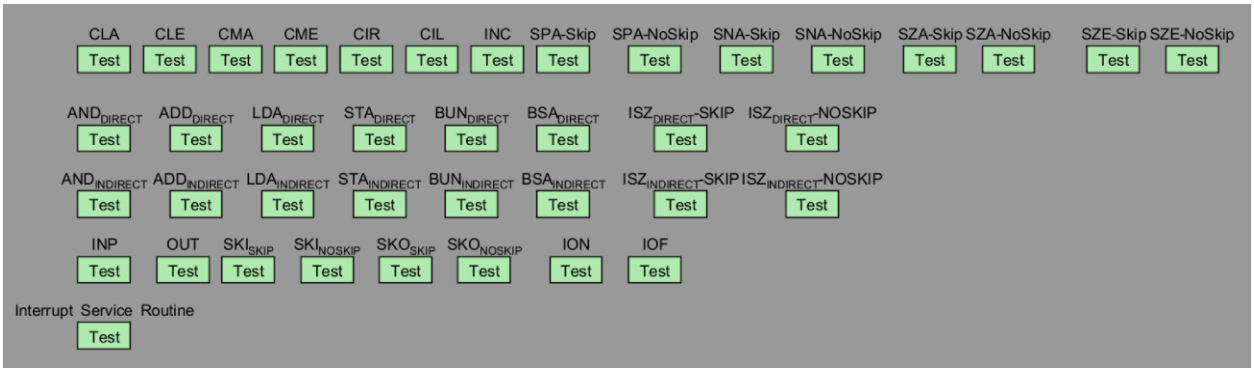


Figure 5: Test Cases

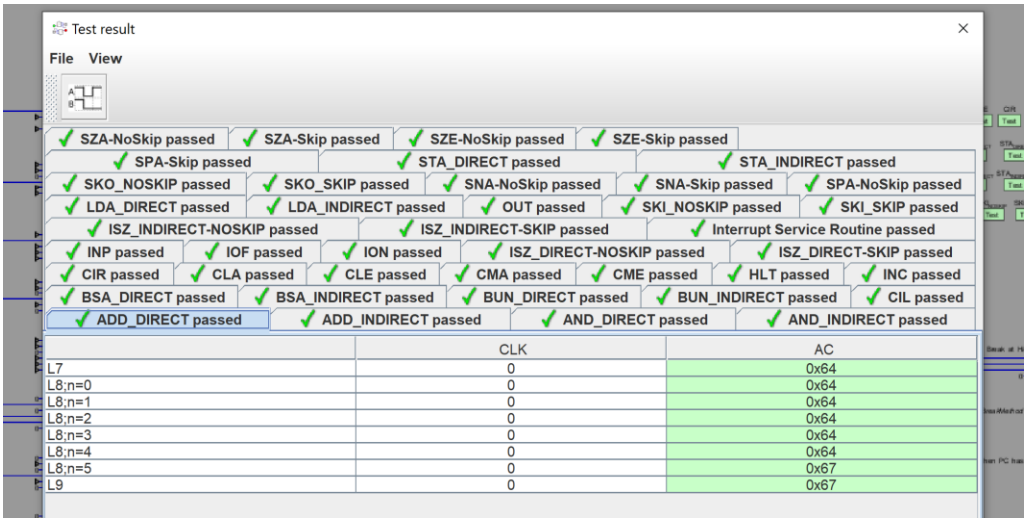


Figure 6: Test case execution results

Example Test Case 1

TEST CASE: CMA

```
                    CLK         AC

init S=1; #Start computer
init AC=0xF0F0;       #Prepare AC
program(0x7200)       #CMA register instruction

repeat(4)             C           X
                      0           0x0F0F
```

1. Initialize the **S** flag and the **AC** register

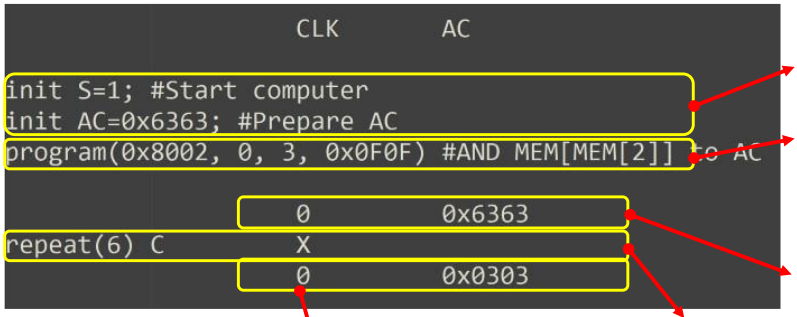
2. The **RAM** should contain the instruction to be tested (**CMA**) at address 0.

3. Give the computer **4 Clock cycles** for the instruction to execute:
T_0, T_1, T_2: Fetch and decode
T_3: Execute the **CMA** instruction

4. Observe the expected result in the **AC** register

Example Test Case 2

TEST CASE: $AND_{INDIRECT}$ 0x002



1. Initialize the **S** flag and the **AC** register

2. The **RAM** should contain the instruction to be tested (**$AND_{INDIRECT}$ 2**) at address 0. Note that we set **M[2] = 3** This means the real operand is in **M[3]**, which we set as **0x0F0F**

3. Before any Clock cycles, make sure AC contains desired initial value.

4. Give the computer **6 Clock cycles** for the instruction to execute:
- **T_0, T_1, T_2**: Fetch and decode
- **T_3**: **AR <- M[AR]** to fetch the indirect operand
- **T_4, T_5**: Execute instruction (see page 146 in textbook)

5. Observe the expected result in the **AC** register

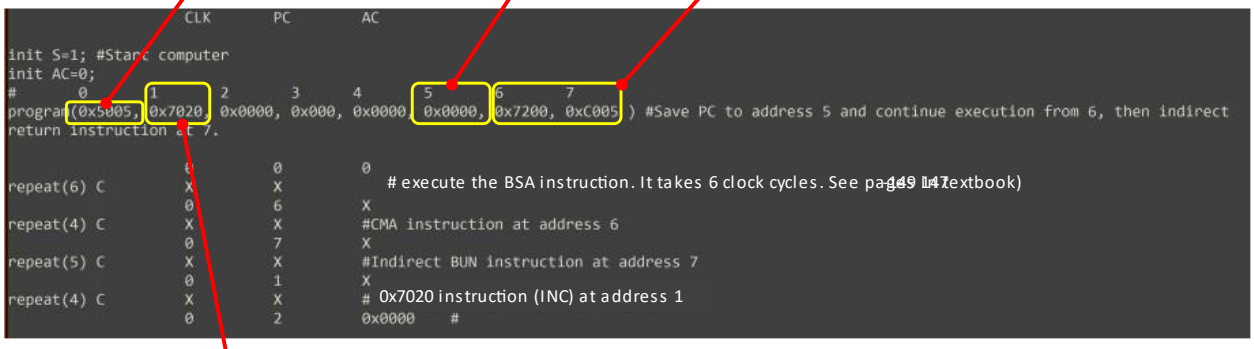
Example Test Case 3

TEST CASE: BSA 0x005

1. Instruction **BSA 0x005**

2. PC will be saved here

3. This is the subroutine body. It ends with instruction **$BUN_{INDIRECT}$ 0x005** located at **M[7]**



4. After returning from the subroutine, program execution continues from this address.

Project Evaluation

As we did in Digital Design I, the evaluation of your project deliverables and results will be in the form of a 1-to-1 15-minute interview. During the interview, you will be expected to explain your approach, demonstrate working results and answer any questions.

Evaluation Criteria

Full Score

1. Student fluently demonstrates a working simulation that meets all the test cases embedded in the provided model.
2. Student can answer all the questions on the design approach, progression and implementation details.
3. The design is unique and not copied from another student.
4. Design report is available.
5. Project was submitted before deadline.

Half Score

1. Student demonstrates a working simulation that realizes a basic subset of the test cases provided.
2. Student can answer all the questions on the design approach and details, including the problems that caused the design to be incomplete.
3. The design is unique and not copied from another student.
4. Project was submitted before deadline.

Lower Score

1. There is no end-to-end test case working, however subsets of the block diagram can be demonstrated to work.
2. Student can answer all the questions on the design approach and details, including the problems that caused the design to be incomplete.
3. The design is unique and not copied from another student.
4. Project was submitted before deadline.

Zero

ZERO SCORE DETECTOR