

Quiz #3

- Due Apr 21 at 11:59pm
- Points 10
- Questions 10
- Available Apr 19 at 12:01am - Apr 21 at 11:59pm
- Time Limit 60 Minutes

Instructions

Welcome to the Week #3 quiz!

This is due Sunday night at 23:59. Canvas is very unforgiving, so don't push it.

Remember that this is open-notes. Good luck!

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	5 minutes	9 out of 10

❗ Correct answers will be available on Apr 22 at 12:01am.

Score for this quiz: 9 out of 10

Submitted Apr 21 at 9:52pm

This attempt took 5 minutes.



Question 1

1 / 1 pts

Why did "Moore's Law of Clock Speed" stop happening a few years ago?

- ☐ Because Moore's Law of Transistor Density stopped holding then too
- ☒ Because it would have resulted in way too much power consumption and require too much heat dissipation
- ☐ Because CPU clocks could no longer be made to run that fast
- ☐ Because connection lines on CPU chips could no longer be made that thin



Question 2

1 / 1 pts

The difference between L1 and L2 cache is

- ☒ L1 is smaller and faster than L2
- ☐ L2 has two banks of memory, L1 only has one

- ☐ Nothing -- they are two terms for the same thing
- ☐ L1 is larger and slower than L2



Question 3

1 / 1 pts

Why is there a photo of a carton of eggs in the Cache notes?

- ☐ Because caches are easily broken
- ☐ Andy Warhol would have appreciated it this way
- ☒ Bringing home a dozen eggs when you only need 2 today is like the need for cache
- ☐ No logical reason -- it looks cool



Question 4

1 / 1 pts

Caches are at their very best when your code takes advantage of

- ☐ Singular and Temporary coherence
- ☒ Spatial and Temporal coherence
- ☐ Spatial and Temporary coherence
- ☐ Singular and Temporal coherence



Question 5

1 / 1 pts

When adding up the elements of a 2D array in C or C++, it is faster to add the elements:

- ☒ Horizontally (i.e., across the rows) first
- ☐ Vertically (i.e., down the columns) first
- ☐ It makes no speed difference either way



Question 6

1 / 1 pts

In terms of 32-bit (4-byte) floating-point numbers, the size of a cache line is:

- ☐ 8 floating-point numbers
- ☐ 64 floating-point numbers
- ☐ 32 floating-point numbers
- ☒ 16 floating-point numbers



Question 7

1 / 1 pts

MESI stands for:

- ☐ Modified-Exclusive-Shared-Instructions
- ☐ Multicore-Exclusive-Shared-Invalid
- ☐ Nothing, it is someone's name
- ☒ Modified-Exclusive-Shared-Invalid
- ☐ Modified-Exterior-Shared-Invalid
- ☐ Modified-Exclusive-Single-Invalid



Question 8

1 / 1 pts

False Sharing happens because:

- ☐ More than two threads are trying to read from the same cache line
- ☐ Two threads are not sharing the same cache line, but should be
- ☐ Two threads are reading from the same cache line
- ☒ One thread is accessing the same cache line that another thread is writing to



IncorrectQuestion 9

0 / 1 pts

Intel recently achieved a remarkably-high CPU clock speed by:

- ☐ Running the CPU outside
- ☐ Cooling the chip with four fans
- ☒ Cooling the chip with liquid nitrogen
- ☐ Cooling the chip with liquid helium



Question 10

1 / 1 pts

When performing a matrix multiply:

- ☐ The order of the i-j-k for-loops makes a slight difference in performance
- ☒ The order of the i-j-k for-loops makes a big difference in performance
- ☐ The order of the i-j-k for-loops makes no difference in performance

Quiz Score: 9 out of 10