
CMOS Active Filters

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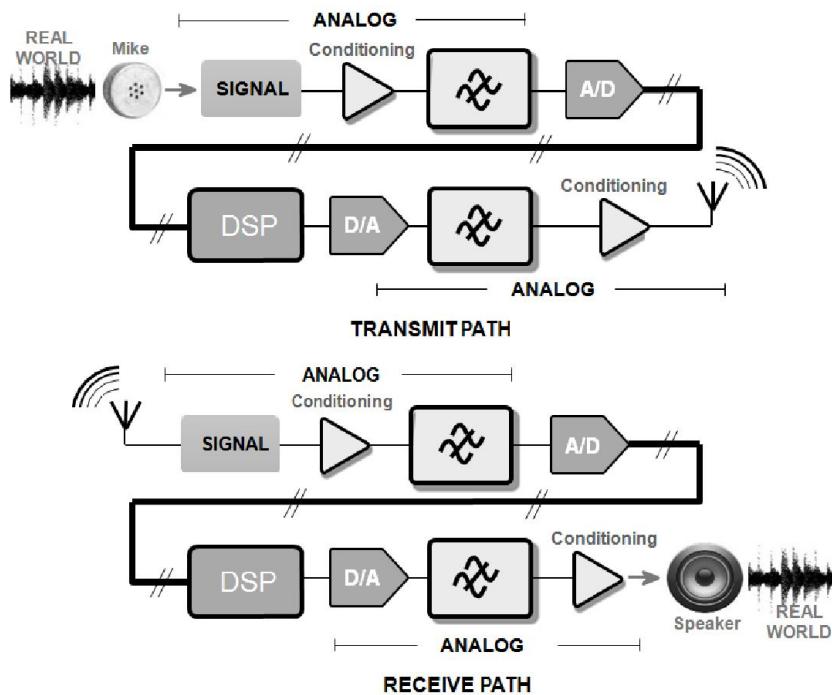
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Filtering

- Task of filters: suppress unwanted signals, change the behavior (amplitude and/or phase) of the wanted ones.
- *Analog filters*: process physical signals, limited accuracy, stability and resolution. Simple structure.
- *Digital filters*: processes numbers only. Highly accurate, stable, extremely high resolution and accuracy possible. Complex structure. Need data conversion to interface with the physical world.

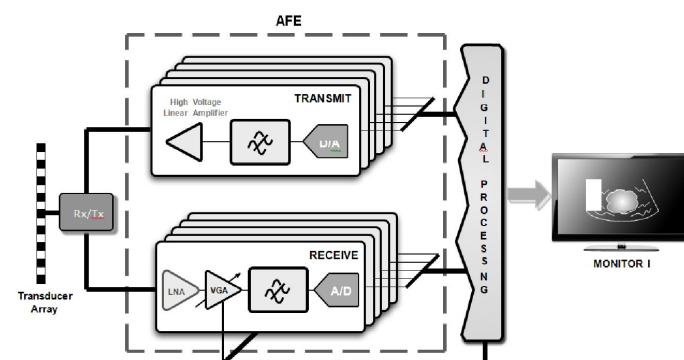
Filtering Examples

- Audio transceiver:



From F. Maloberti and G.C. Temes, *CMOS Analog Filter Design*, Wiley, 2015.

- Ultrasonic imager



Task: Transmit section: antialiasing; receive section; suppression of unwanted signals with large dynamic range. Linear phase, low power.

Structure of the Lectures

- Only CMOS integratable filters are discussed;
- Continuous-time CMOS filters;
- Discrete-time switched-capacitor filters (SCFs);
- Non-ideal effects in SCFs;
- Design examples: a Gm-C filter and an SCF;
- The switched-R/MOSFET-C filter.

Classification of Filters

- *Digital filter*: both time and amplitude are quantized.
- *Analog filter*: time may be continuous (CT) or discrete (DT); the amplitude is always continuous (CA).
- Examples of CT/CA filters: active-RC filter, Gm-C filter.
- Examples of DT/CA filters: switched-capacitor filter (SCF), switched-current filter (SIF).
- Digital filters need complex circuitry, data converters.
- CT analog filters are fast, not very linear and inherently inaccurate, may need tuning circuit for controlled response.
- DT/CA filters are linear, accurate, slower.

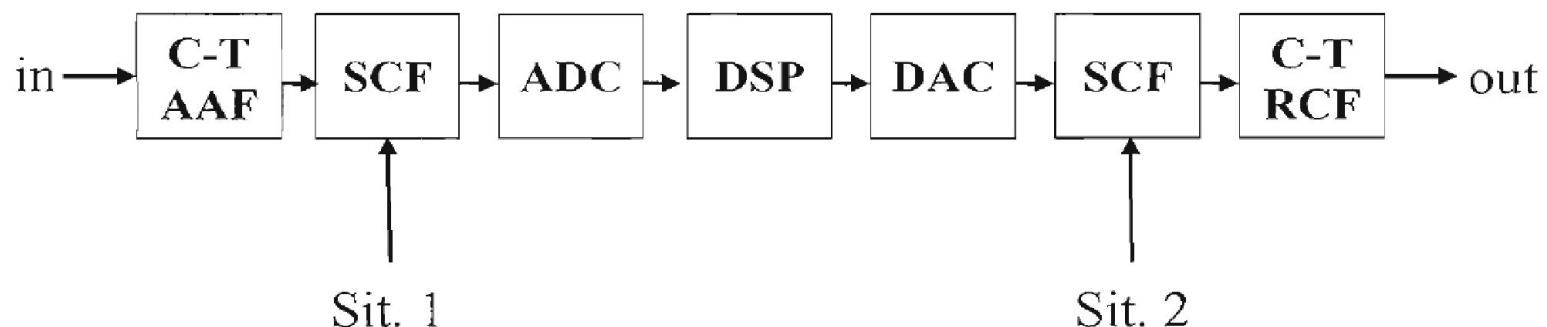
Filter Design

- Steps in design:
 1. *Approximation* – translates the specifications into a realizable rational function of s (for CT filters) or z (for DT filters). May use MATLAB, etc. to obtain Chebyshev, Bessel, etc. response.
 2. *System-level (high-level) implementation* – may use Simulink, etc. Architectural and circuit design should include scaling for impedance level and signal swing.
 3. *Transistor-level implementation* – may use CAD tools (SPICE, Spectre, etc).

These lectures will focus on Step. 2 for CMOS filters.

Mixed-Mode Electronic Systems

- Analog filters are needed to suppress out-of-band noise and prevent aliasing. Also used as channel filters, or as loop filters in PLLs and oversampled ADCs, etc.
- In a mixed-mode system, *continuous-time filter* allows sampling by discrete-time *switched-capacitor filter* (SCF). The SCF performs sharper filtering; following *DSP filtering* may be even sharper.
- In Sit. 1, SCF works as a DT filter; in Sit. 2 it is a CT one.



Frequency Range of Analog Filters

- Discrete active-RC filters: 1 Hz – 100 MHz
- On-chip continuous-time active filters: 10 Hz - 1 GHz
- Switched-capacitor or switched-current filters:
1 Hz – 10 MHz
- Discrete LC: 10 Hz - 1 GHz
- Distributed: 100 MHz – 100 GHz

Accuracy Considerations

- The *absolute* accuracy of on-chip analog components is poor (10% - 50%). The *matching* accuracy of like elements can be much better with careful layout.
- In untuned analog integrated circuits, on-chip R_s can be matched to each other typically within a few %, C_s within 0.05%, with careful layout. The transconductance (G_m) of stages can be matched to about 10 - 30%.
- In an active-RC filter, the time constant T_c is determined by RC products, hence it is accurate to only 20 – 50%. In a G_m -C filter , $T_c \sim C/G_m$, also inaccurate. Tuning may be used to obtain 1 - 5% accuracy.
- In an SC filter, $T_c \sim (C_1/C_2)/f_c$, where f_c is the clock frequency. T_c accuracy may be 0.05% or better!

Design Strategies

- Three basic approaches to analog filter design:
 1. For simple filters (e.g., anti-aliasing or smoothing filters), a *single-opamp stage* may be used.
 2. For more demanding tasks, *cascade design* is often used— splits the transfer function $H(s)$ or $H(z)$ into first and second-order realizable factors, realizes each by buffered filter sections connected in cascade. Simple design and implementation, medium sensitivity and noise.
 3. *Multi-feedback (simulated reactance filter) design.* Complex design and structure, lower noise and sensitivity. Hard to lay out and debug.

Active-RC Filters [1], [4], [5]

- *Single-amplifier filters*: Sallen-Key filter; Kerwin filter; Rauch filter, Delyiannis-Friend filter. Simple structures, but with high sensitivity for high-Q response.
- *Integrator-based filter sections*: Tow-Thomas biquads; Ackerberg-Mossberg filter. 2 or 3 op-amps, lower sensitivity for high-Q. May be cascaded.
- *Cascade design issues*: pole-zero pairing, section ordering, dynamic range optimization. OK passband sensitivities, good stopband rejection.
- *Simulated LC filters*: gyrator-based and integrator-based filters; dynamic range optimization. Low passband sensitivities and noise, but high stopband sensitivity and complexity in design, layout, testing.

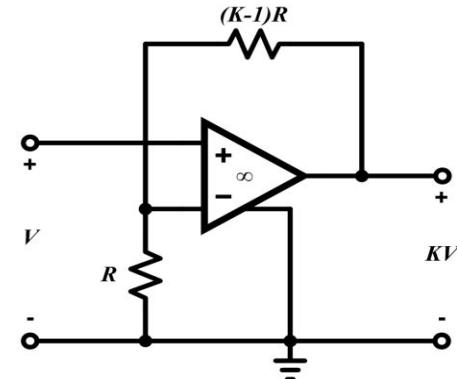
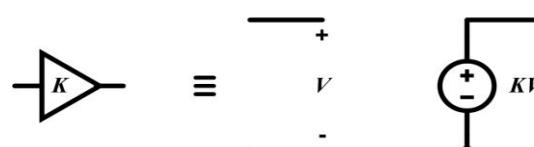
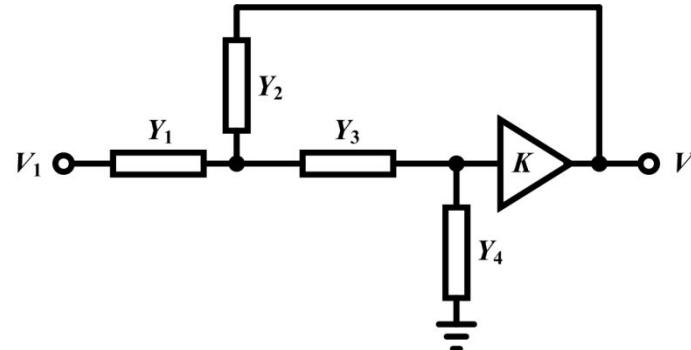
Sallen-Key Filter [1],[4]

First single-opamp biquad. General diagram:

Often, $K = 1$. Has 5 parameters, only 3 specified values.

Scaling or noise reduction possible.

- Realization of active block:



- Amplifier not grounded. Its input common-mode changes with output. Differential implementation difficult.

Sallen-Key Filter

- Transfer function:

$$H(s) = \frac{V_2}{V_1} = \frac{KY_1Y_3}{(Y_1 + Y_2)(Y_3 + Y_4) + Y_3Y_4 - KY_2Y_3}$$

- Second-order transfer function (biquad) if two of the admittances are capacitive. Complex poles are achieved by subtraction of term containing K .
- 3 specified parameters (1 numerator coefficient, 2 denominator coeffs for single-element branches).

Sallen-Key Filter

- Low-pass S-K filter ($R1, C2, R3, C4$):

$$H(s) = \frac{a_0}{b_2 s^2 + b_1 s + b_0}$$

- Highpass S-K filter ($C1, R2, C3, R4$):

$$H(s) = \frac{a_2 s^2}{b_2 s^2 + b_1 s + b_0}$$

- Bandpass S-K filter ($R1, C2, C3, R4$ or $C1, R2, R3, C4$):

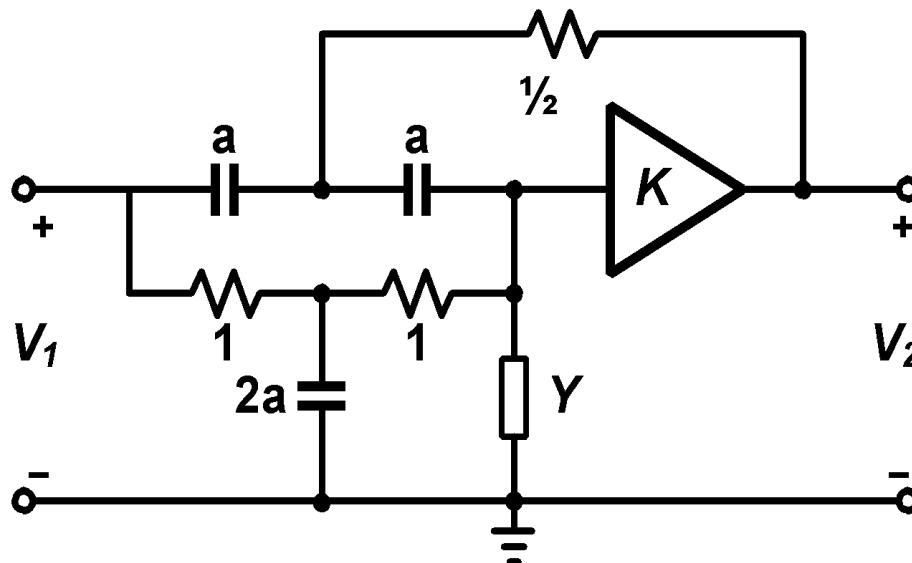
$$H(s) = \frac{a_1 s}{b_2 s^2 + b_1 s + b_0}$$

Sallen-Key Filter

- Pole frequency ω_0 : absolute value of natural mode;
- Pole Q: $\omega_0/2|\text{real part of pole}|$. Determines the stability, sensitivity, and noise gain. $Q > 5$ is dangerous, $Q > 10$ can be lethal! For S-K filter,
 $dQ/Q \sim (3Q - 1) dK/K$. So, if $Q = 10$, 1% error in K results in 30% error in Q.
- Pole Q tends to be high in band-pass filters, so S-K may not be suitable for those.
- Usually, only the peak gain, the Q and the pole frequency ω_0 are specified. There are 2 extra degrees of freedom. May be used for specified R noise, minimum total C, equal capacitors, or $K = 1$.
- Use a differential difference amplifier for differential circuitry.

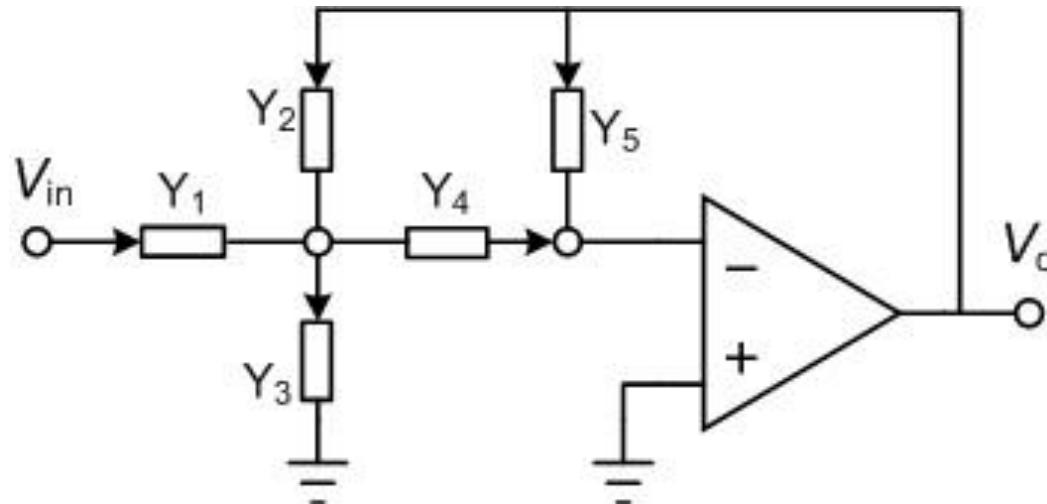
Kerwin Filter

- Sallen-Key filters cannot realize finite imaginary zeros, needed for elliptic or inverse Chebyshev response. Kerwin filter can, with $Y = G$ or sC . For $Y = G$, highpass response; for $Y = sC$, lowpass.



Single-Amplifier Stage

- General single-opamp stage, with grounded opamp, suitable for differential implementation:



Single-Amplifier Stage

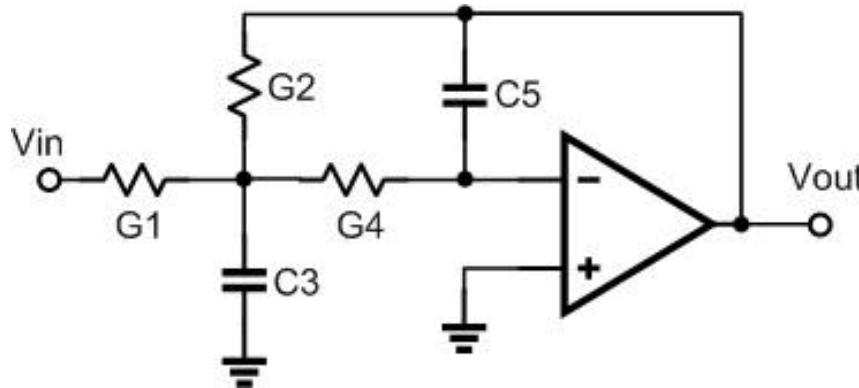
- Transfer function $H(s)$:

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{-Y_1 Y_4}{Y_2 Y_4 + (Y_1 + Y_2 + Y_3 + Y_4) Y_5}$$

- For $Y_1 = G_1$ and $Y_4 = G_4$, Rauch (low-pass) filter; for $Y_1 = G_1$ and $Y_4 = sC_4$, Delyiannis (bandpass) filter. For $Y_1 = sC_1$, $Y_2 = sC_2$ and $Y_4 = sC_4$, high-pass filter results.

Rauch Filter

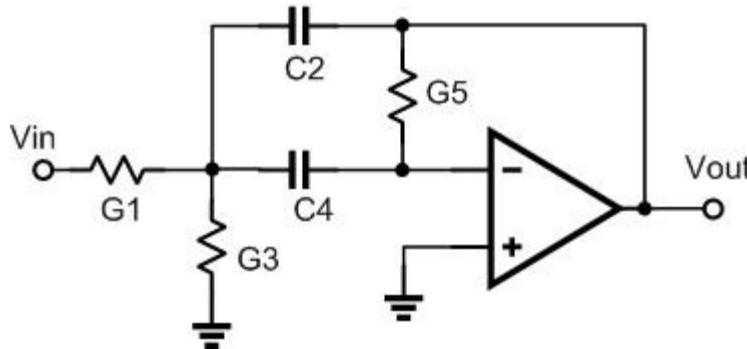
Often applied as anti-aliasing low-pass filter:



- Grounded opamp, may be realized fully differentially. 5 parameters, 3 constraints. Minimum noise, or $C_1 = C_2$, or minimum total C can be achieved.
- Size of resistors limited by thermal ($4kTR$) noise. Smaller resistors, larger capacitors \rightarrow less noise, more power!

Delyiannis-Friend Filter

Single-opamp *bandpass* filter:

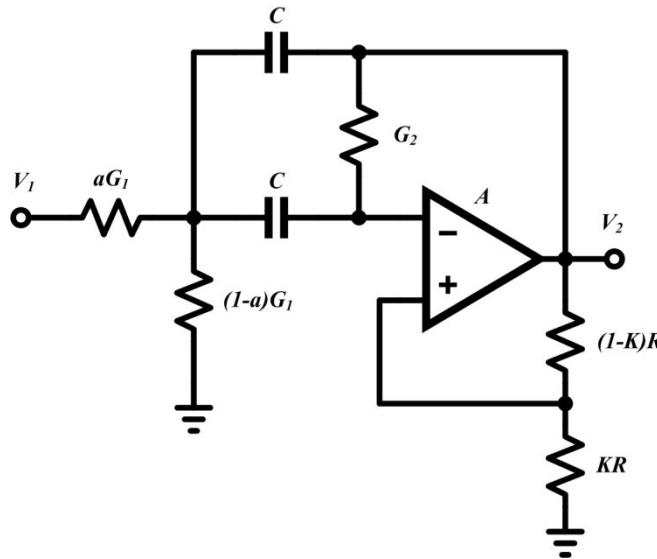


- Grounded opamp, $V_{cm} = 0$. The circuit may be realized in a fully differential form suitable for noise cancellation. Input CM is held at analog ground.
- Finite gain slightly reduces gain factor and Q. Sensitivity is not too high even for high Q.

Delyiannis-Friend Filter

- Q may be enhanced using positive feedback:

$$\text{New } Q = \frac{Q_0}{1 - 2\alpha Q_0^2}$$



- $\alpha = K/(1-K)$
- Opamp no longer grounded, V_{cm} not zero, no easy fully differential realization.

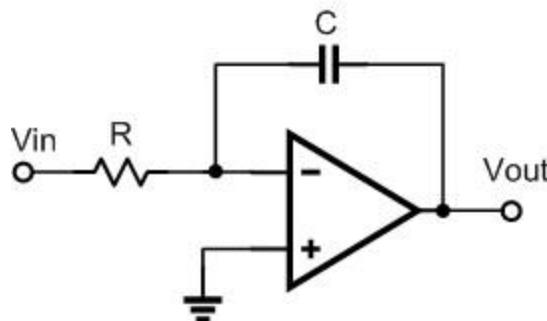
Active-RC Integrator

- Transfer functions:

$$v_{out}(t) = -\frac{1}{RC} \int_{-\infty}^t v_{in}(\tau) d\tau$$

$$H(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = -\frac{1}{j\omega RC}$$

- Circuit:

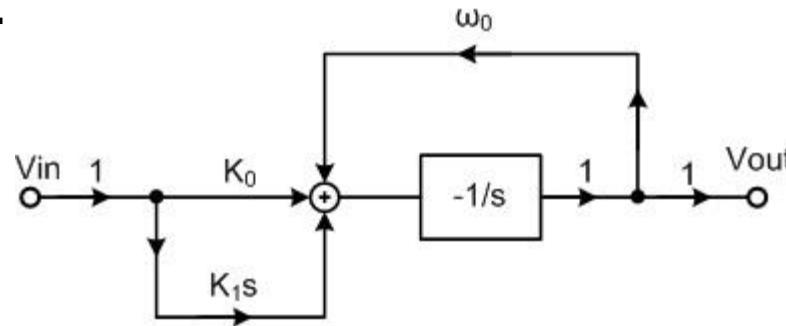


Bilinear Filter Stage

Transfer function:

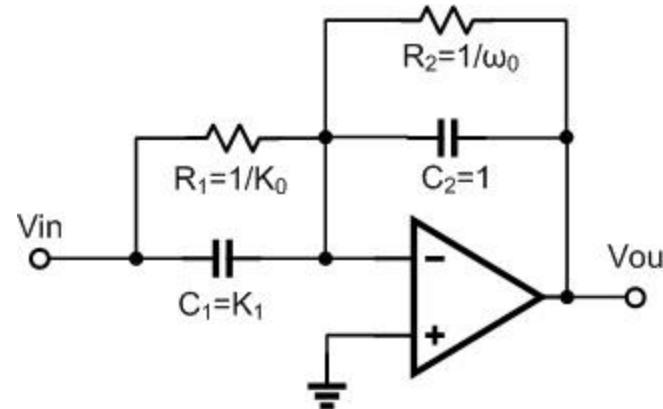
$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{K_1 s + K_0}{s + \omega_0}$$

Block diagram:

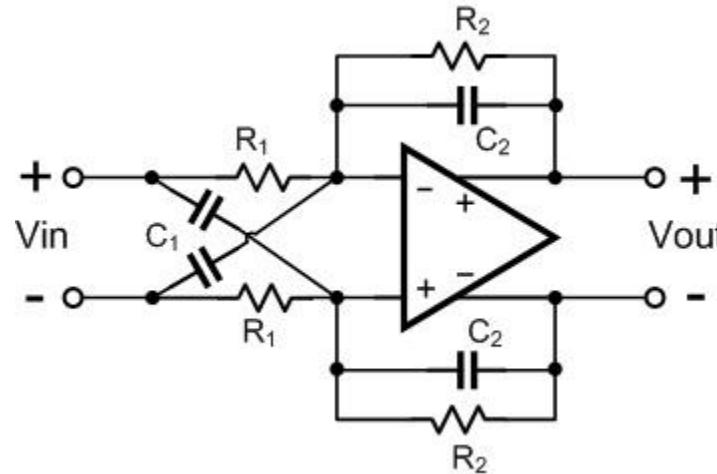


Bilinear Filter Stage

- Circuit diagram:



For positive zero:



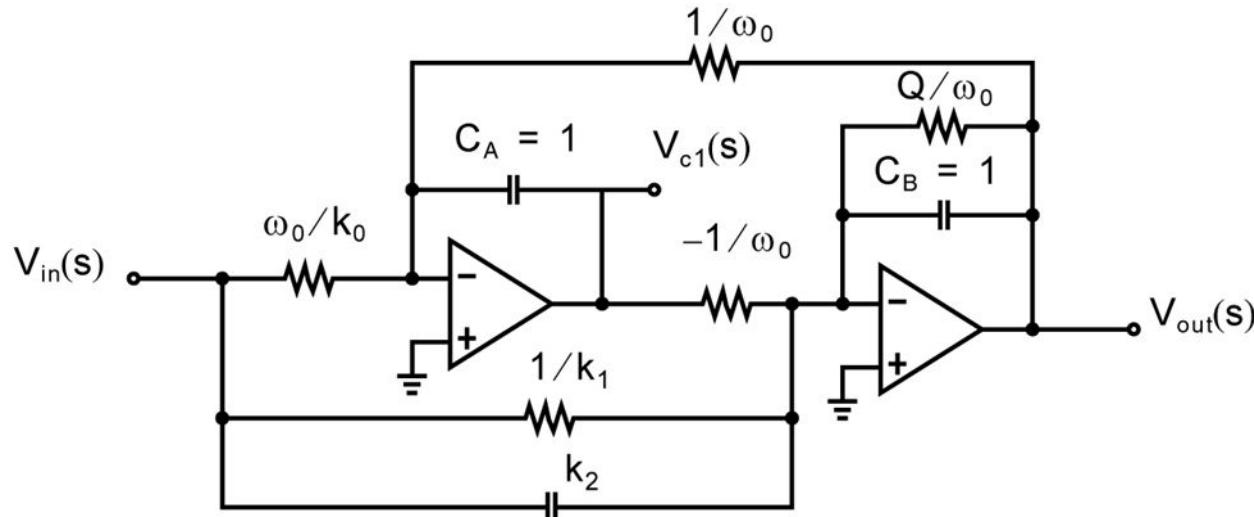
Biquadratic Filter Stages (Biquads)

- Biquadratic transfer function:

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{k_2 s^2 + k_1 s + k_0}{s^2 + (\omega_0 / Q)s + \omega_0}$$

- An important parameter in filter design is the *pole-Q*. It is defined as $Q = \omega_0/(2|\sigma_p|)$, where ω_0 is the magnitude of the complex pole, often called *pole frequency*, and σ_p is the real part ($\sigma_p < 0$) of the pole.

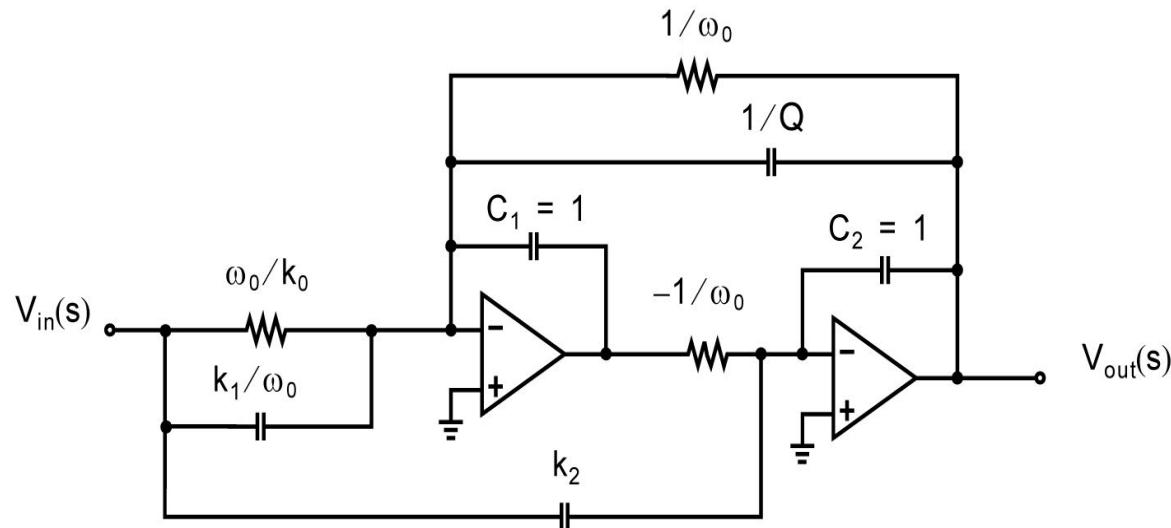
Low-Q Tow-Thomas Biquad



- *Multi-opamp integrator-based biquads:* lower sensitivities, better stability, and more versatile use. They can be realized in fully differential form.
- The Tow-Thomas biquad is a sine-wave oscillator, stabilized by one or more additional element. (Here by the resistor Q/ω_0 .) This reduces the integrator phase shift to a value below 90° .

High-Q Tow-Thomas Biquad

For high-Q poles, damping can be introduced by shunting the feedback resistor with a capacitor. In the low-Q biquad, the value of Q is determined by the ratio of the damping resistor to the other integrator resistors, while in the biquad shown by the ratio of the damping capacitance to the feedback ones. Since large capacitance ratios are more accurately controlled than large resistance ratios, this circuit is preferable for the realization of high-Q biquads.

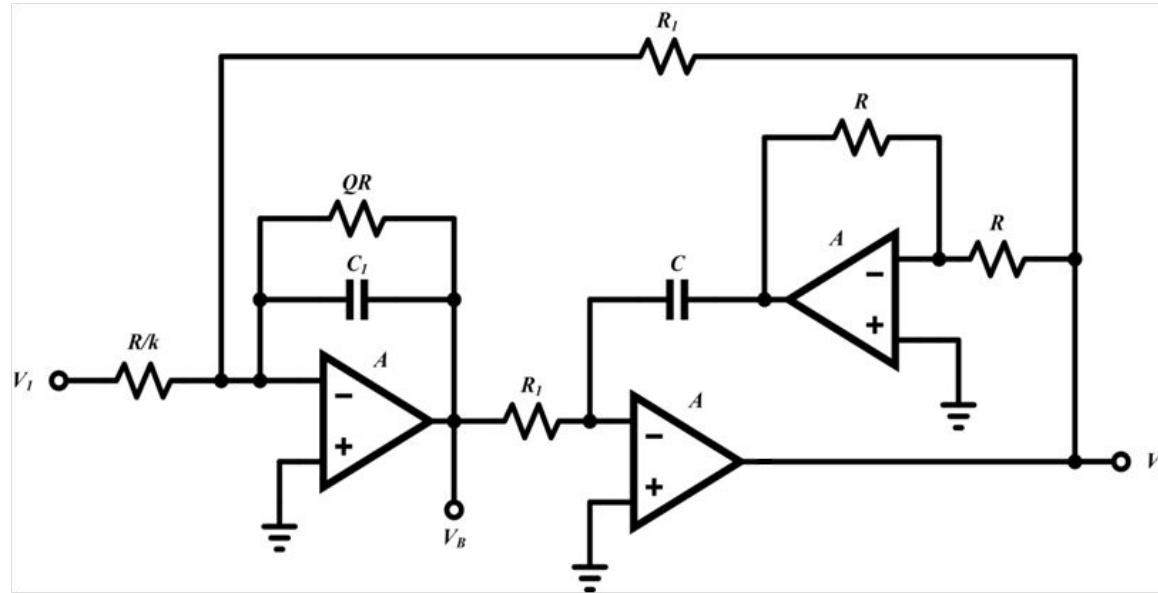


Biquad Design Issues

- The Tow-Thomas biquads contain 8 designable elements.
- The prescribed transfer function has 5 coefficients, so there are 3 degrees of freedom available.
- One degree should be used for dynamic range scaling of the first opamp, the other two to optimize the impedance level of both stages
- Higher impedance level yields lower power requirements, lower level gives lower noise.

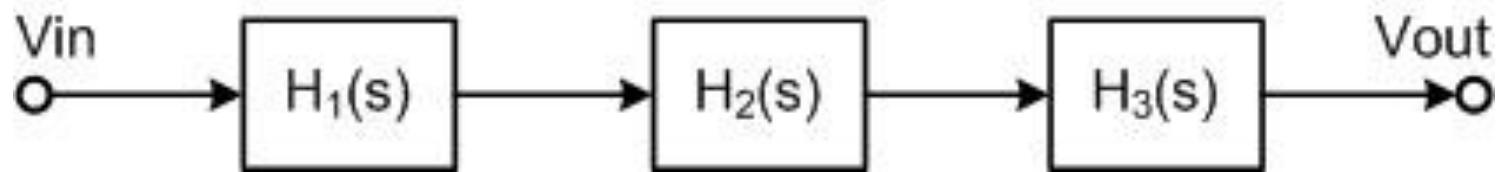
Ackerberg–Mossberg Filter [1]

- Similar to the Tow-Thomas biquad, but less sensitive to finite opamp gain effects.



- The inverter is not needed for fully differential realization. Then it becomes the Tow-Thomas structure.

Cascade Filter Design [3], [5]



- Higher-order filter can be constructed by cascading low-order ones. The $H_i(s)$ are multiplied, provided the stage outputs are buffered.
- The $H_i(s)$ can be obtained from the overall $H(s)$ by factoring the numerator and denominator, and assigning conjugate zeros and poles to each biquad.
- Sharp peaks and dips in $|H(f)|$ cause noise spurs in the output. So, dominant poles should be paired with the nearest zeros.

Cascade Filter Design [5]

- Ordering of sections in a cascade filter dictated by low noise and overload avoidance. Some rules of thumb:
- High-Q sections should be in the middle;
- First sections should be low-pass or band-pass, to suppress incoming high-frequency noise;
- All-pass sections should be near the input;
- Last stages should be high-pass or band-pass to avoid output dc offset.

Rules of Cascade Filter Design [5]

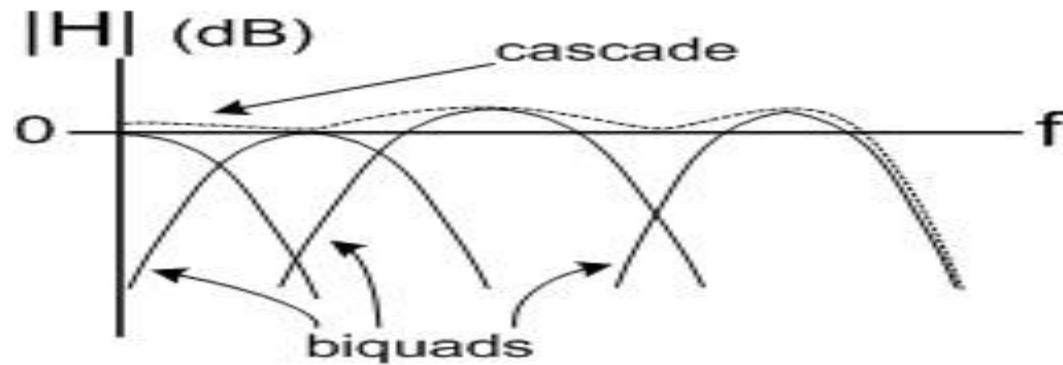
- 1. Order the stages in the cascade so as to equalize their output signal swings as much as possible for dynamic range considerations;
- 2. Choose the first biquad to be a lowpass or bandpass to reject high-frequency noise, and thus to prevent overload in the remaining stages;
- 3. If the reduction of the DC offset at the filter output is critical, the last stage should be a highpass or bandpass section, to reject the DC offset introduced by the preceding stages;
- 4. The last stage should NOT in general have a high Q, because these stages tend to have higher fundamental noise and worse sensitivity to power supply noise;

More Rules of Cascade Filter Design

- 5. Also, do not place all-pass stages at the end of the cascade, because these have wideband noise. It is usually best to place all-pass stages near the input port of the filter.
- 6. If several highpass or bandpass stages are available, one can place them at the beginning, middle and end of the filter. This will prevent the input offset from overloading the filter, and also will prevent the internal offsets of the filter from accumulating (and hence decreasing the available signal swing).
- The amount of thermal noise at the filter output varies widely with the order of its sections; therefore by careful ordering several dB of SNR improvement can often be gained.

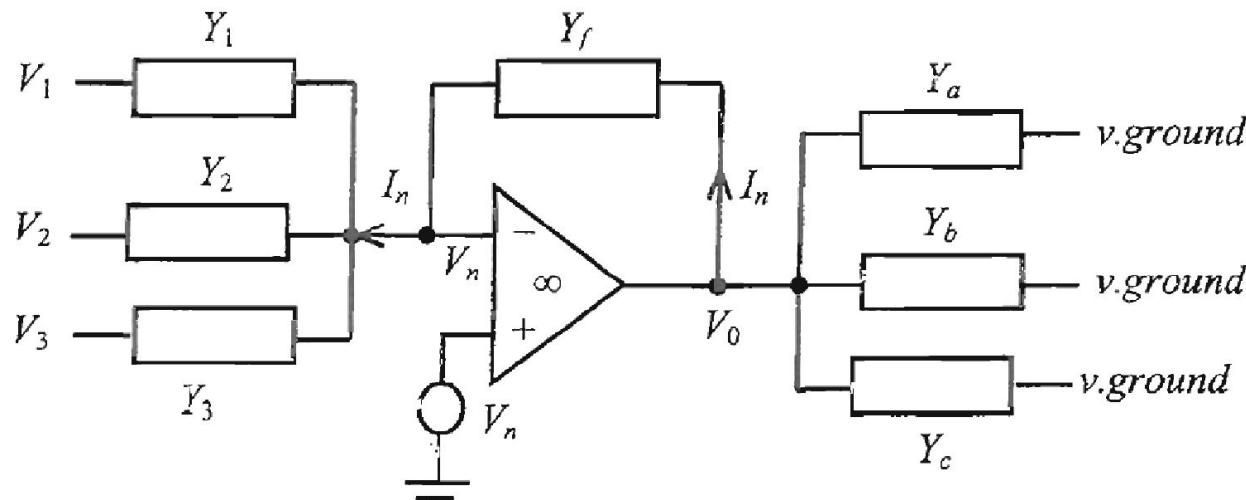
Cascade Filter Performance

- Cascade filters achieve a flat passband by cancelling the slopes of the gain responses of the individual sections. This is an inaccurate process, and hence the passband ripple of these filters is not well controlled. It is difficult to achieve a ripple less than, say, 0.1 dB. By contrast, since the stopband attenuations of the sections (in dB) are simply added, very high stop-band attenuations can be realized.



Dynamic Range Optimization [3]

- Scaling for dynamic range optimization is very important in multi-op-amp filters.
- Active-RC structure:

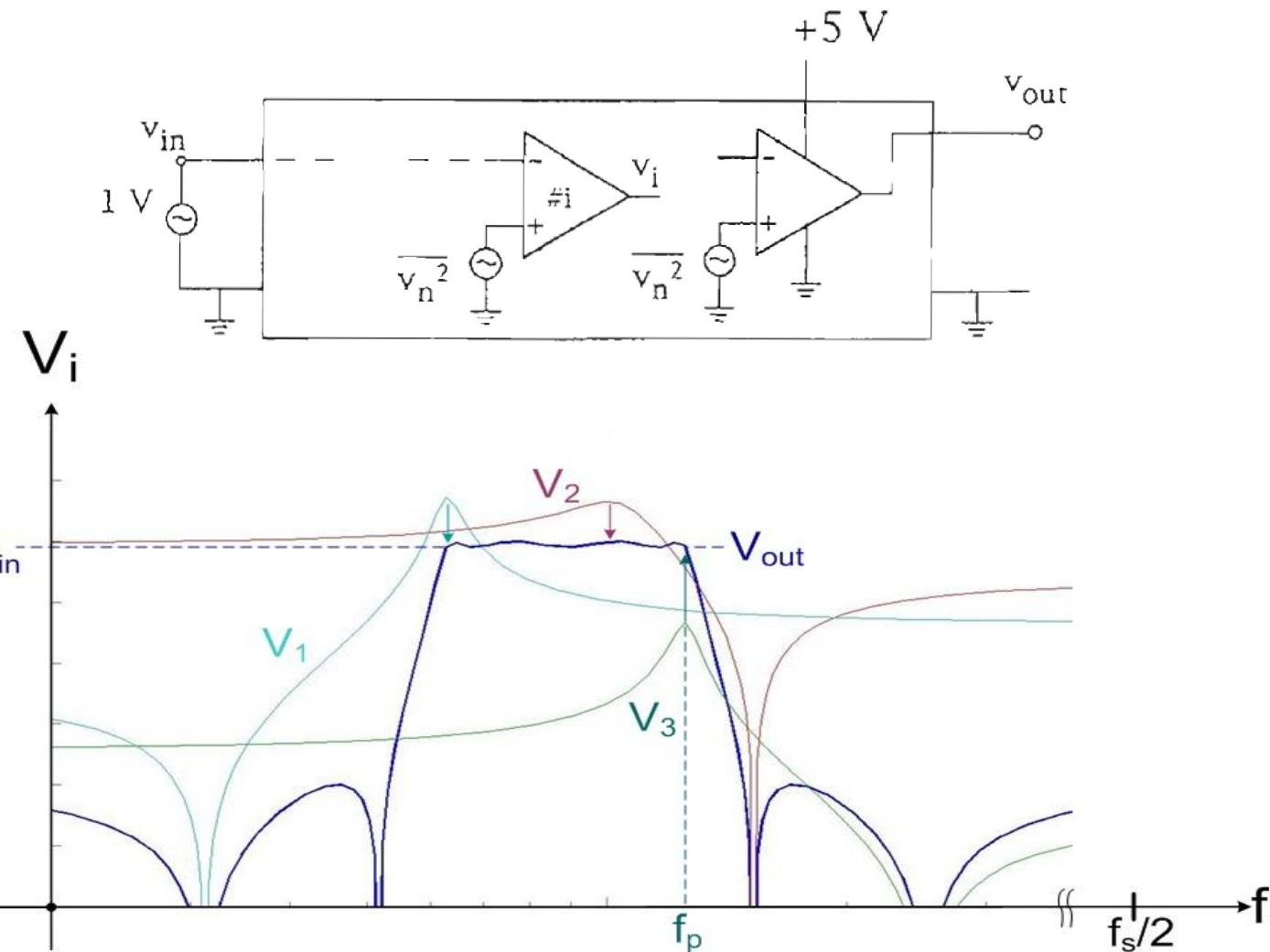


- Op-amp output swing must remain in linear range, but should be made large, as this reduces the noise gain from the stage output to the filter output. However, it reduces the feedback factor and hence increases the settling time.

Dynamic Range Optimization

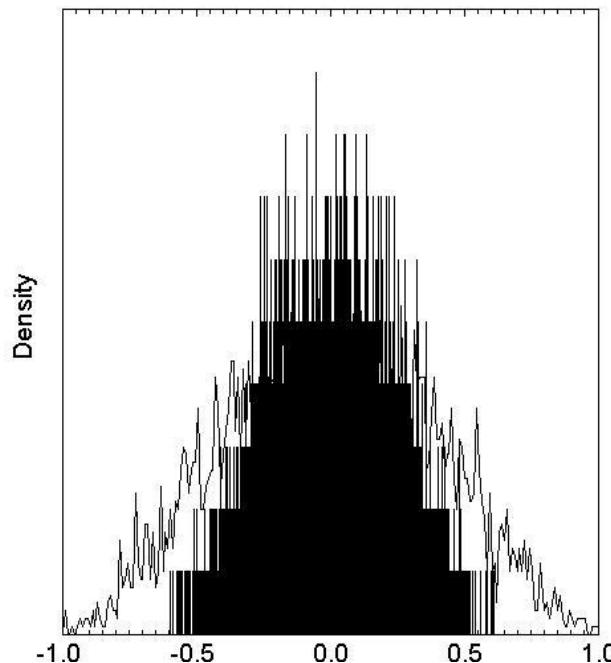
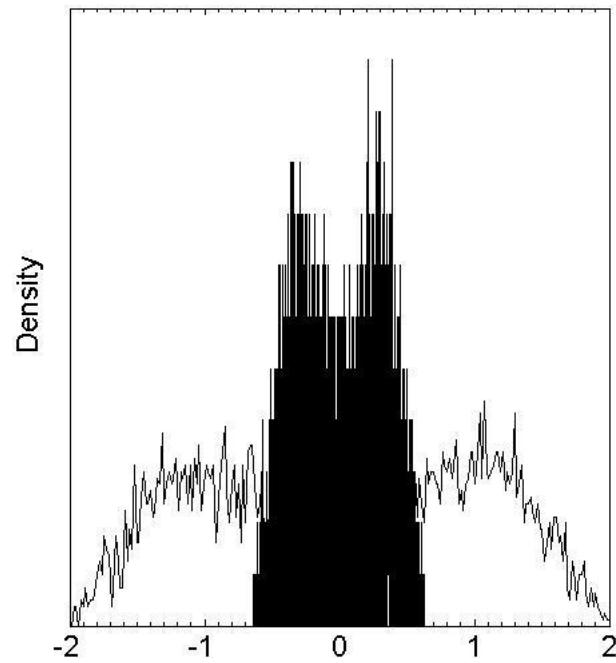
- Multiplying all impedances connected to the opamp *output* by k , the output voltage V_{out} becomes $k \cdot V_{out}$, and all output currents remain unchanged.
- Choose $k \cdot V_{out}$ so that the maximum swing occupies a large portion of the linear range of the opamp.
- Find the maximum swing in the *time domain* by plotting the histogram of V_{out} for a typical input, or in the *frequency domain* by sweeping the frequency of an input sine-wave to the filter, and compare V_{out} with the maximum swing of the output opamp.

Optimization in Frequency Domain



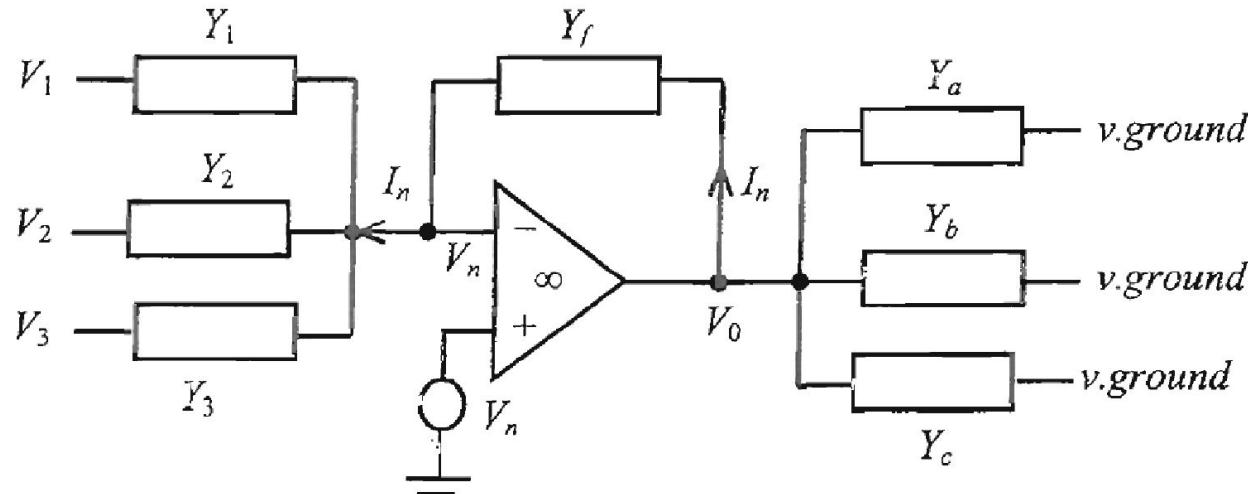
Optimization in the Time Domain

Histogram-based optimization:



Impedance Level Scaling

- Lower impedance \rightarrow lower noise, but more bias power!
- All admittances connected to the *input* node of the opamp may be multiplied by a convenient scale factor without changing the output voltage or output currents. This may be used, e.g., to minimize the area of capacitors.
- Impedance scaling should be done *after* dynamic range scaling, since it doesn't affect the dynamic range.

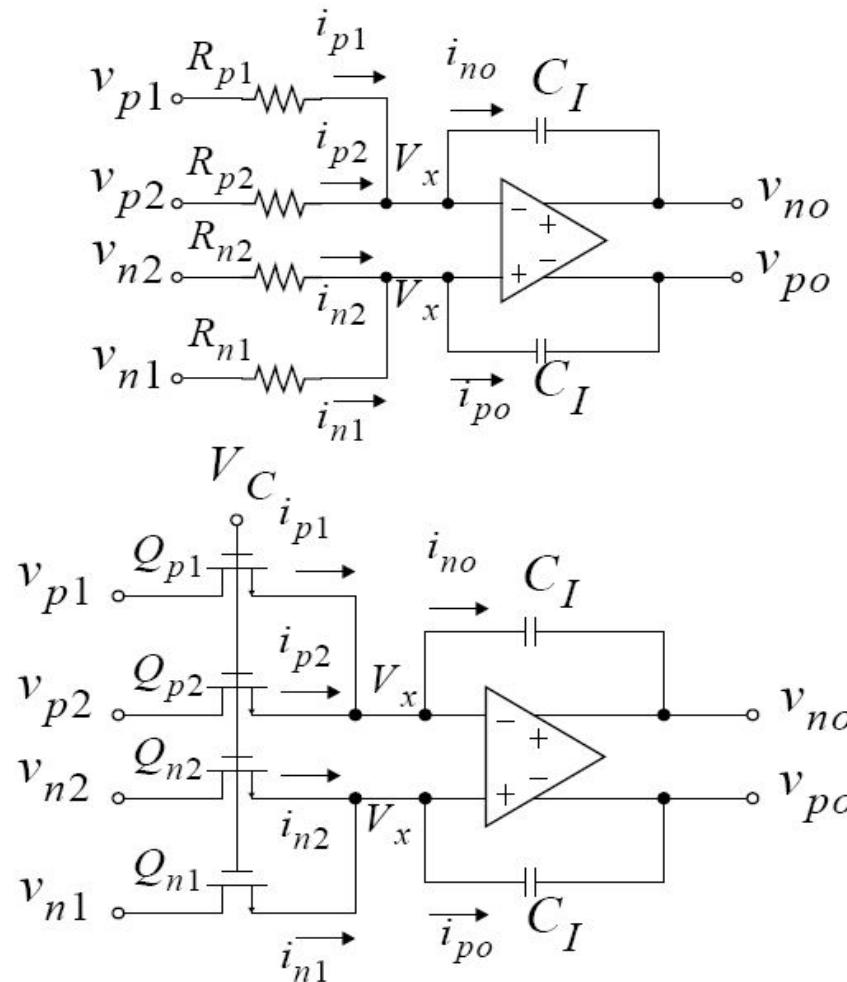


Tunable Active-RC Filters [2], [3]

- Tolerances of RC time constants typically $30 \sim 50\%$, so the realized frequency response may not be acceptable.
- Resistors may be trimmed, or made variable and then automatically tuned, to obtain time constants locked to the period T of a crystal-controlled clock signal.
- Simplest: replace R_s by MOSFETs operating in their linear (triode) region. MOSFET-C filters result.
- Compared to Gm-C filters, slower and need more power, but may be more linear, and easier to design.

Two-Transistor Integrators

- V_c is the control voltage for the MOSFET resistors.



Two-Transistor Integrators

- For resistor integrator

$$v_{\text{diff}} = \frac{1}{sR_1C_I}(v_{p1} - v_{n1}) + \frac{1}{sR_2C_I}(v_{p2} - v_{n2}) \quad (59)$$

- Negative integration — cross-couple wires
- For MOSFET-C integrator

$$r_{DS} = \left(\mu_n C_{ox} \left(\frac{W}{L} \right) (v_{GS} - V_{tn}) \right)^{-1} \quad (60)$$

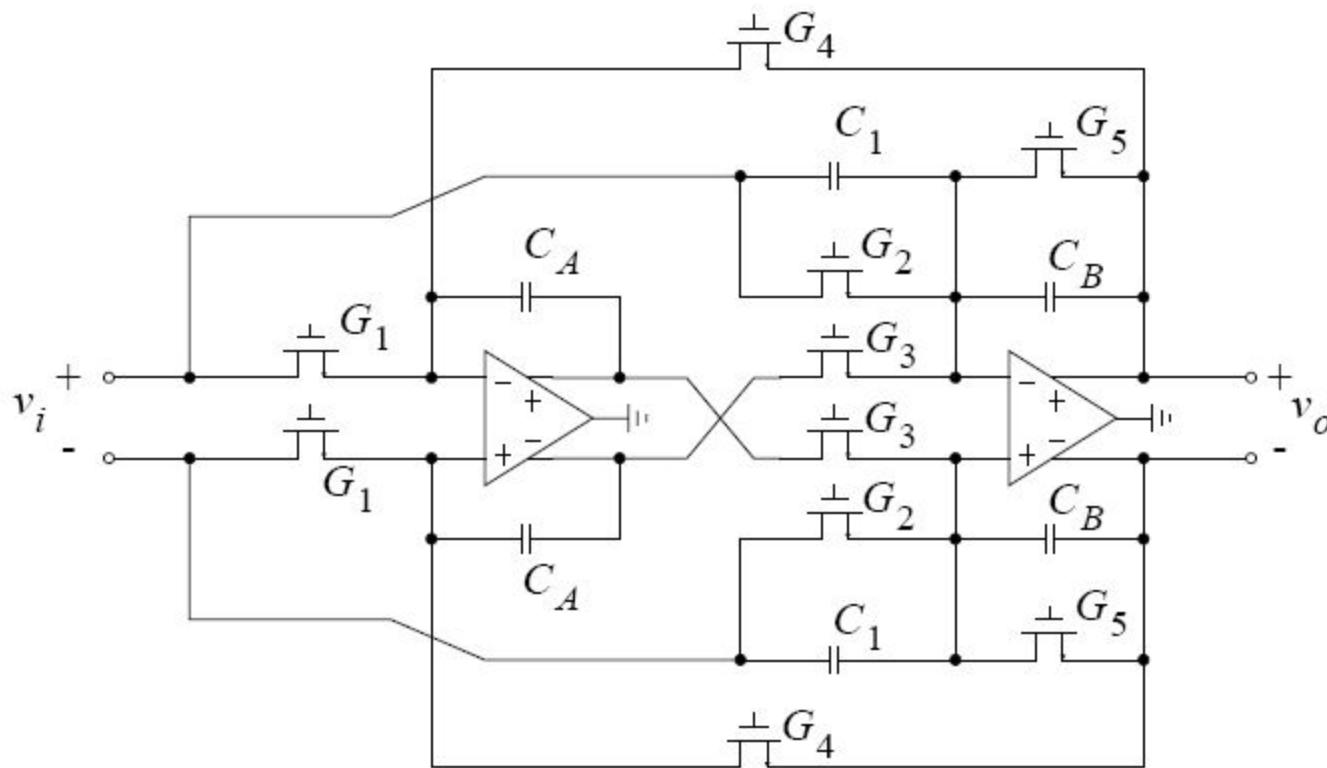
leading to

$$v_{\text{diff}} = \frac{1}{sr_{DS1}C_I}(v_{p1} - v_{n1}) + \frac{1}{sr_{DS2}C_I}(v_{p2} - v_{n2}) \quad (61)$$

$$r_{DSi} = \left(\mu_n C_{ox} \left(\frac{W}{L} \right)_i (V_C - V_x - V_{tn}) \right)^{-1} \quad (62)$$

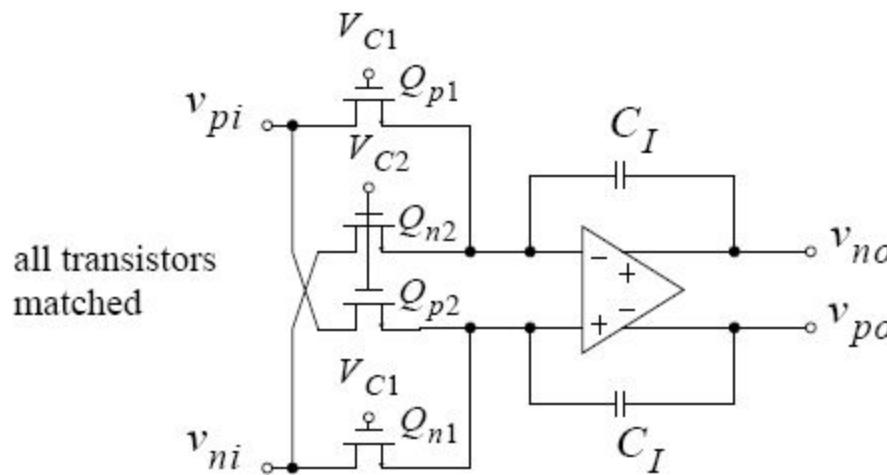
MOSFET-C Biquad Filter [2], [3]

- Tow-Thomas MOSFET-C biquad:



Four-Transistor Integrator

- Linearity of MOSFET-C integrators can be improved by using 4 transistors rather than 2 (Z. Czarnul):



- May be analyzed as a two-input integrator with inputs ($V_{pi}-V_{ni}$) and ($V_{ni}-V_{pi}$).

Four-Transistor Integrator

- If all four transistor are matched in size,

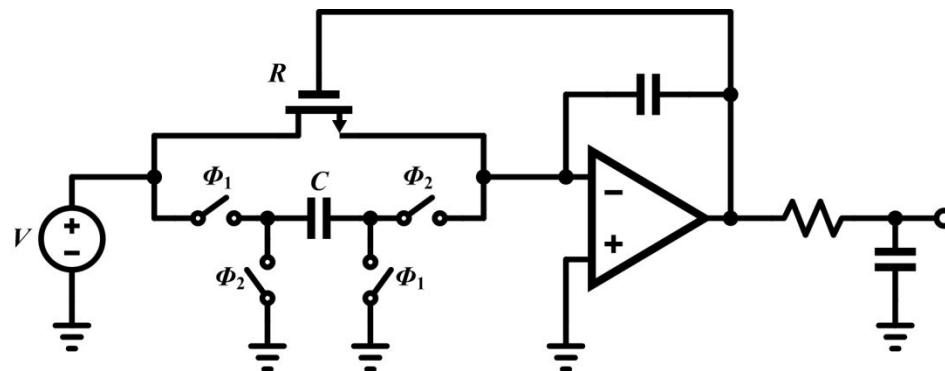
$$v_{\text{diff}} = v_{po} - v_{no} = \frac{1}{sr_{DS}C_I}(v_{pi} - v_{ni})$$

$$r_{DS} = \left(\mu_n C_{ox} \left(\frac{W}{L} \right) (V_{C1} - V_{C2}) \right)^{-1}$$

- Model for drain-source current shows nonlinear terms not dependent on controlling gate-voltage;
- All even and odd distortion products will cancel;
- Model only valid for older long-channel length technologies;
- In practice, about a 10 dB linearity improvement.

Tuning of Active-RC Filters

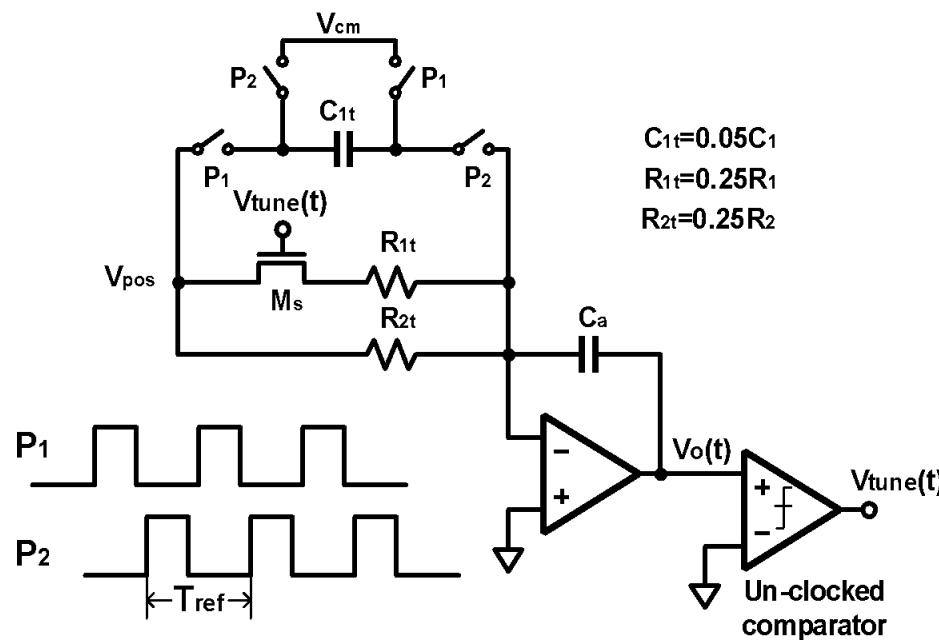
- R_s may be automatically tuned to match to an accurate off-chip resistor, or to obtain an accurate time constant locked to the period T of a crystal-controlled clock signal:



- In equilibrium, $R.C = T$. Match R_s and C_s to the ones in the tuning stage using careful layout. Residual error 1-2%.

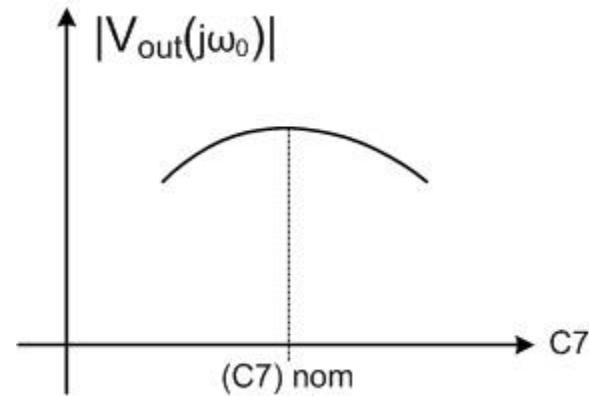
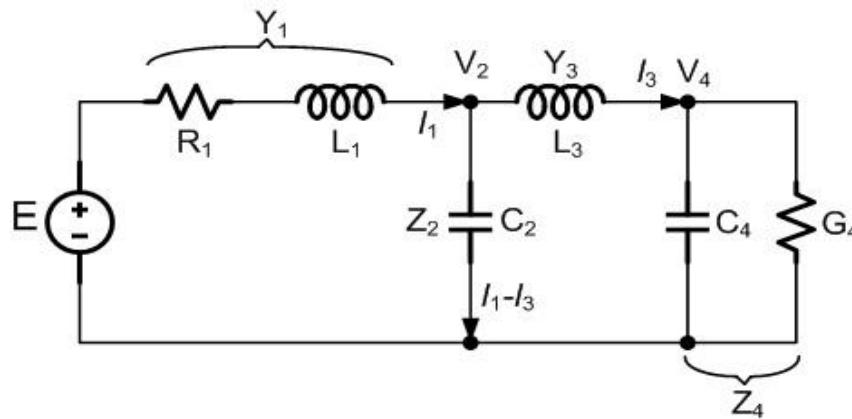
Switched-R Filters [6]

- Replace tuned resistors by a combination of two resistors and a periodically opened/closed switch.
- Automatically tune the duty cycle of the switch:



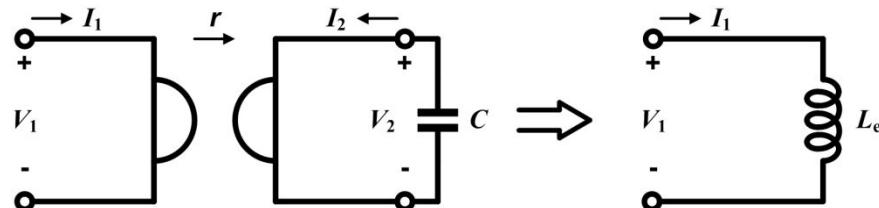
Simulated LC Filters [3], [5]

- A doubly-terminated LC filter with near-optimum power transmission in its passband has low sensitivities to all L & C variations, since the output signal can only decrease if a parameter is changed from its nominal value.

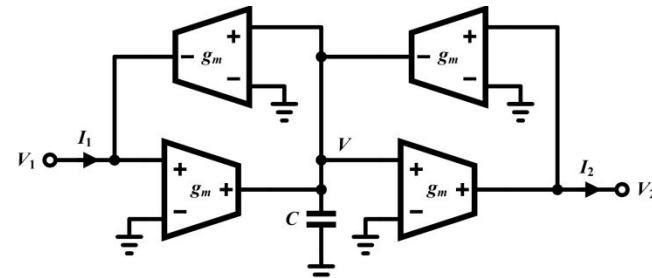
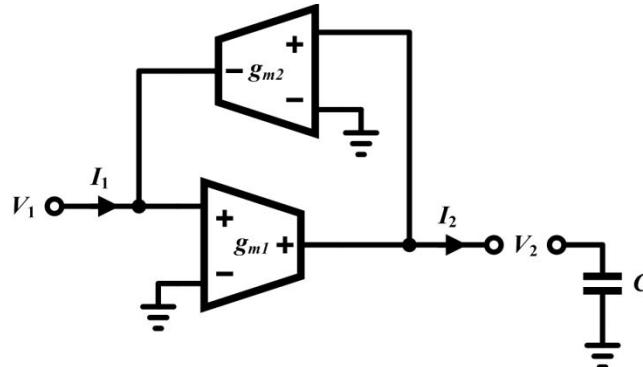


Simulated LC Filters

- Simplest: replace all inductors by gyrator-C stages:



- Using transconductances:

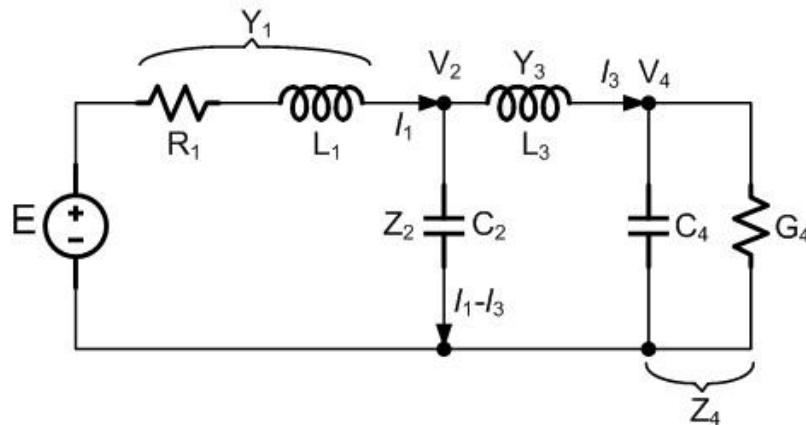


$$L = \frac{C}{g_m^2}$$

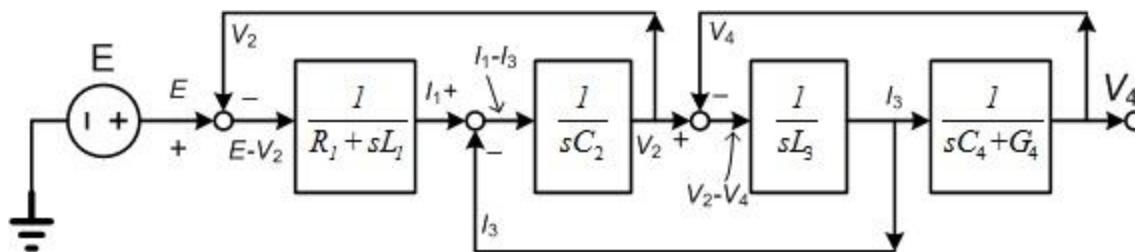
A schematic representation of the inductor L is shown as a series inductor symbol with value $\frac{C}{g_m^2}$.

Simulated LC Filters with Integrators

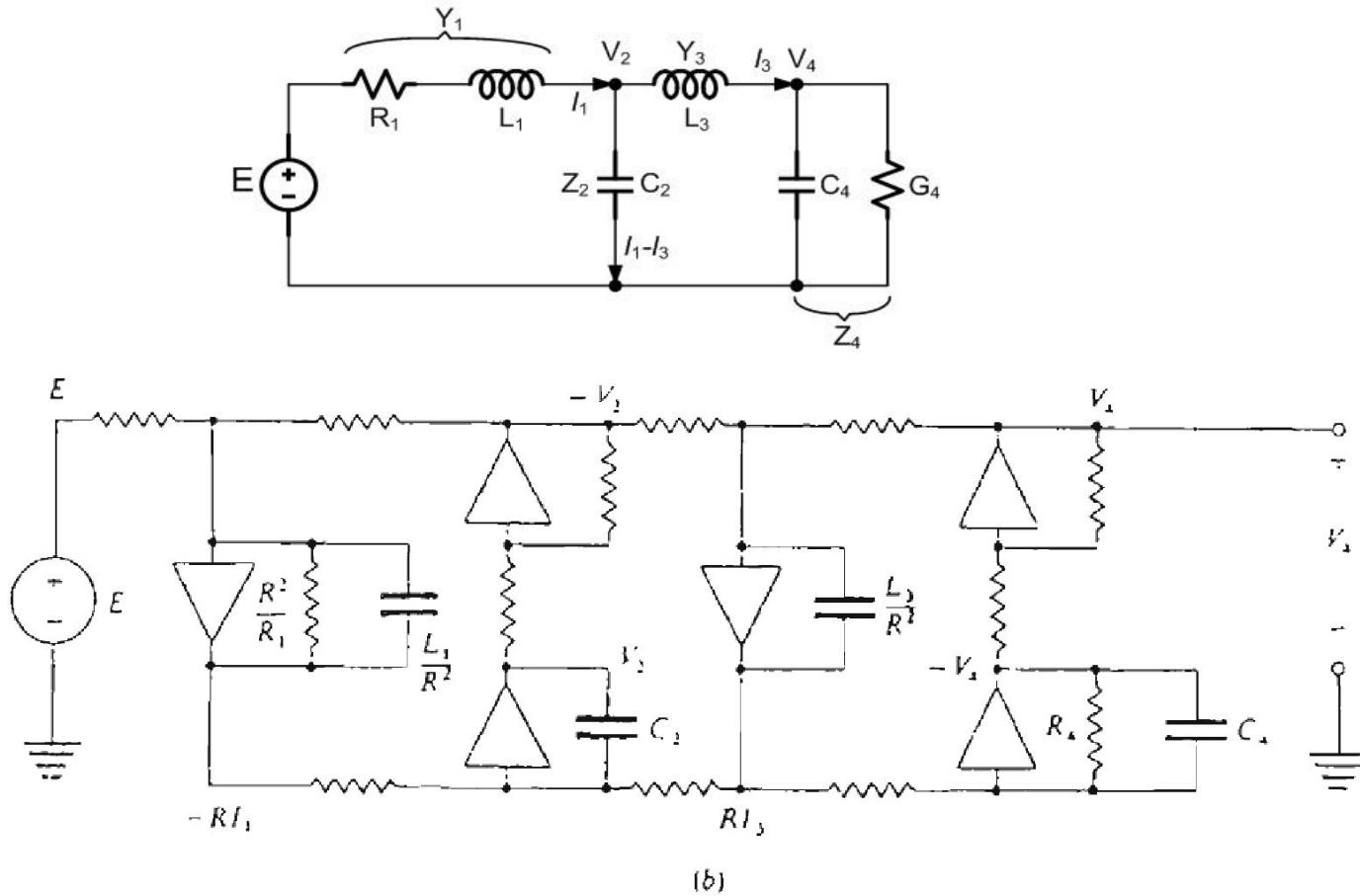
- Simulating the Kirchhoff and branch relations for the circuit:



- Block diagram:



Simulated LC Filters Using Integrators



Cascade vs. LC Simulation Design

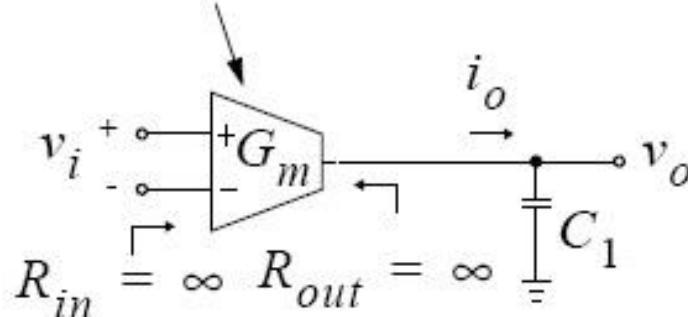
- *Cascade design*: modular, easy to design, lay out, trouble-shoot. Passband sensitivities moderate (~ 0.3 dB), since peaks need to be matched, but the stopband sensitivities excellent, since the stopband losses of the cascaded sections add.
- *LC simulation*: passband sensitivities (and hence noise suppression) excellent due to *Orchard's Rule*. Stopband sensitivities high, since suppression is only achieved by cancellation of large signals at the output:

Gm-C Filters [1], [2], [5]

- Alternative realization of tunable continuous-time filters: *Gm-C filters*.
- Faster than active-RC filters, since they use open-loop stages, and (usually) no opamps..
- Lower power, since the active blocks drive only capacitive loads.
- More difficult to achieve linear operation (no feedback).

Gm-C Integrator

transconductor



$$i_o = G_m v_i$$

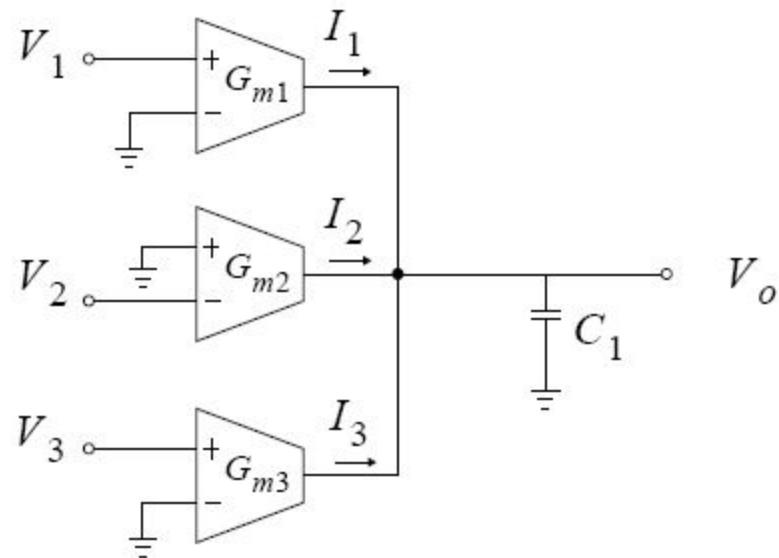
$$V_o = \frac{I_o}{sC_1} = \frac{G_m V_i}{sC_1} \equiv \left(\frac{\omega_{ti}}{s} \right) V_i$$

$$\omega_{ti} = \frac{G_m}{C_1}$$

- Uses a transconductor to realize an integrator;
- The output current of Gm is (ideally) linearly related to the input voltage;
- Output and input impedances are ideally infinite.
- Gm is *not* an operational transconductance amplifier (OTA) which needs a high G_m value, but need not be very linear.

Multiple-Input Gm-C Integrator

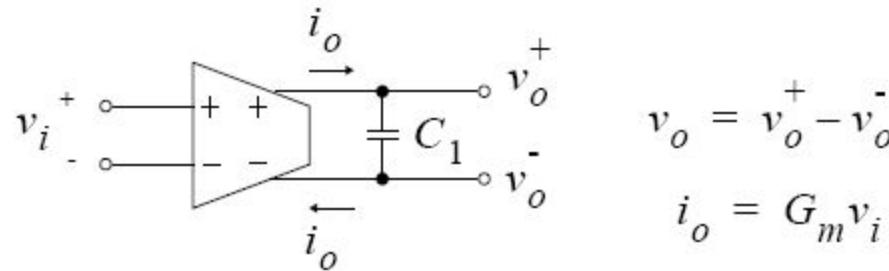
- It can process several inputs:



$$V_o = \frac{1}{sC_1} (G_{m1}V_1 - G_{m2}V_2 + G_{m3}V_3)$$

Fully-Differential Integrators

- Better noise and linearity than for single-ended operation:

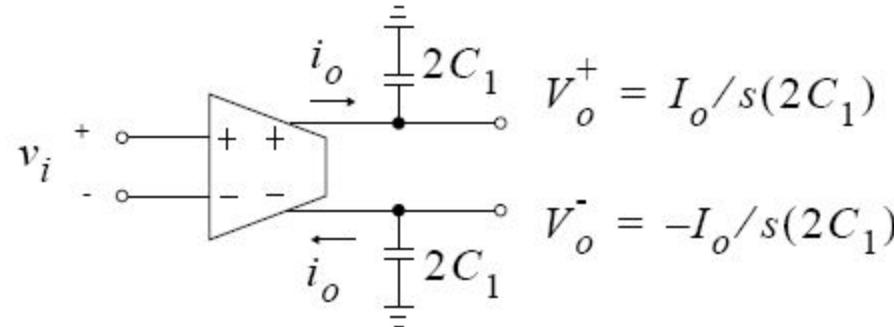


$$v_o = v_o^+ - v_o^-$$
$$i_o = G_m v_i$$

$$V_o = \frac{I_o}{sC_1} = \frac{G_m V_i}{sC_1} \quad \omega_{ti} = \frac{G_m}{C_1}$$

- Uses a single capacitor between differential outputs.
- Requires some sort of common-mode feedback to set output common-mode voltage.
- Needs extra capacitors for compensating the common-mode feedback loop.

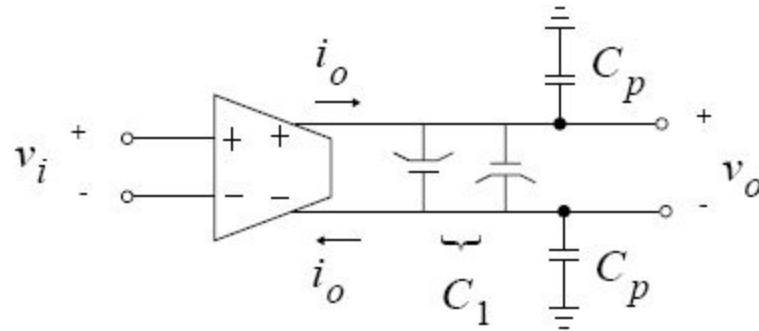
Fully-Differential Integrators



$$V_o = \frac{2I_o}{s(2C_1)} = \frac{G_m V_i}{sC_1} \quad \omega_{ti} = \frac{G_m}{C_1} \quad v_o = v_o^+ - v_o^- \quad i_o = G_m v_i$$

- Uses two grounded capacitors; needs 4 times the capacitance of previous circuit.
- Still requires common-mode feedback, but here the compensation for the common-mode feedback can utilize the same grounded capacitors as used for the signal.

Fully-Differential Integrators

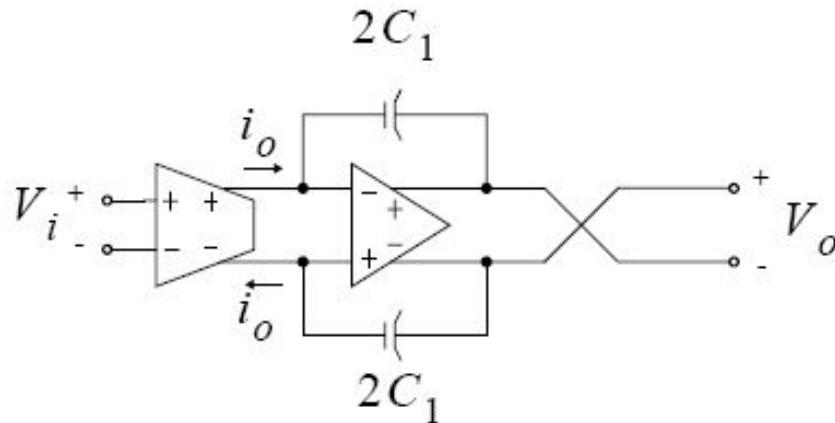


$$V_o = \frac{G_m V_i}{s(C_1 + C_p/2)}$$

$$\omega_{ti} = \frac{G_m}{(C_1 + C_p/2)}$$

- Integrated capacitors have top and bottom plate parasitic capacitances.
- To maintain symmetry, usually two parallel capacitors turned around are used, as shown above.
- The parasitic capacitances affect the time constant.

Gm-C-Opamp Integrator



$$V_o = \frac{2I_o}{s(2C_1)} = \frac{G_m V_i}{sC_1} \quad \omega_{ti} = \frac{G_m}{C_1}$$

- Uses an extra opamp to improve linearity and noise performance.
- Output is now buffered.

Gm-C-Opamp Integrator

Advantages

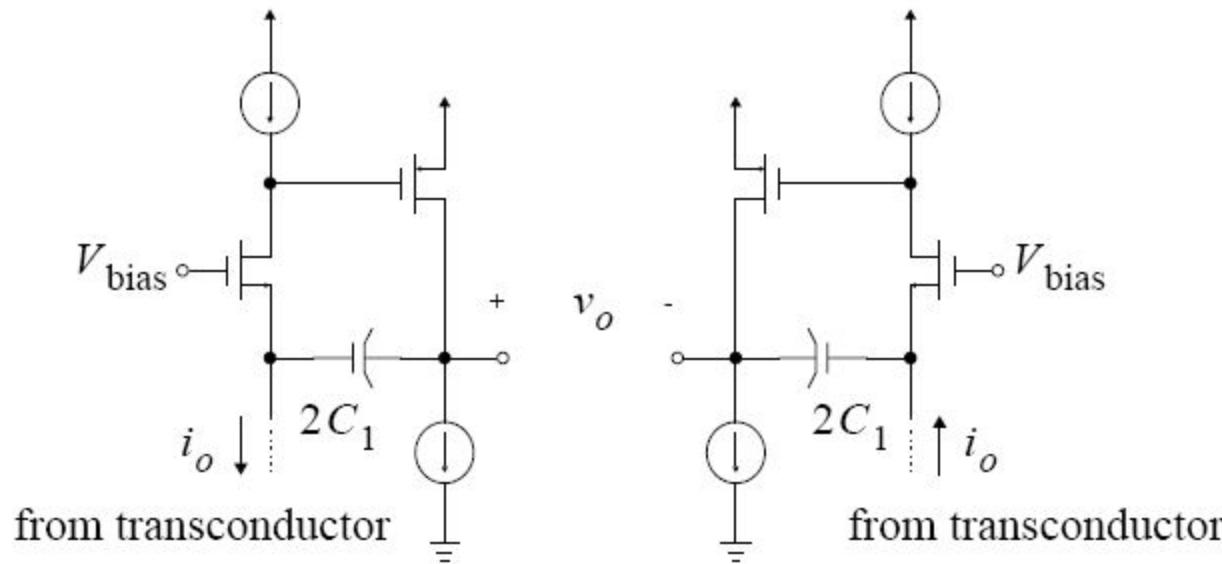
- Effect of parasitics reduced by opamp gain —more accurate time constant and better linearity.
- Less sensitive to noise pick-up, since transconductor output is low impedance (due to opamp feedback).
- *Gm* cell drives virtual ground — output impedance of *Gm* cell can be lower, and smaller voltage swing is needed.

Disadvantages

- Lower operating speed because it now relies on feedback;
- Larger power dissipation;
- Larger silicon area.

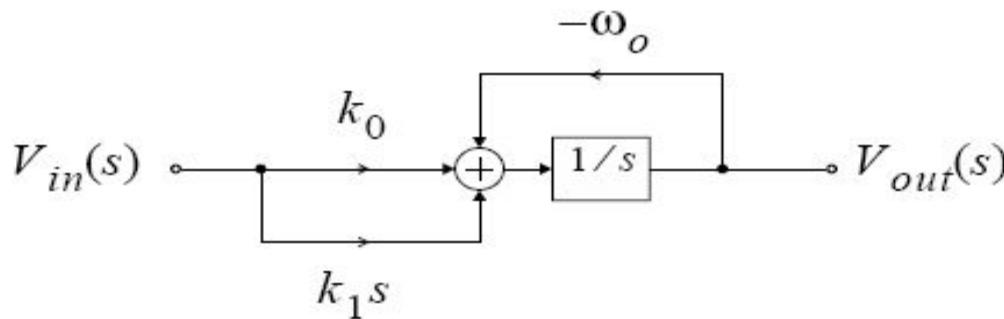
A Simple Gm-C Opamp Integrator

- Pseudo-differential operation. Simple opamp:



- Opamp has a low input impedance, $2/(g_m^2 r_{ds})$, due to common-gate input impedance and feedback.

First-Order Gm-C Filter

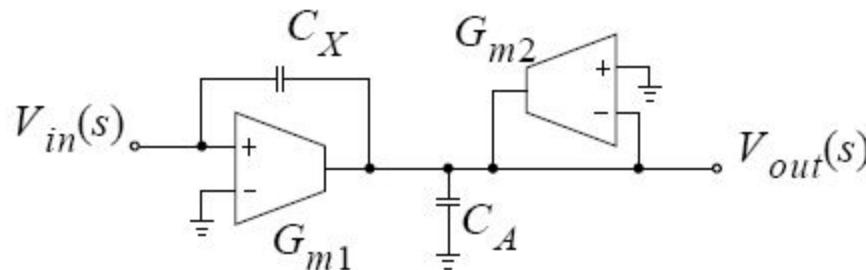


- General first-order transfer-function

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{k_1 s + k_0}{s + \omega_0}$$

- Built with a single integrator and two feed-in branches.
- Branch ω_0 sets the pole frequency.

First-Order Filter

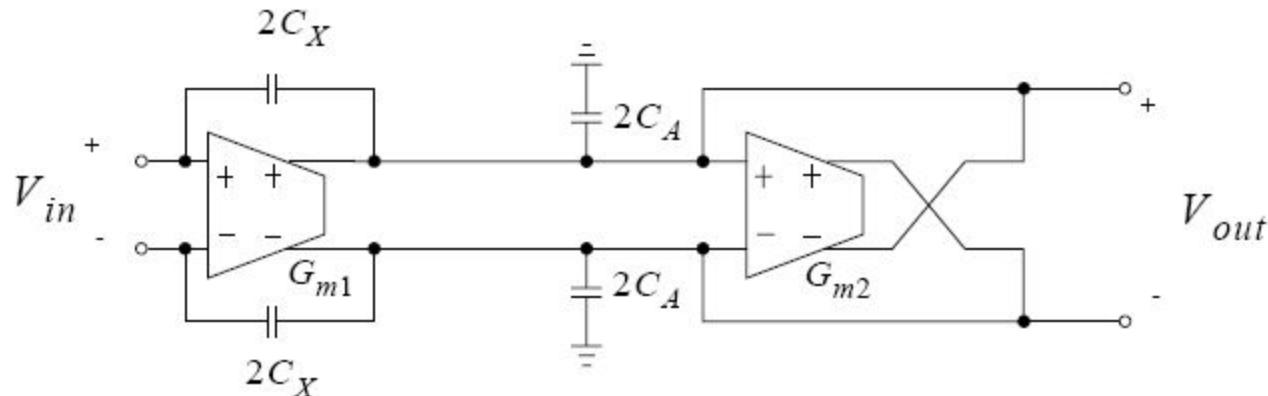


$$C_X = \left(\frac{k_1}{1 - k_1} \right) C_A \text{ where } (0 \leq k_1 < 1) \quad G_{m1} = k_0(C_A + C_X) \quad G_{m2} = \omega_o(C_A + C_X)$$

At infinite frequency, the voltage gain is C_X/C_A . Four parameters, three constraints: impedance scaling possible. The transfer function is given by

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{sC_X + G_{m1}}{s(C_A + C_X) + G_{m2}} = \frac{s \left(\frac{C_X}{C_A + C_X} \right) + \left(\frac{G_{m1}}{C_A + C_X} \right)}{s + \left(\frac{G_{m2}}{C_A + C_X} \right)} \quad (5)$$

Fully-Differential First-Order Filter

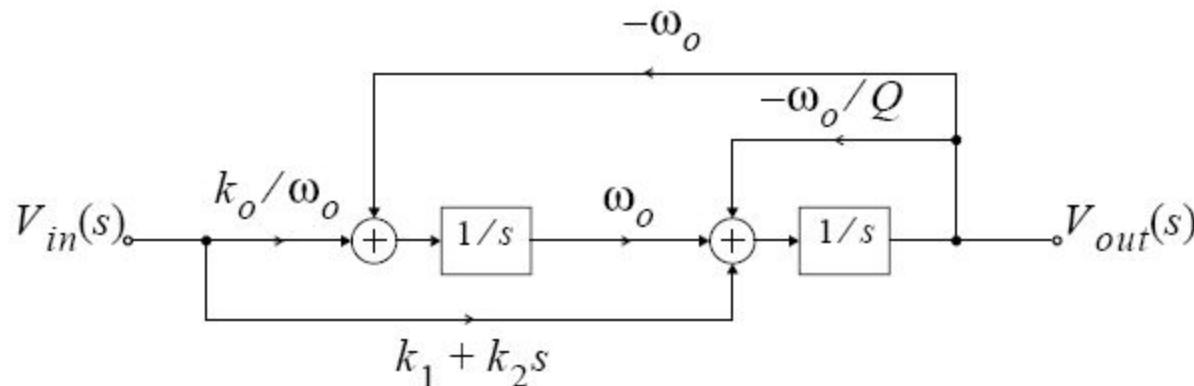


$$C_X = C_A \left(\frac{k_1}{1 - k_1} \right) \text{ where } (0 \leq k_1 < 1)$$
$$G_{m1} = k_0(C_A + C_X)$$
$$G_{m2} = \omega_o(C_A + C_X)$$

- Same equations as for the single-ended case, but the capacitor sizes are doubled.
- 3 coefficients, 4 parameters. May make $G_{m1} = G_{m2}$.
- Can also realize $K1 < 0$ by cross-coupling wires at C_X .

Second-Order Filter

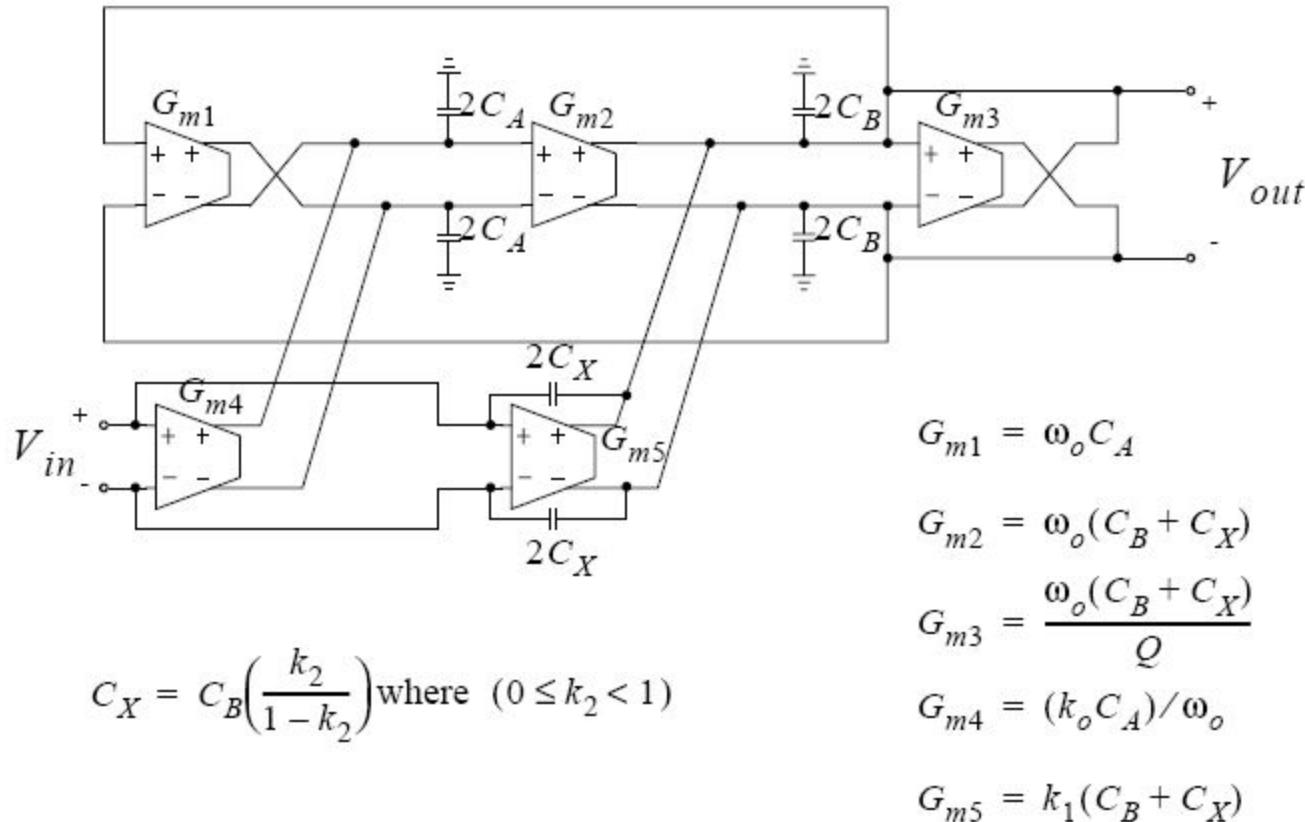
- Tow-Thomas biquad:



$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{k_2 s^2 + k_1 s + k_o}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2} \quad (11)$$

Second-Order Filter

- Fully differential realization:



Second-Order Filter

- Transfer function:

$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{s^2 \left(\frac{C_X}{C_X + C_B} \right) + s \left(\frac{G_{m5}}{C_X + C_B} \right) + \left(\frac{G_{m2} G_{m4}}{C_A (C_X + C_B)} \right)}{s^2 + s \left(\frac{G_{m3}}{C_X + C_B} \right) + \left(\frac{G_{m1} G_{m2}}{C_A (C_X + C_B)} \right)} \quad (12)$$

- There is a restriction on the high-frequency gain coefficients k_2 , just as in the first-order case (not for differential realization).
- G_{m3} sets the damping of the biquad.
- G_{m1} and G_{m2} form two integrators, with unity-gain frequencies of ω_0/s .

Second-Order Filter

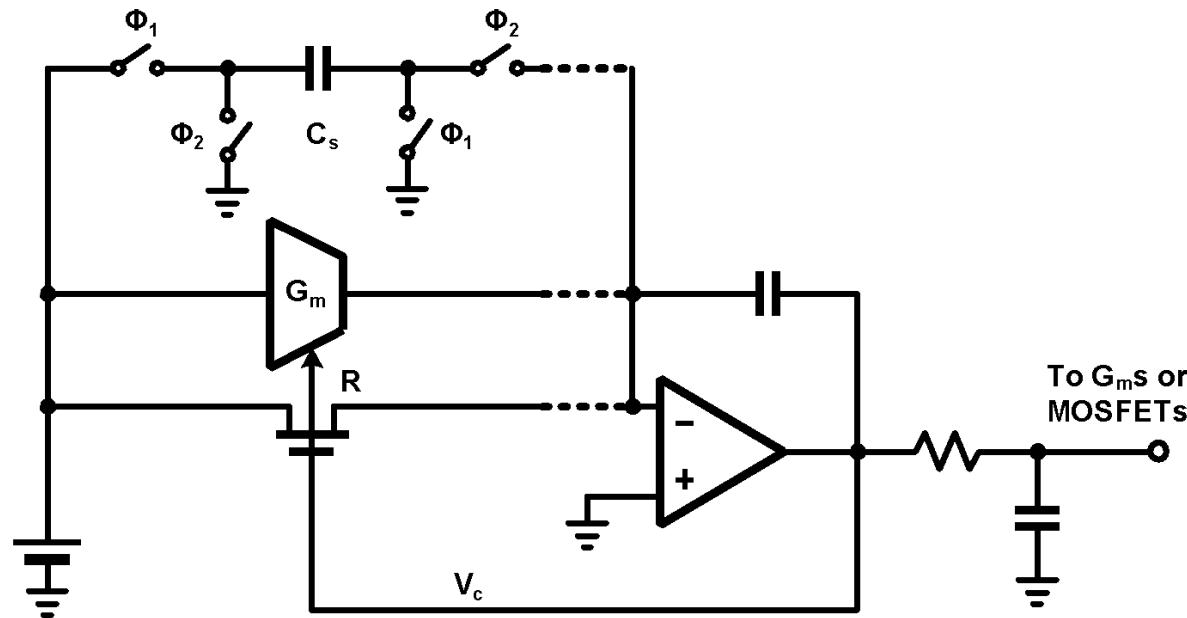
- 5 coefficients needed to match in $H(s)$, 8 designable parameters (5 Gms, 3 capacitances).
- Extra degrees of freedom may be used for dynamic range at internal node and impedance scaling, and for using matched Gm blocks.
- In cascade design, the input admittance Y_{in} is important. If $C_x = 0$, $Y_{in} = 0$. Otherwise, it is $Y_{in} = sC_x [1 - H(s)]$.
- Y_{in} may be absorbed in the previous stage's output capacitor CB .

Scaling of Cascade Gm-C Filter

- In a cascade of biquads, $H(s) = H1(s).H2(s)$ Before realization, scale all $Hi(s)$ so that the maximum output swings are the largest allowable. This takes care of the output swings of $Gm2$, $Gm3$, and $Gm5$.
- Multiply $Gm1$ and $Gm4$, or divide CA, by the desired voltage scale factor for the internal capacitor CA. This takes care of the output swings of $Gm1$ and $Gm4$.
- It is possible to multiply the Gms and capacitors of both integrators by any constant, to scale the impedances of the circuit at a convenient level (noise vs. chip area and power).

Tuning of MOSFET-C or Gm-C Filters

- The control voltage V_c is adjusted so that the average input current of the integrator becomes zero. Then, C_s/T equals $1/R(V_c)$ or $G_m(V_c)$, so that the time constant $R(V_c)C_s$ or C_s/G_m equals the clock period T .
- Matching the filter capacitors and its MOSFET or G_m elements to the calibration ones, $\sim 1\%$ accuracy can be achieved.

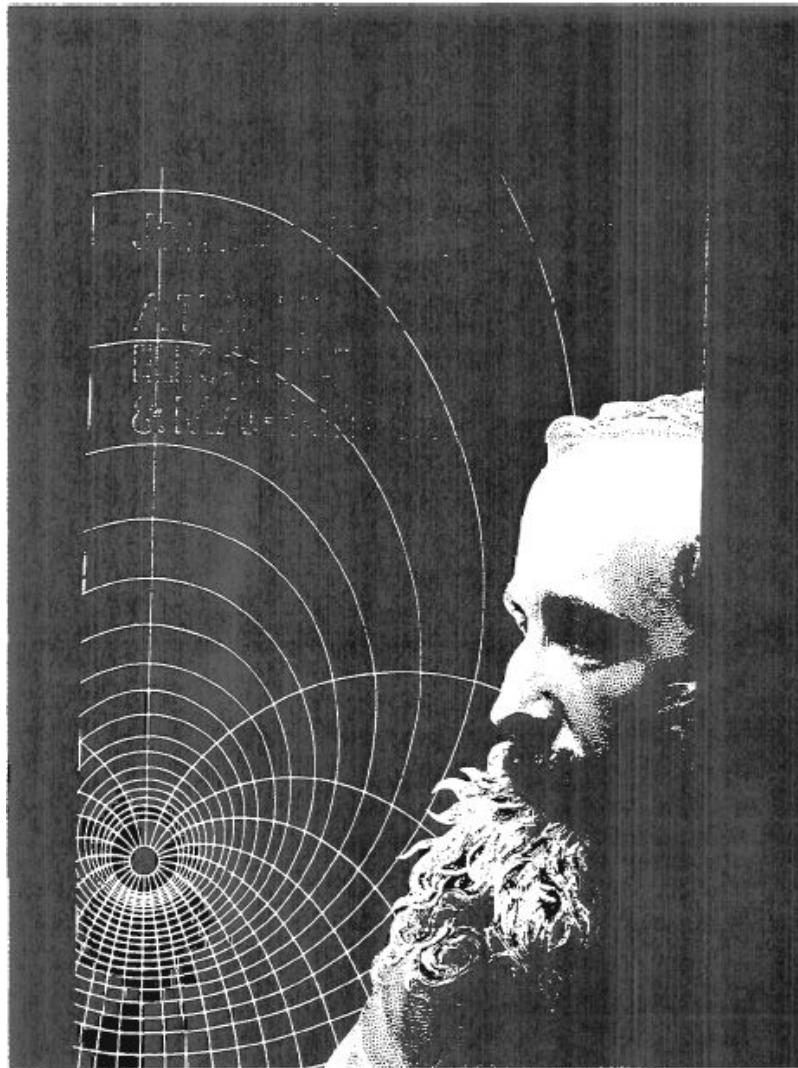


Switched-Capacitor Circuits

History

- "SC" replacing "R"; 1873, James Clerk Maxwell, "A TREATISE ON ELECTRICITY AND MAGNETISM", PP. 420-421.
- IC Context: 1972, D. L. Fried. Low-, high- and bandpass (n-path!) SC filters.
- Application as ADCs: 1975, McCreary and Gray.
- 1977, UC Berkeley, BNR, AMI, U. of Toronto, Bell labs., UCLA, etc.: Design of high-quality SC filters and other analog blocks.

The First Inventor



The Invention

420

COMPARISON OF UNITS

The capacity of the condenser is thus determined by the following quantities:—

T , the time of vibration of the magnet from rest to rest.

R , the resistance of the coil.

θ , the extreme limit of the swing produced by the discharge.

v , the constant deflexion due to the current through the coil R . This method was employed by Professor Fleming Jenkin in determining the capacity of condensers in electromagnetic measure.*

If c be the capacity of the same condenser in electrostatic measure, as determined by comparison with a condenser whose capacity can be calculated from its geometrical data,

$$c = v^2 C.$$

Hence $v^2 = \pi R \frac{c}{T} \frac{\tan \phi}{2 \sin \frac{1}{2} \theta}$.

The quantity v may therefore be found in this way. It depends on the determination of R in electromagnetic measure, but as it involves only the square root of R , an error in this determination will not affect the value of v so much as in the methods of Arts. 772, 773.

Intermittent Current.

775.] If the wire of a battery-circuit be broken at any point, and the broken ends connected with the electrodes of a condenser, the current will flow into the condenser with a strength which diminishes as the difference of the potentials of the plates of the condenser increases, so that when the condenser has received the full charge corresponding to the electromotive force acting on the wire the current ceases entirely.

If the electrodes of the condenser are now disconnected from the ends of the wire, and then again connected with them in the reverse order, the condenser will discharge itself through the wire, and will then become recharged in the opposite way, so that a transient current will flow through the wire, the total quantity of which is equal to two charges of the condenser.

By means of a piece of mechanism (commonly called a Commutator, or wippe) the operation of reversing the connexions of the condenser can be repeated at regular intervals of time, each interval being equal to T . If this interval is sufficiently long to

* Report of British Association, 1807, pp. 483-488.

776.]

INTERMITTENT CURRENT

421

allow of the complete discharge of the condenser, the quantity of electricity transmitted by the wire in each interval will be $2 EC$, where E is the electromotive force, and C is the capacity of the condenser.

If the magnet of a galvanometer included in the circuit is loaded, so as to swing so slowly that a great many discharges of the condenser occur in the time of one free vibration of the magnet, the succession of discharges will act on the magnet like a steady current whose strength is $\frac{2 EC}{T}$.

If the condenser is now removed, and a resistance coil substituted for it, and adjusted till the steady current through the galvanometer produces the same deflexion as the succession of discharges, and if R is the resistance of the whole circuit when this is the case,

$$\frac{R}{R} = \frac{2 EC}{T}; \quad (1)$$

or $R = \frac{T}{2C}$. (2)

We may thus compare the condenser with its commutator in motion to a wire of a certain electrical resistance, and we may make use of the different methods of measuring resistance described in Arts. 345 to 357 in order to determine this resistance.

776.] For this purpose we may substitute for any one of the wires in the method of the Differential Galvanometer, Art. 346, or in that of Wheatstone's Bridge, Art. 347, a condenser with its commutator. Let us suppose that in either case a zero deflexion of the galvanometer has been obtained, first with the condenser and commutator, and then with a coil of resistance R_1 in its

place, then the quantity $\frac{T}{2C}$ will be measured by the resistance of the circuit of which the coil R_1 forms part, and which is completed by the remainder of the conducting system including the battery. Hence the resistance, R , which we have to calculate, is equal to R_1 , that of the resistance coil, together with R_2 , the resistance of the remainder of the system (including the battery), the extremities of the resistance coil being taken as the electrodes of the system.

In the cases of the differential galvanometer and Wheatstone's Bridge it is not necessary to make a second experiment by substituting a resistance coil for the condenser. The value of

Switched-Capacitor Circuit Techniques [2], [3]

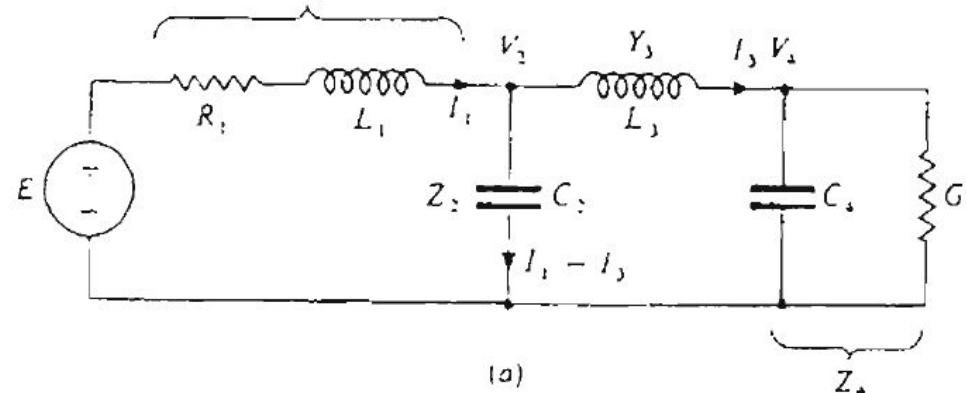
- Signal entered and read out as voltages, but processed internally as charges on capacitors. Since CMOS reserves charges well, high SNR and linearity possible.
 - Replaces absolute accuracy of R & C (10-30%) with matching accuracy of C (0.05-0.2%);
 - Can realize accurate and tunable large RC time constants;
 - Can realize high-order dynamic range circuits with high dynamic range;
 - Allows medium-accuracy data conversion without trimming;
 - Can realize large mixed-mode systems for telephony, audio, aerospace, physics etc. Applications on a single CMOS chip.
 - Tilted the MOS VS. BJT contest decisively.
-

Competing Techniques

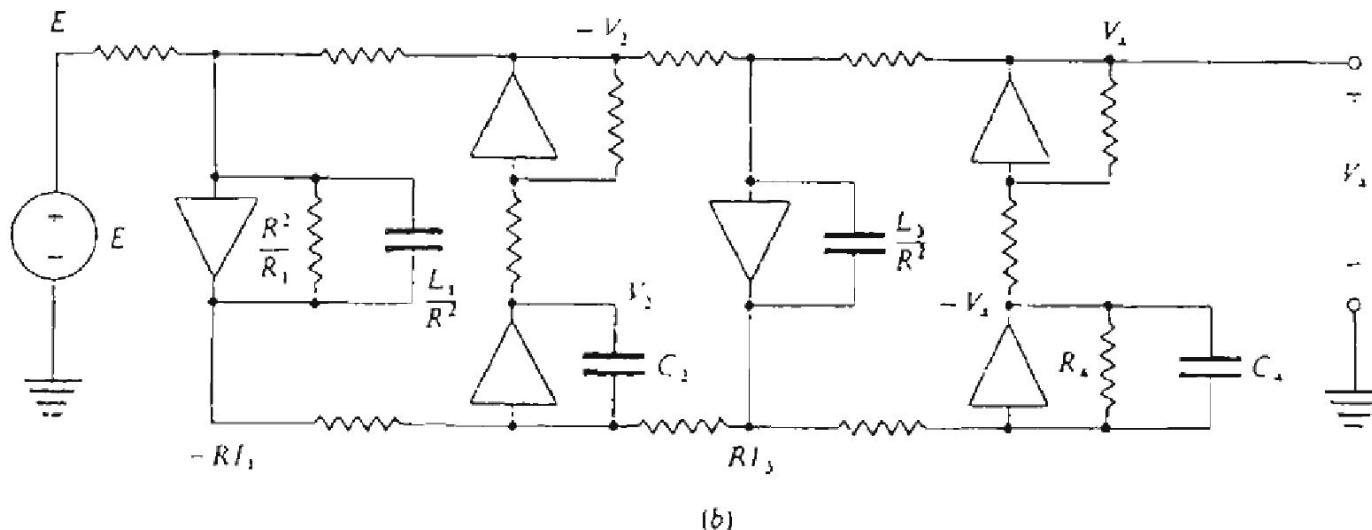
- Switched-current circuitry: Can be simpler and faster, but achieves lower dynamic range & much more THD; Needs more power. Can use basic digital technology; now SC can too!
- Continuous-time filters: much faster, less linear, less accurate, lower dynamic range. Need tuning.

LCR Filters to Active-RC Filters

INDUCTORS REPLACED BY R, C, OP-AMP BLOCKS. SPACE REQUIREMENT FOR TELEPHONE FILTERS REDUCED FROM 3"X3"X.5" TO ABOUT 1.5"X1.5"X.2", OR LESS WITH THICK FILM IMPLEMENTATION.

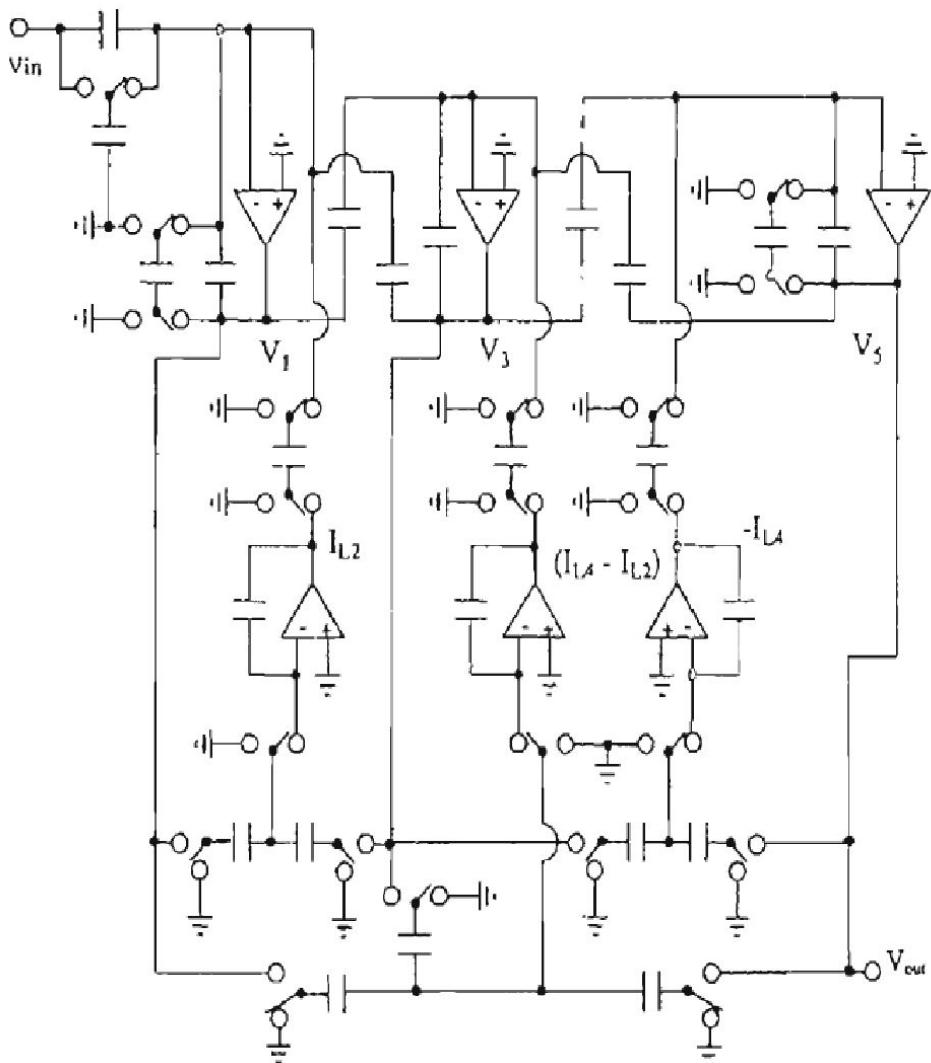
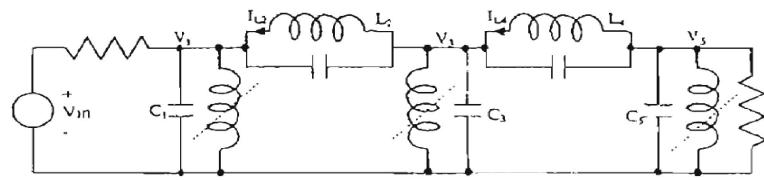


(a)



(b)

LCR Filters to Active-SC Filters



Typical Applications of SC Technology -(1)

Line-Powered Systems:

- Telecom systems (telephone, radio, video, audio)
- Digital/analog interfaces
- Smart sensors
- Instrumentation
- Neural nets.
- Music synthesizers

Typical Applications of SC Technology -(2)

Battery-Powered Micropower Systems:

- Watches
- Calculators
- Hearing aids
- Pagers
- Implantable medical devices
- Portable instruments, sensors
- Nuclear array sensors (micropower, may not be battery powered)

New SC Circuit Techniques

To improve accuracy:

- Oversampling, noise shaping
- Dynamic matching
- Digital correction
- Self-calibration
- Offset/gain compensation

To improve speed, selectivity:

- GaAs technology
- BiCMOS technology
- N-path, multirate circuits

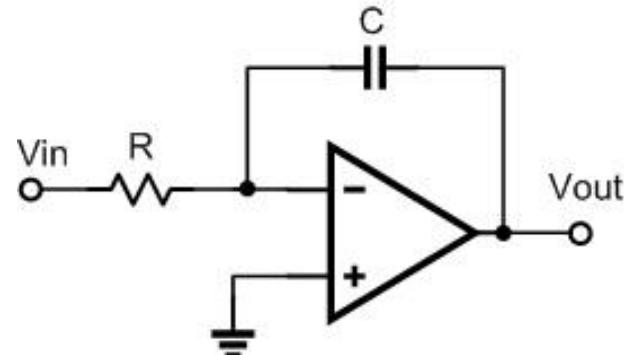
Typical SC Stages

- Amplifiers: programmable, precision, AGC, buffer, driver, sense
- Filters
- S/H and T/H stages
- MUX and deMUX stages
- PLLs
- VCOs
- Modulators, demodulators
- Precision comparators
- Attenuators
- ADC/DAC blocks

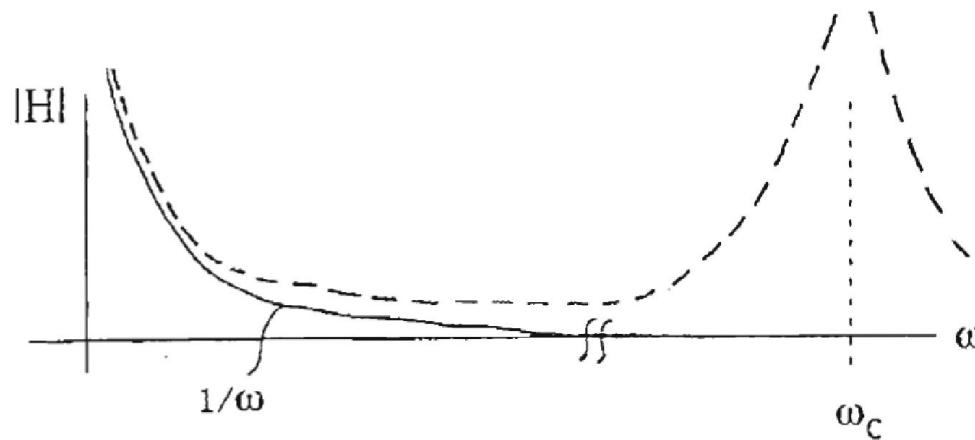
Active - RC Integrator

$$v_{out}(t) = -\frac{1}{RC} \int_{-\infty}^t v_{in}(\tau) d\tau$$

$$H(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = -\frac{1}{j\omega RC}$$

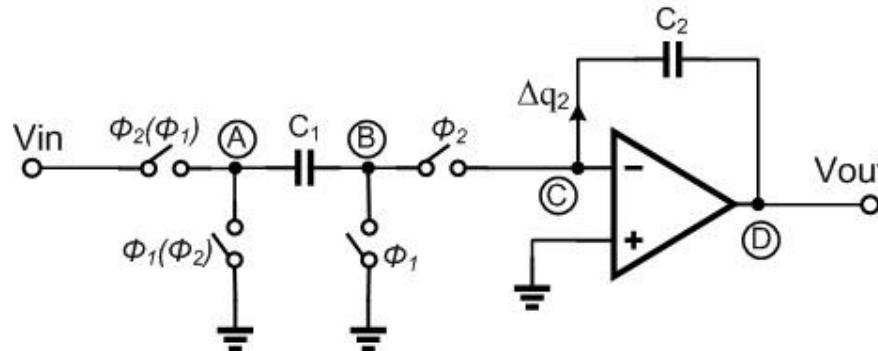


Can be transformed by replacing R1 by an SC branch.



SC Integrator (Analog Accumulator)

Stray insensitive integrators:



For inverting operation,

$$H(z) = V_{out}(z)/V_{in}(z) = - (C_1 / C_2) / (1 - z^{-1})$$

For noninverting operation

$$H(z) = (C_1 / C_2) z^{-1/2} / (1 - z^{-1})$$

SC Integrator Issues

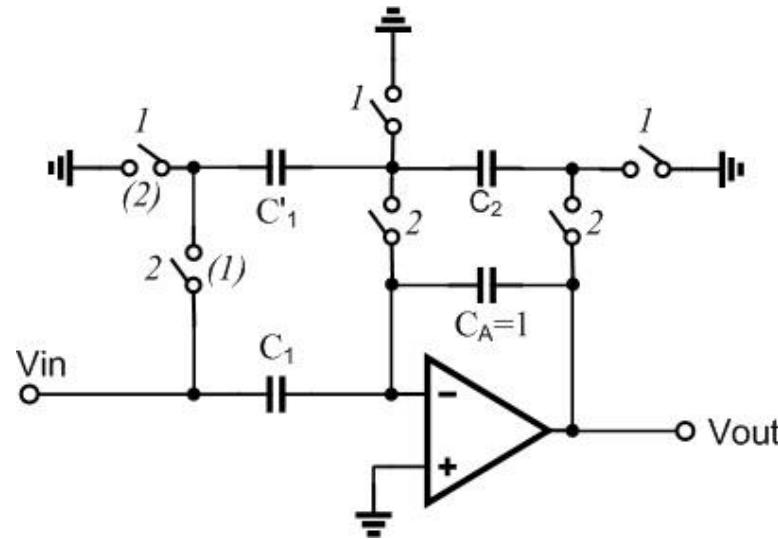
- Every node is an opamp input or output node – low impedance, insensitive to stray capacitances.
- Clock phases must be non-overlapping to preserve signal charges. Gap shouldn't be too large for good SNR.
- For single-ended stage, positive = delaying, negative = non-delaying. For differential, polarity is arbitrary.
- For cascade design, two integrators can be connected in a Tow-Thomas loop. No inverter stage needed; SC branch can invert charge polarity.

Bilinear SC Stage

Transfer function:

$$H(z) = \frac{a_1 z + a_0}{b_1 z + b_0}$$

Circuit:



Bilinear SC Stage

Pole and zero both on positive real axis in z plane,
between zero and one.

In differential circuit, cross-coupling can give negative values.

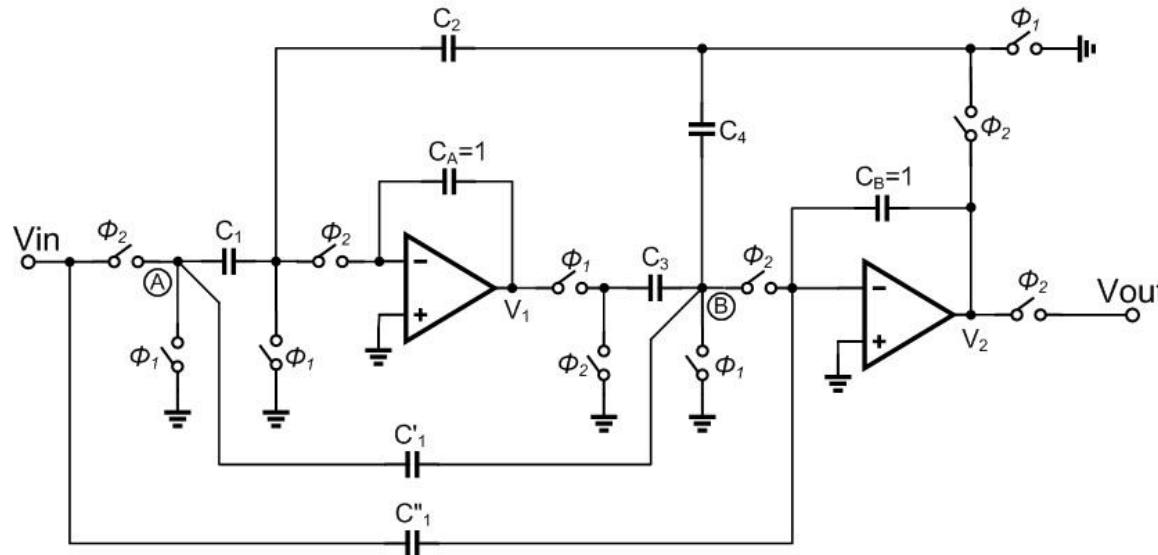
Positive feedback must be avoided!

Low-Q SC Biquad

Biquadratic transfer function:

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + b_0}$$

SC realization:



Low-Q SC Biquad – (3)

Approximate design equations for $\omega_0 T \ll 1$:

$$(\omega_0 T)^2 \equiv \frac{C_2 C_3}{1 + C_4 / 2} \ll 1 \quad R = \dot{T} / C$$

$$Q \equiv \frac{\omega_0 T}{C_4 / C_{A,B}} \quad \text{If } Q > 1 \quad C_4 \text{ very small!}$$

$$\text{DC gain} \equiv \frac{C_1}{C_2} \quad \frac{C_4}{C_A} \sim \frac{\omega_0 T}{Q} \ll 1$$

$$C_A = C_B \equiv 1$$

$$C_2 = C_3 \quad \text{for minimum spread} \sim \omega_0 T$$

Exact equations:

$$H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + b_0} = -\frac{(C_1' + C_1'')z^2 + (C_1 C_3 - C_1' - 2C_1'')z + C_1''}{(1 + C_4)z^2 + (C_2 C_3 - C_4 - 2)z + 1}$$

Low-Q SC Biquad – (4)

- Without C4, sine-wave oscillator. With C4, loop phase < 360 degrees for any element values. Poles always inside the unit circle.
- DC feedback always negative.
- Pole locations determined by C4/CA only - sensitive to mismatch for high Q!
- Capacitance ratio CA/C4 large for high Q.

Low-Q Biquad Issues

- Assuming that (as is normally the case) the biquad realizes a pair of complex conjugate poles, the sensitivity to element value variations and other nonideal effects depends largely on the proximity of these poles to the unit circle, i.e. on the value of $(1 - |z_p|)$. The smaller this value is, the more selective the response is, and also the more sensitive is the biquad to nonideal effects. The value of $(1 - |z_p|)$ can be directly estimated from $H(z)$. For the circuit of Slide 86,
 - $b_0/b_2 = 1/(1 + C_4/C_B)$
 - $1 - |z_p| \sim 1/[2(C_B/C_4 + 1)]$.
 - For highly selective filters where $1 - |z_p| \ll 1$, this indicates that C_B/C_4 must be large, resulting in a large spread of element values, and also that the circuit will be sensitive to errors in C_B/C_4 . Thus this circuit is not suitable for the realization of such biquadratic $H(z)$ functions.

Low-Q SC Biquad – (4)

For $b_0 = 1$, matching coefficients:

$$C_1'' = a_0$$

$$C_1' = a_2 - a_0$$

$$C_4 = b_2 - 1$$

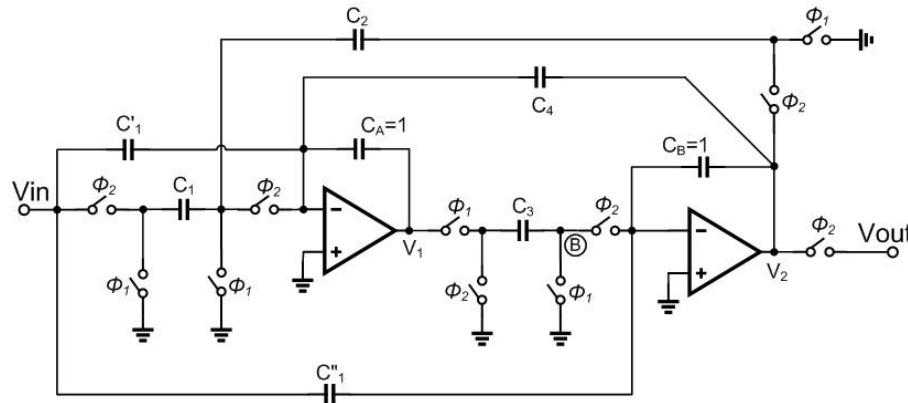
$$C_2 C_3 = 1 + b_1 + b_2 \rightarrow C_2 = C_3 = \sqrt{1 + b_1 + b_2}$$

$$C_1 = (a_0 + a_1 + a_2) / C_3$$

8 C_i values, 5 constraints. Scaling for optimum dynamic range and impedance level must follow!

High-Q Biquad

- For higher pole Q (say $Q > 4$), high-Q biquad:



$1 - b_0/b_2 = C_3 C_4 / (C_A C_B)$, and hence $1 - |z_p| \sim C_3 C_4 / (2 C_A C_B)$. Hence, even for poles very close to the unit circle, the capacitance ratios need not be very small. Also, an error in C_3/C_A is multiplied by the small factor C_4/C_B in $H(z)$, reducing the sensitivity to this error, and vice versa for an error in C_4/C_B . This makes the circuit suitable for realizing highly selective transfer functions.

High-Q Biquad – (2)

$$\frac{V_{out}}{V_{in}} = H(z) = \frac{a_m z^m + a_{m-1} z^{m-1} + \dots}{1}$$

H, z both dimensionless $\leftarrow z = e^{st}$

$$a_m = f(C_1, C_2, \dots) = f\left(\frac{C_1}{C_2}, \dots\right)$$

Approximate design equations :

$$(\omega_0 T)^2 \approx C_2 C_3 \ll 1 \quad \left(\frac{C_2 C_3}{C_A C_B} \right)$$

$$Q \approx 1 / C_4 \quad (C_A / C_4)$$

$$\text{DC Gain} = \frac{C_1}{C_2}$$

$$\text{Good choice : } C_2 = C_3 \approx \omega_0 T \ll 1$$

$$C_4 \approx 1 / Q > C_2$$

Then, $C_{\max} / C_{\min} \sim 1 / \omega_0 T$ as before.

High-Q Biquad – (3)

Exact equations:

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1'' z^2 + (C_1 C_3 + C_1' C_3 - 2C_1'') z + (C_1'' - C_1' C_3)}{z^2 + (C_2 C_3 + C_3 C_4 - 2) z + (1 - C_3 C_4)} \leftarrow \sim (z - 1)^2$$

For $b_2 = 1$, coefficient matching gives C values. Spread & sensitivities reasonable even for high Q & f_c/f_o , since C_2 , C_3 , C_4 enter only in products:

$$C_1'' = a_2$$

$$C_4 = \frac{1 - b_0}{C_3}$$

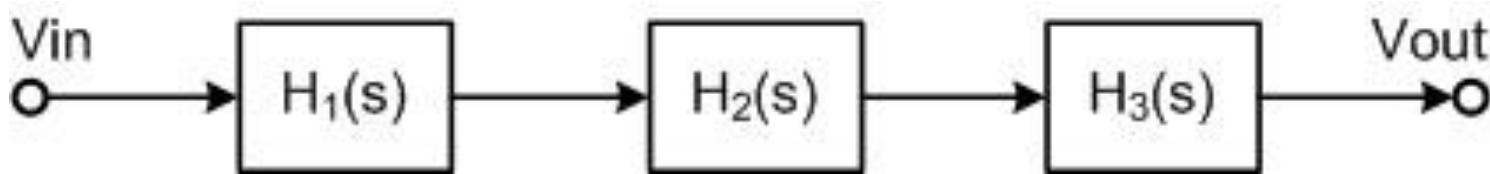
$$C_1' = \frac{a_2 - a_0}{C_3}$$

$$C_2 C_3 = 1 + b_0 + b_1$$

$$C_1 = \frac{a_0 + a_1 + a_2}{C_3}$$

$$C_2 = C_3 = \sqrt{1 + b_0 + b_1}$$

Cascade SC Filter Design



Higher-order filter can be constructed by cascading low-order ones. The $H_i(s)$ are multiplied, provided the stage outputs are buffered.

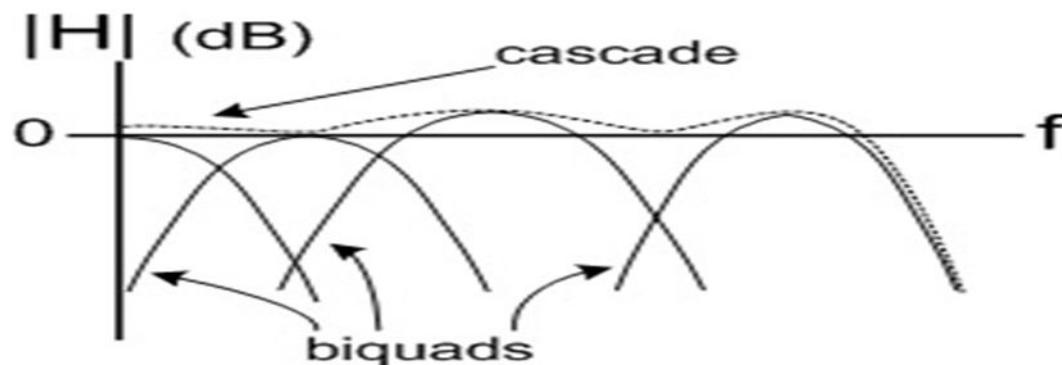
The $H_i(s)$ can be obtained from the overall $H(s)$ by factoring the numerator and denominator, and assigning conjugate zeros and poles to each biquad.

Sharp peaks and dips in $|H(f)|$ cause noise spurs in the output. So, dominant poles should be paired with the nearest zeros.

See earlier discussions (Slides 28 – 30) on ordering the stages.

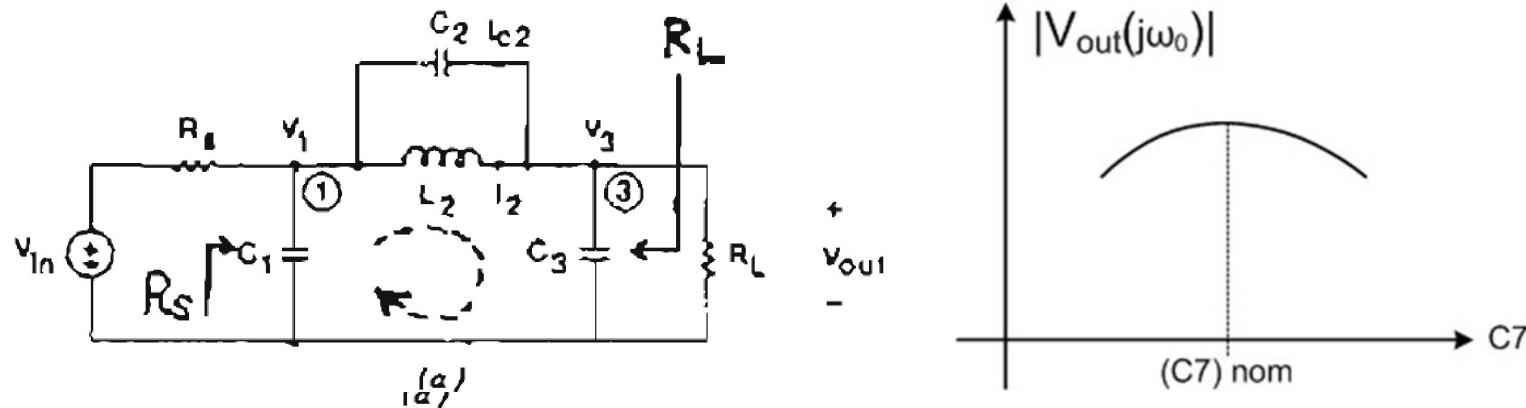
Cascade Design – (2)

Easy to design, layout, test, debug, Passband sensitivities “moderate,” 0.1 - 0.3 dB/% in passband. Stopband sensitivities good. Pairing of num. & denom., ordering of sections all affect S/N, element spread and sensitivities.



SC Ladder Filters

For optimum passband matching, for nominal $\partial V_o / \partial x \sim 0$ since V_o is maximum x values. x : any L or C.



Use doubly-terminated LCR filter prototype, with 0 flat passband loss.
State equations:

$$-V_1 = \frac{-1}{s(C_1 + C_2)} \left[\frac{V_{in} - V_1}{R_s} + sC_2V_3 - I_2 \right] \text{ KCL @ 1}$$

$$-I_2 = \frac{-1}{sL_2} [V_1 - V_3] \text{ KVL}$$

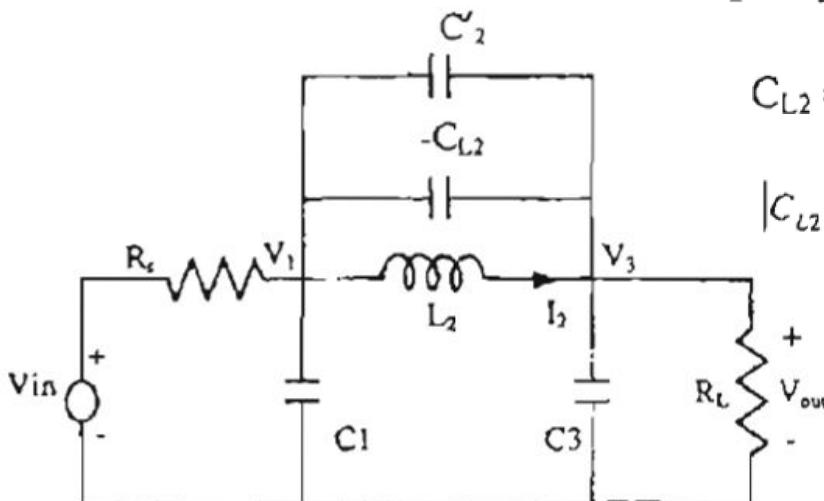
$$V_3 = \frac{-1}{s(C_2 + C_3)} \left[-sC_2V_1 - I_2 + \frac{V_3}{R_L} \right] \text{ KCL @ 3}$$

The Exact Design of SC Ladder Filters

Purpose: $H_a(s_a) \leftrightarrow H(z)$, where $s_a = \frac{2}{T} \frac{z-1}{z+1}$.

Then, gain response is only frequency warped.

Example:



Split C_2 into
 $C'_2 \equiv C_2 + C_{L2}$, and

$$C_{L2} = \frac{T^2}{4L_2},$$

$$|C_{L2}| \ll C_2$$

State equations for V_1, I_1 & V_3 :

$$-V_1 = \frac{-1}{s_a(C_1 + C'_2)} \left[\frac{-V_1 + V_{in}}{R_t} + s_a C'_2 V_3 - I_2 \right]$$

$$-I_2 = \left[s_a C_{L2} - \frac{1}{s_a L_2} \right] [V_1 - V_3]$$

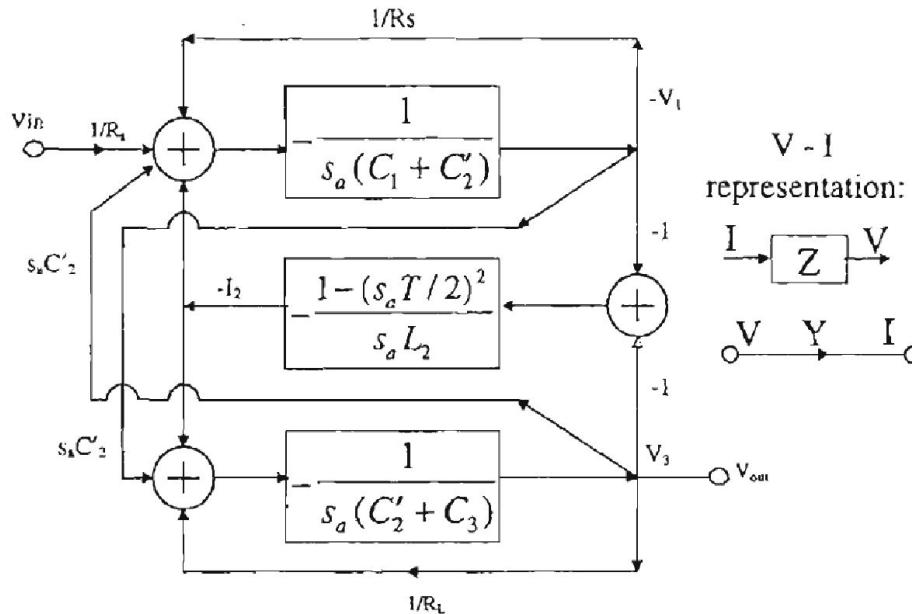
$$V_3 = \frac{-1}{s_a(C'_2 + C_3)} \left[-s_a C'_2 V_1 - I_2 + \frac{V_3}{R_L} \right]$$

Purpose of splitting C_2 :

$$H_2(s_a) = s_a C_{L2} - \frac{1}{s_a L_2} = -\frac{1 - s_a^2 L_2 C_{L2}}{s_a L_2} = -\frac{1 - (s_a T / 2)^2}{s_a L_2}$$

has a simple z-domain realization.

S_a -Domain Block Diagram



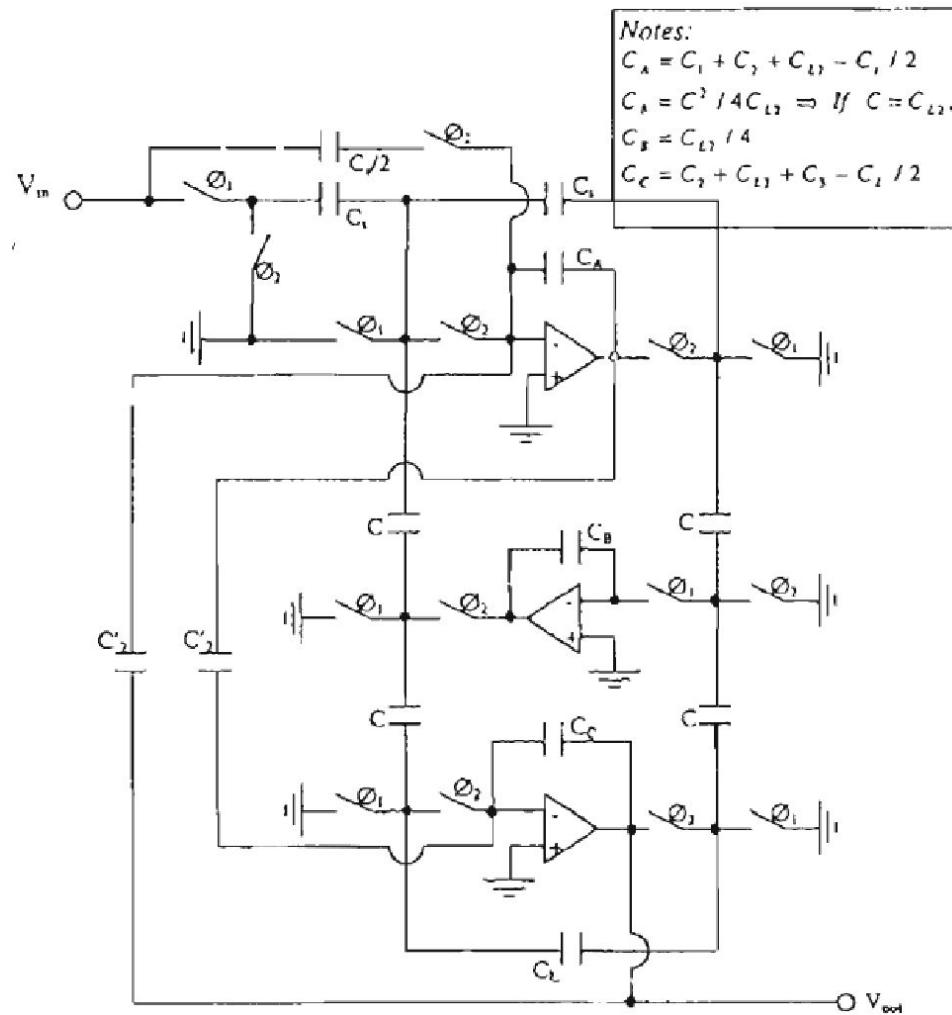
Realization of input branch: $Q_{in} = V_{in}/s_a R_s$, which becomes, $Q_{in}(z) = \frac{T}{2} \frac{(z+1)}{(z-1)} \frac{V_{in}(z)}{R_s}$

This relation can be rewritten in the form $\Delta Q_{in} = (1-z^{-1})Q_{in}(z) = \frac{T}{2R_s} (1+z^{-1})V_{in}(z)$

or, in the time domain $\Delta q_{in}(t_n) = q_{in}(t_n) - q_{in}(t_{n-1}) = \frac{C_s}{2} [v_{in}(t_n) + v_{in}(t_{n-1})]$.

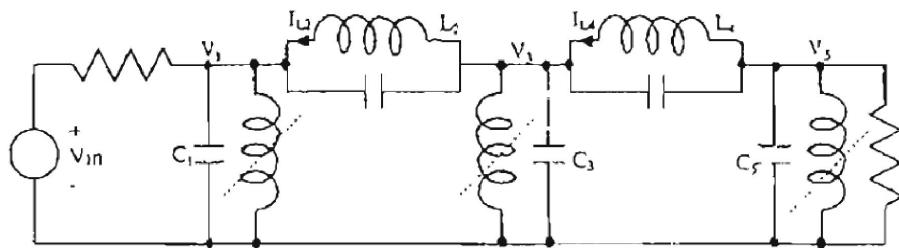
$\Delta q_{in}(t_n)$: incremental charge flow during $t_{n-1} < t < t_n$, in SCF.

SC Filter Circuit

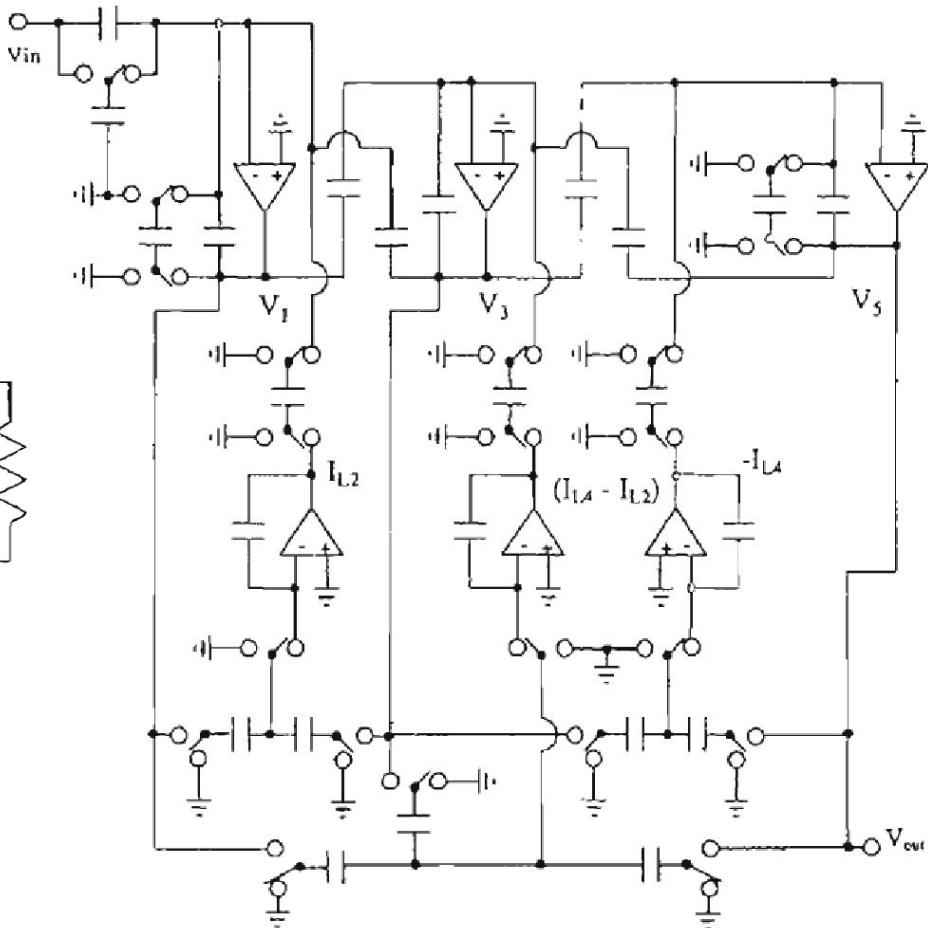


Sixth-Order SCBandpass Filter

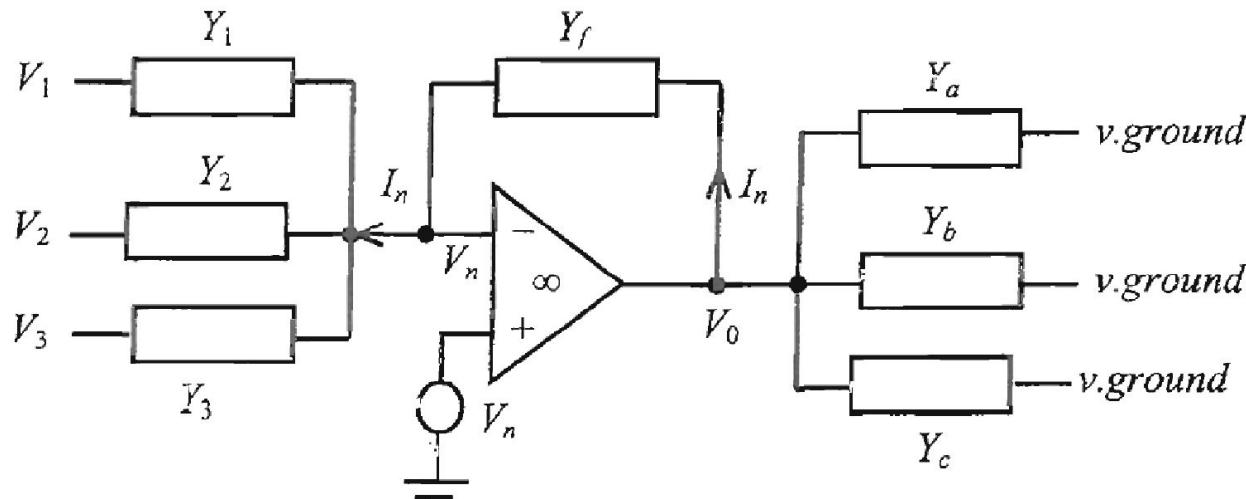
Using bandpass realization tables to obtain low-pass response gives an extra op-amp, which can be eliminated:



Sixth-order bandpass filter: LCR prototype and SC realization.



Scaling for Optimal DR and Chip Area -(1)



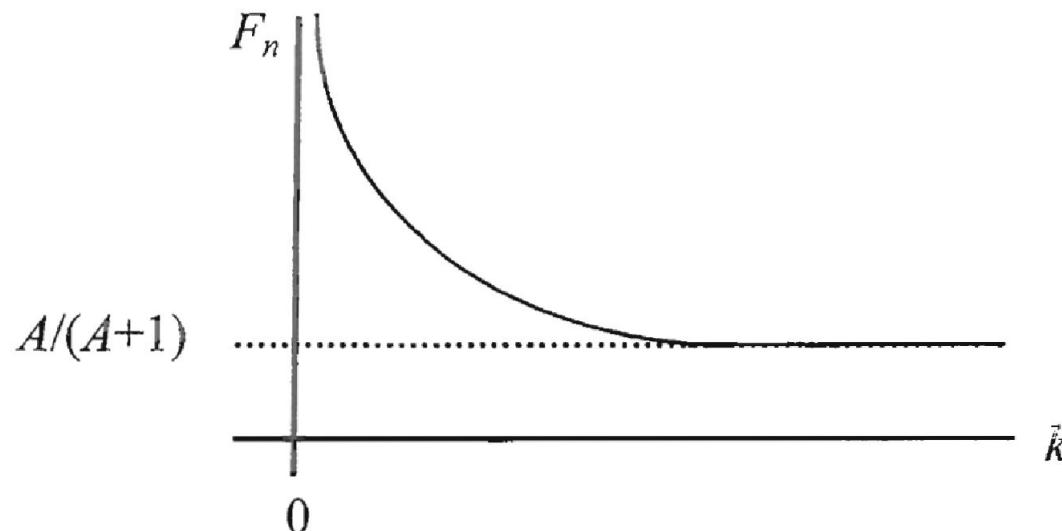
To modify $V_o \rightarrow kV_o$; $Y_i/Y_f \rightarrow kY_i/Y_f \forall i$. Hence, change Y_f to Y_f/k or Y_i to kY_i . (It doesn't matter which; area scaling makes the results the same.) To keep all output currents unchanged, also $Y_a \rightarrow Y_a/k$, etc.

$$\text{Noise gain : } V_{on} = V_0 \Big|_{V_i=0} = V_n + \frac{I_n}{Y_f} = V_n \left[1 + \frac{\sum Y_i}{Y_f} \right]$$

Scaling for Optimal DR and Chip Area –(2)

Hence, $V'_{on} = \frac{1+k \sum_i Y_i / Y_f}{1 + \sum_i Y_i / Y_f} V_{on}$. The output noise currents are also divided by k , due to $Y'_a = Y_a/k$, etc. Hence, the overall output noise from this stage changes by a factor

$$F_n = \frac{Ak+1}{(A+1)k}, \text{ where } A = \frac{\sum_i Y_i}{Y_f} : \text{the signal gain.}$$



Scaling for Optimal DR and Chip Area –(3)

The output signal does not change, so the SNR improves with increasing \underline{k} . However, the noise reduction is slower than $1/k$, and also this noise is only one of the terms in the output noise power.

If $V_o > V_{DD}$, distortion occurs, hence $k \leq k_{max}$ is limited such that Y_o saturates for the same V_{in} as the overall V_{out} . Any $k > k_{max}$ forces the input signal to be reduced by \underline{k} so the SNR will now decrease with \underline{k} .

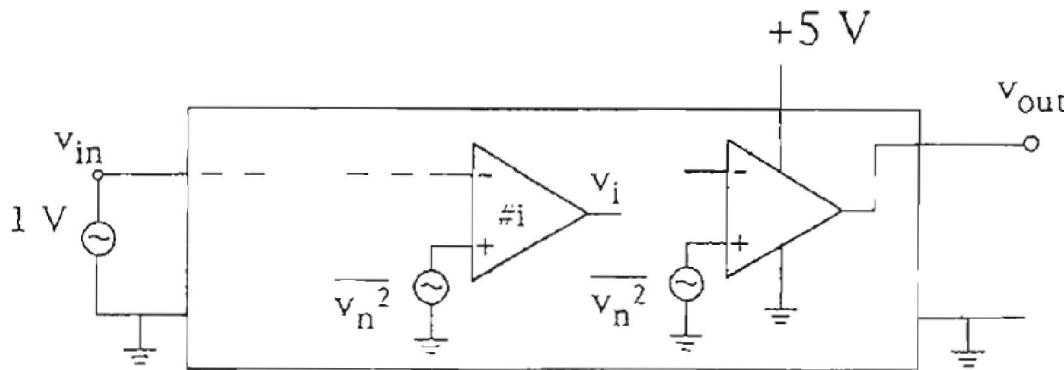
Conclusion: k_{max} is optimum, if settling time is not an issue.

Scaling of SCF's. – (1)

Purposes :

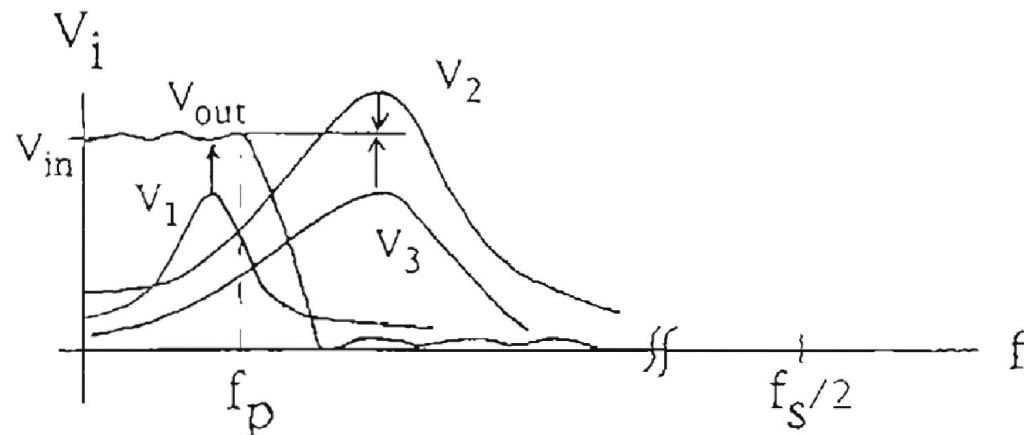
1. Maximum dynamic range
2. Minimum C_{max} / C_{min} , $\sum C / C_{min}$
3. Minimum sens. to op-amp dc gain effects.

1. Dynamic range scaling:



Assume that opamps have same input noise v_n^2 , and max. linear range $|V_{max}|$. For an optimum dynamic range $V_{in\ max} / V_{in\ min}$, each opamp should have the same $V_{imax}(f)$, so they all saturate at the same $V_{in\ max}$. Otherwise, the S/N of the op-amp is not optimal. May also use histograms!

Scaling of SCF's. – (2)



To achieve $V_{1 \max} = V_{2 \max} = \dots = V_{out \max}$, use amplitude scaling:

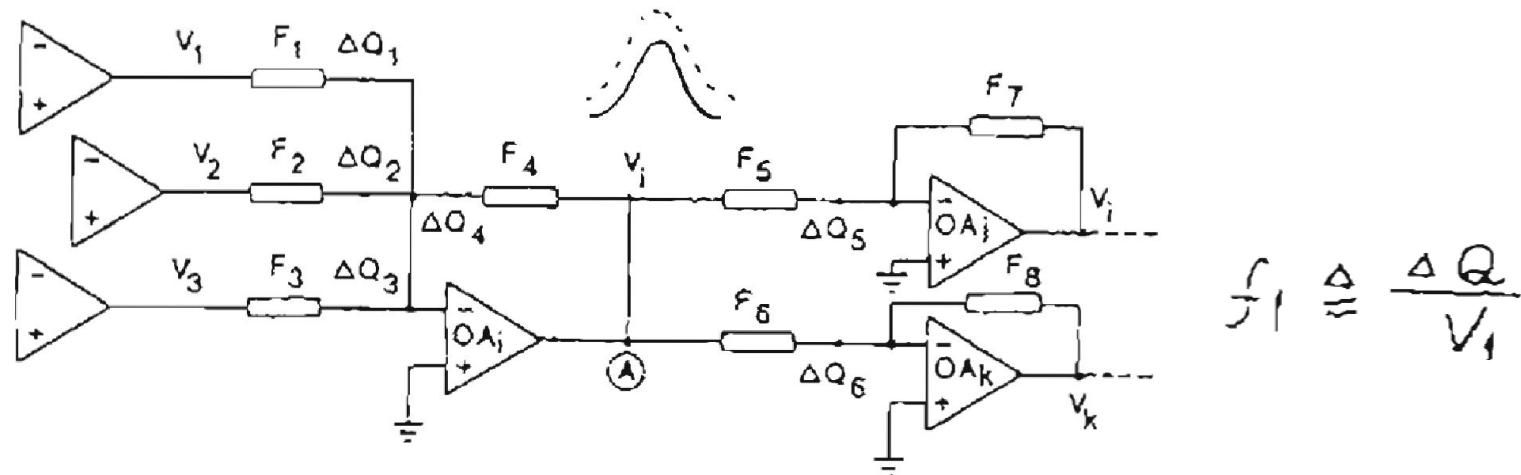
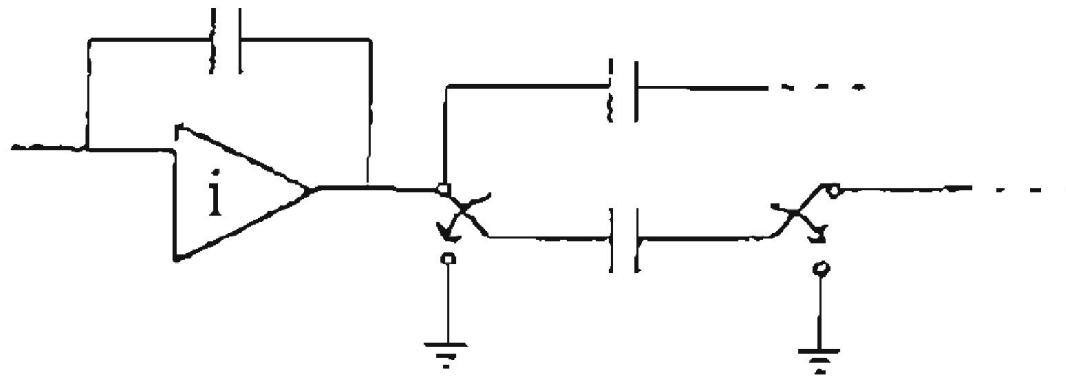


Figure 5.17 SC filter section.

Scaling of SCF's. – (3)

Simple rule:

Multiply all C_j connected or switched to the output of opamp i by k_i !



Scaling of SCF's. – (4)

2. Minimum C_{max}/C_{min} :

If all $f_n(z)$ & $h(z)$ are multiplied by the same I_i , nothing will change. Choose $I_i = C_{min} / C_{i min}$ where $C_{i min}$ is the smallest C connected to the input of op-amp i , and C_{min} is the smallest value of cap. permitted by the technology (usually $0.1 \text{ pF} \leq C_{min} \leq 0.5 \text{ pF}$ for stray-insensitive circuits). Multiply all caps connected or switched to opamp input by I_i . Big effect on C_{max}/C_{min} !

3. Sensitivities:

The sensitivity of the gain to C_k remain unchanged by scaling; However, the sensitivity to finite op-amp gain effects is very much reduced. Optimum dynamic-range scaling is nearly optimal for dc gain sens. as well.

Scaling of SCF's. – (5)

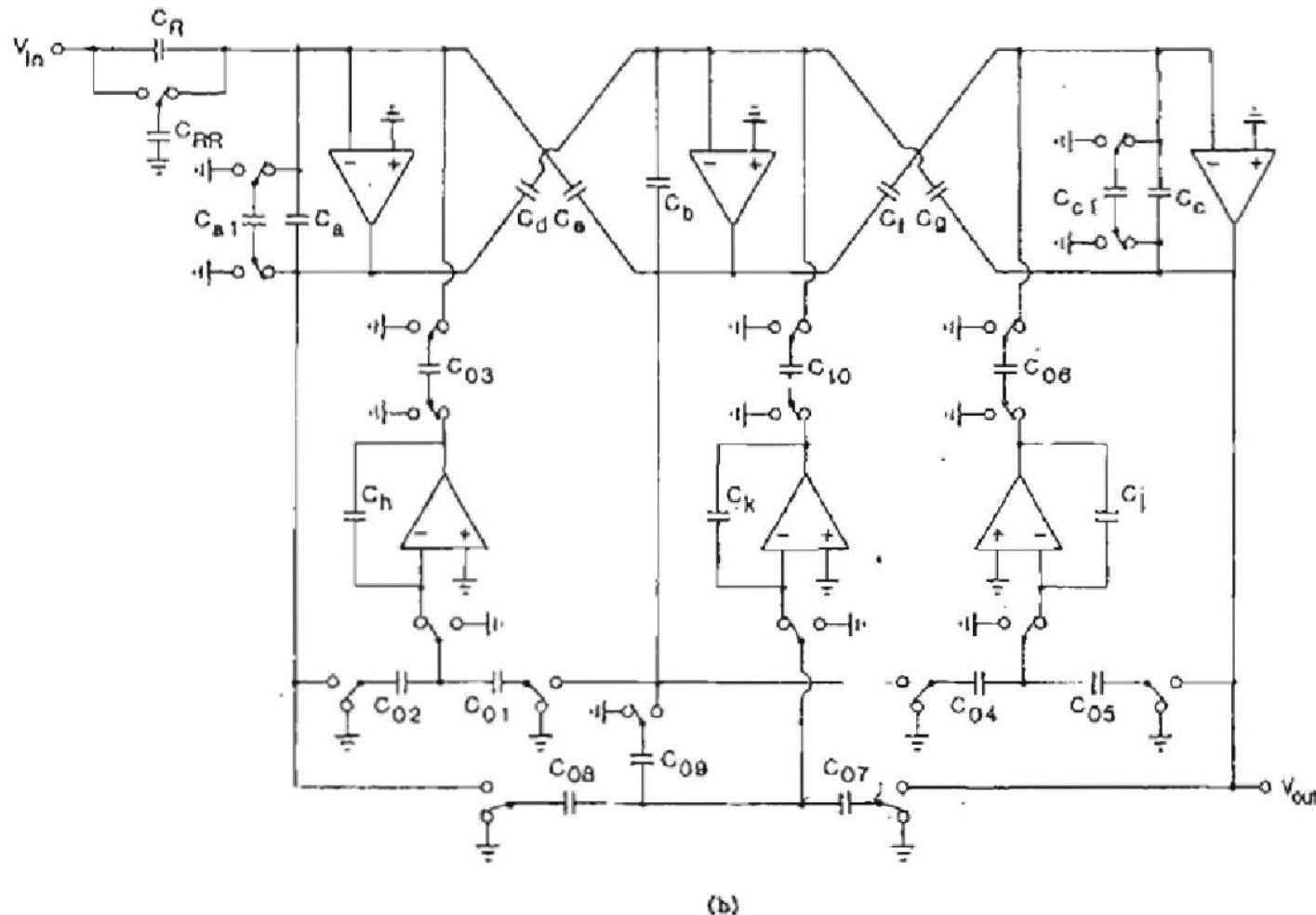
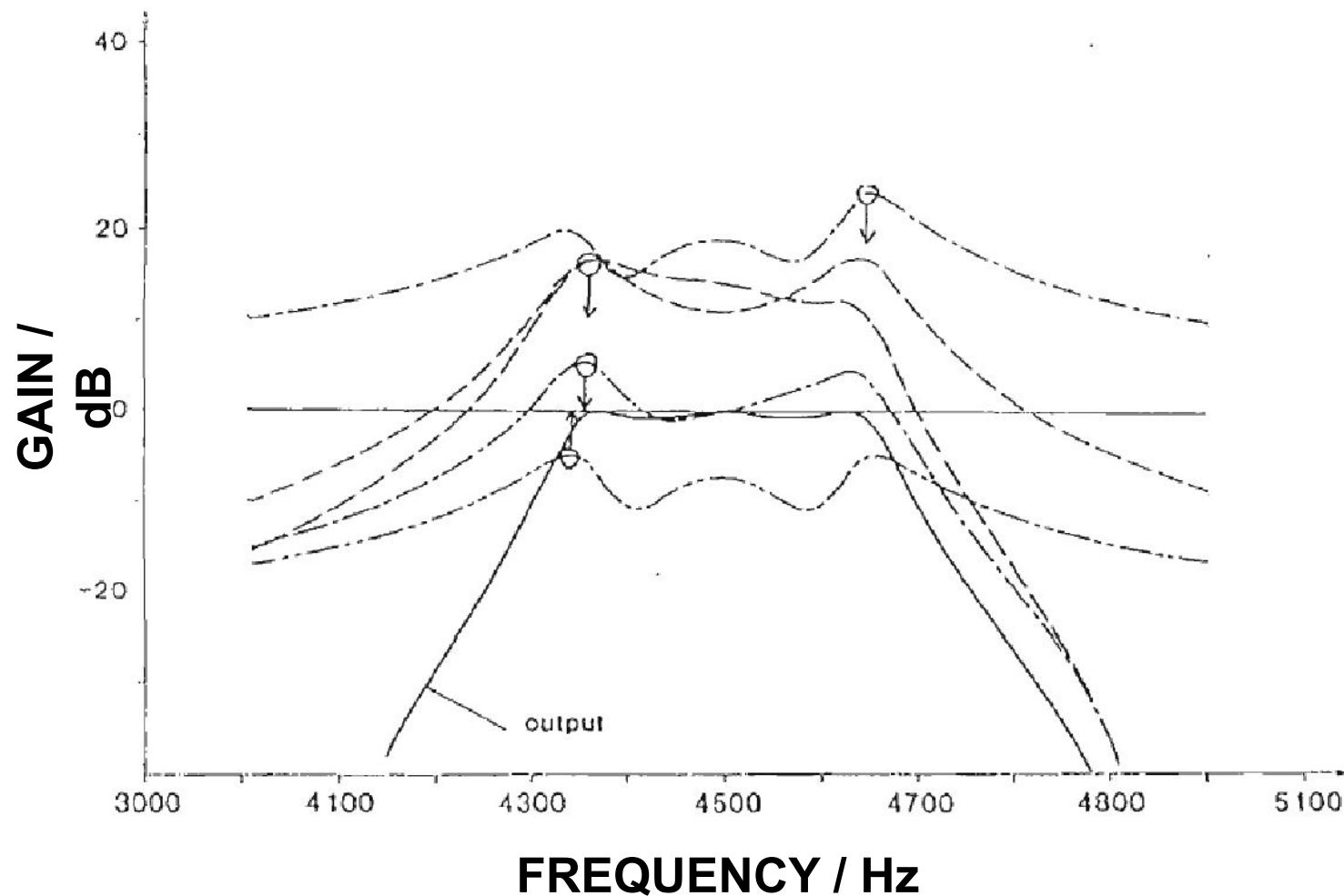
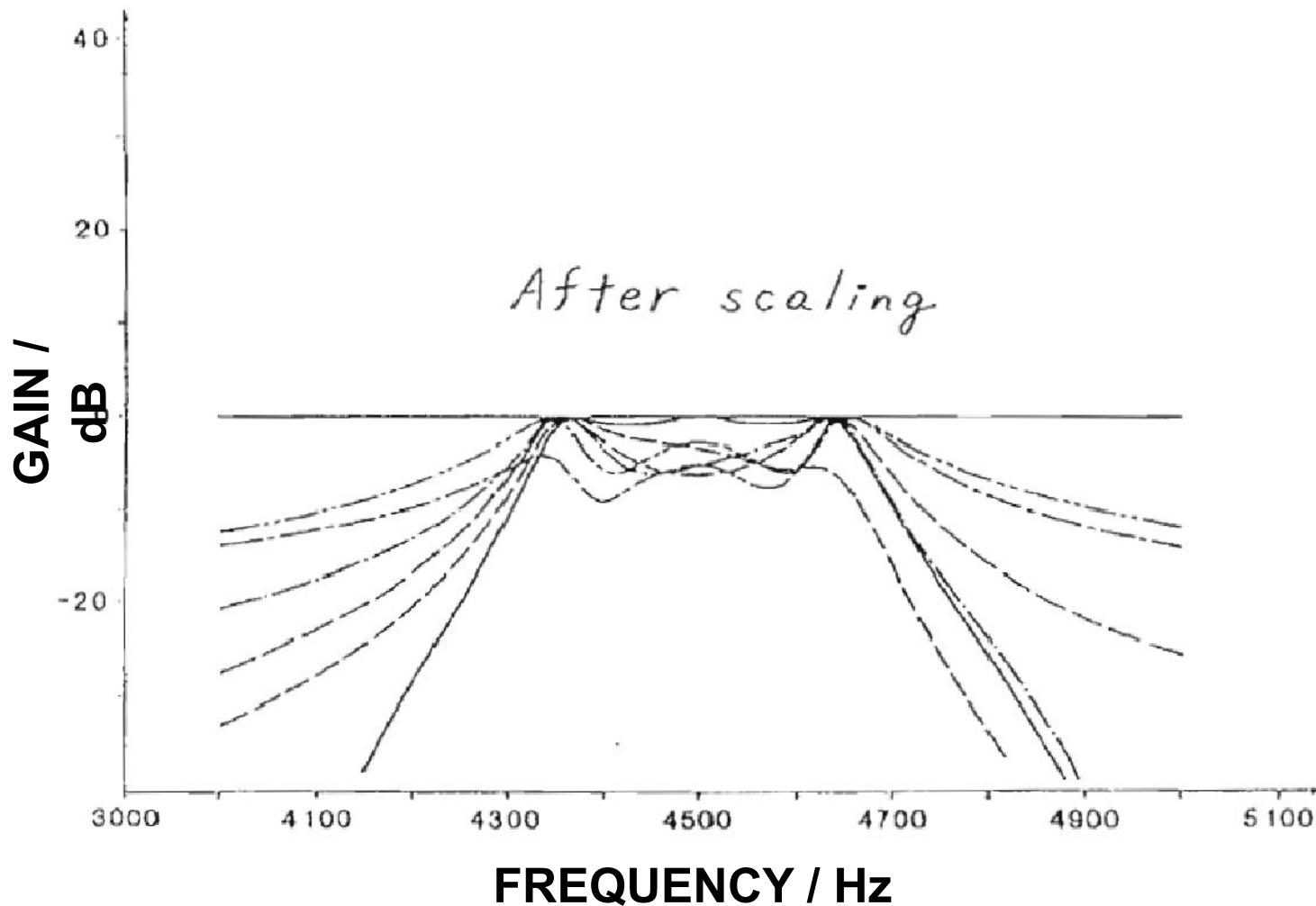


FIGURE 5.36. Sixth-order bandpass filter: (a) LCR prototype; (b) SC realization.

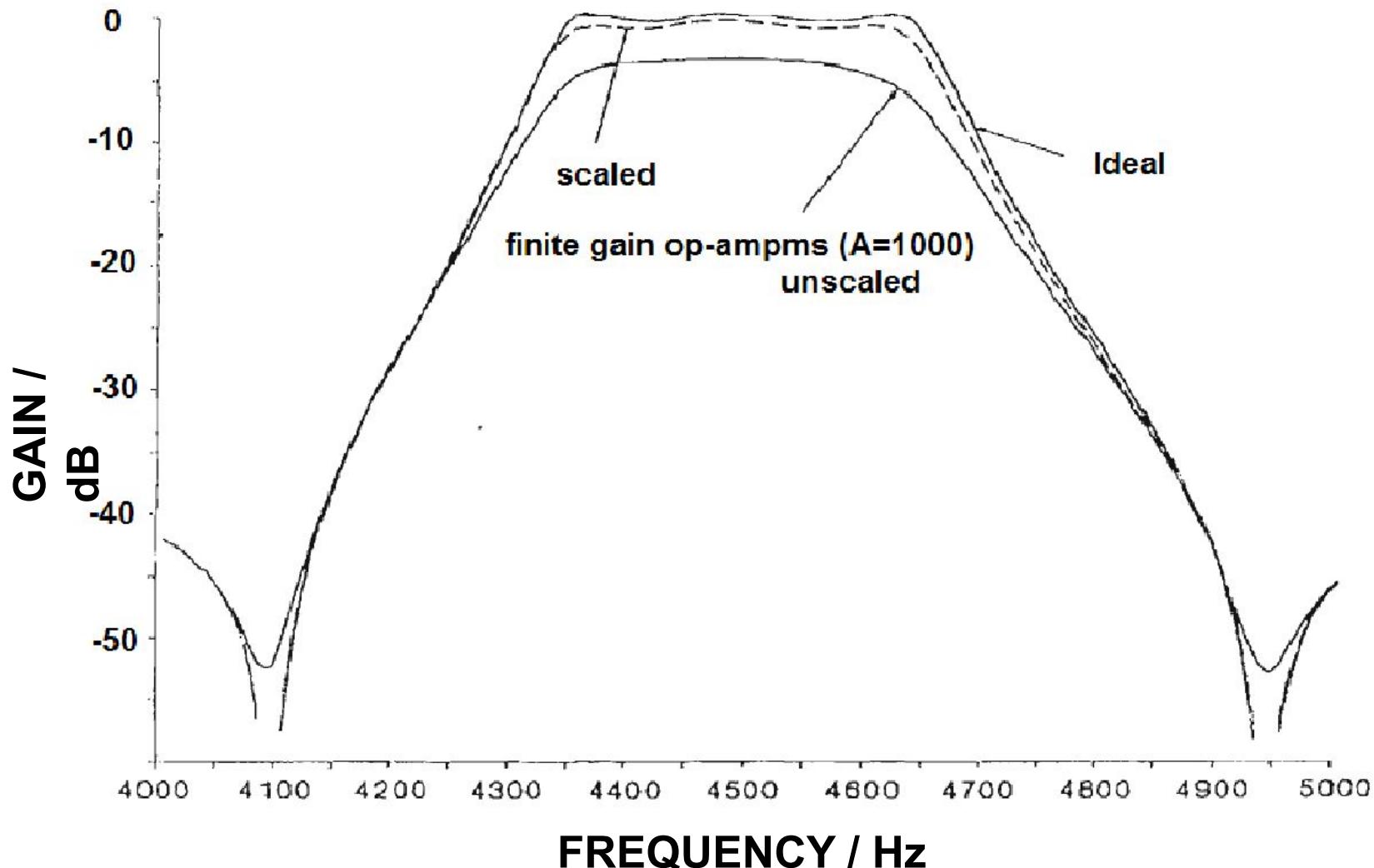
Scaling of SCF's. – (6)



Scaling of SCF's. – (7)

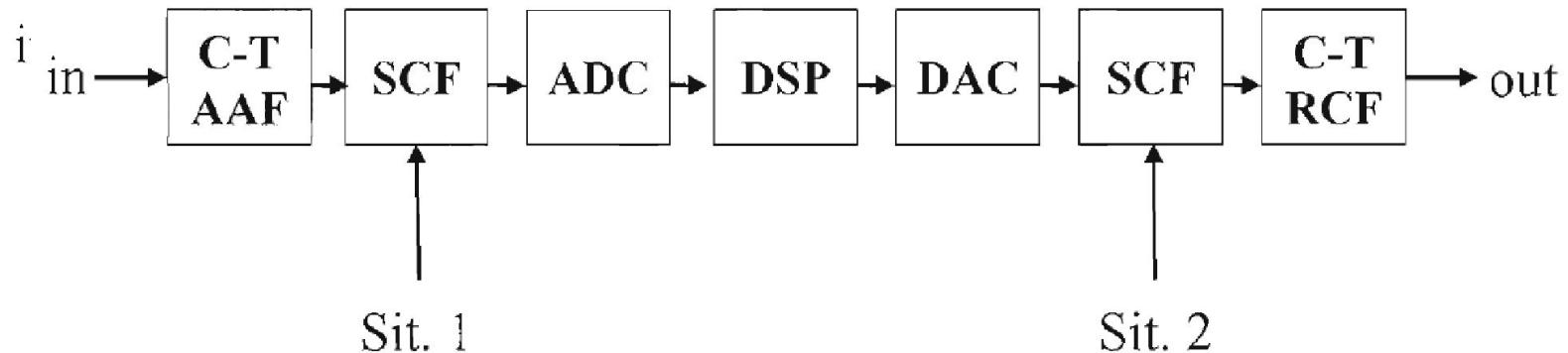


Scaling of SCF's. – (8)



SC Filters in Mixed-Mode System

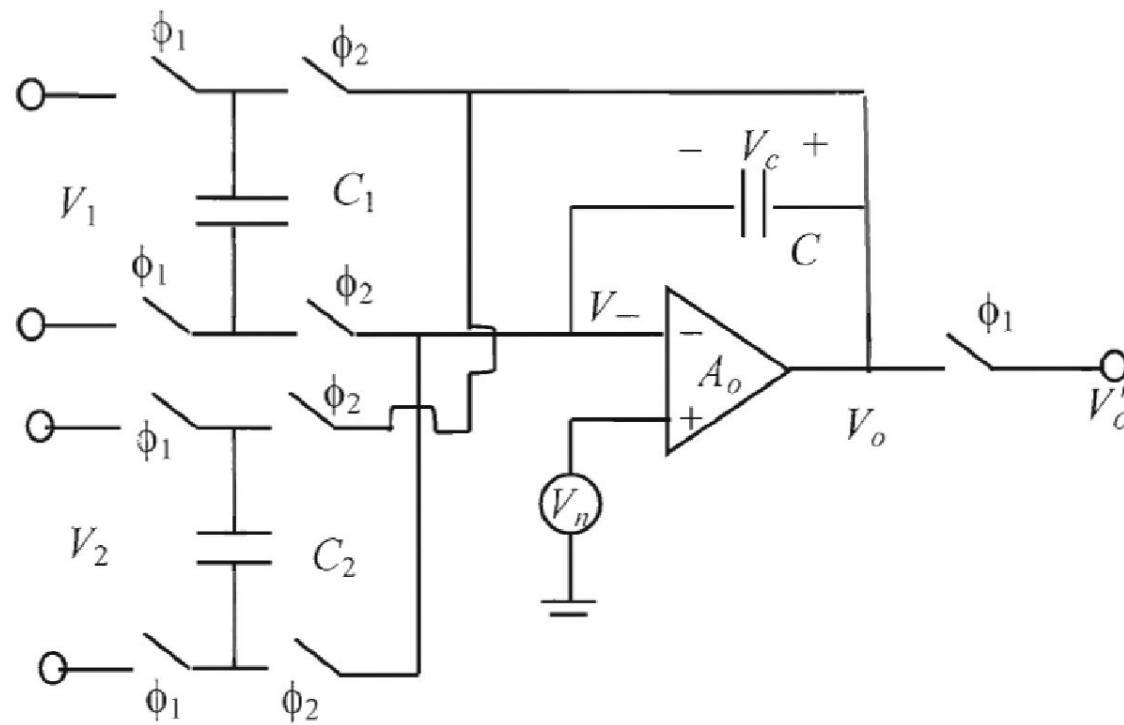
Two situations; example:



Situation 1: Only the sampled values of the output waveform matter; the output spectrum may be limited by the DSP, and hence $V_{RMS,n}$ reduced.

Situation 2: The complete output waveform affects the *SNR*, including the S/H and direct noise components. Usually the S/H dominates. Reduced by the reconstruction filter.

Direct-Charge-Transfer Stage – (1)



Advantages:

Opamp does not participate in charge transfer \rightarrow no slewing distortion, clean S/H output waveform. Finite DC gain A , introduces only a scale factor $K = 1/[1+1/A_o]$.

Direct-Charge-Transfer Stage – (2)

Analysis gives

$$V'_o(z) = K \cdot [V'_{o,ideal}(z) + V_n(z)]$$

where

$$V'_{o,ideal} = [C_1 \cdot V_1(z) + C_2 \cdot V_2(z)] / [(C + C_1 + C_2) - C/z]$$

is the ideal lowpass filter response.

Applications:

- SC-to-CT buffer in smoothing filter for D-S DAC (Sooch et al., AES Conv., Oct. 1991)
- DAC + FIR filter + IIR filter (Fujimori et al., JSSC, Aug. 2000).

Double Sampled Data Converter – (1)

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 32, NO. 12, DECEMBER 1997

1907

Low-Voltage Double-Sampled $\Sigma\Delta$ Converters

Daniel Senderowicz, *Member, IEEE*, Germano Nicollini, Sergio Pernici, Angelo Nagari, *Member, IEEE*, Pierangelo Confalonieri, and Carlo Dallavalle, *Member, IEEE*

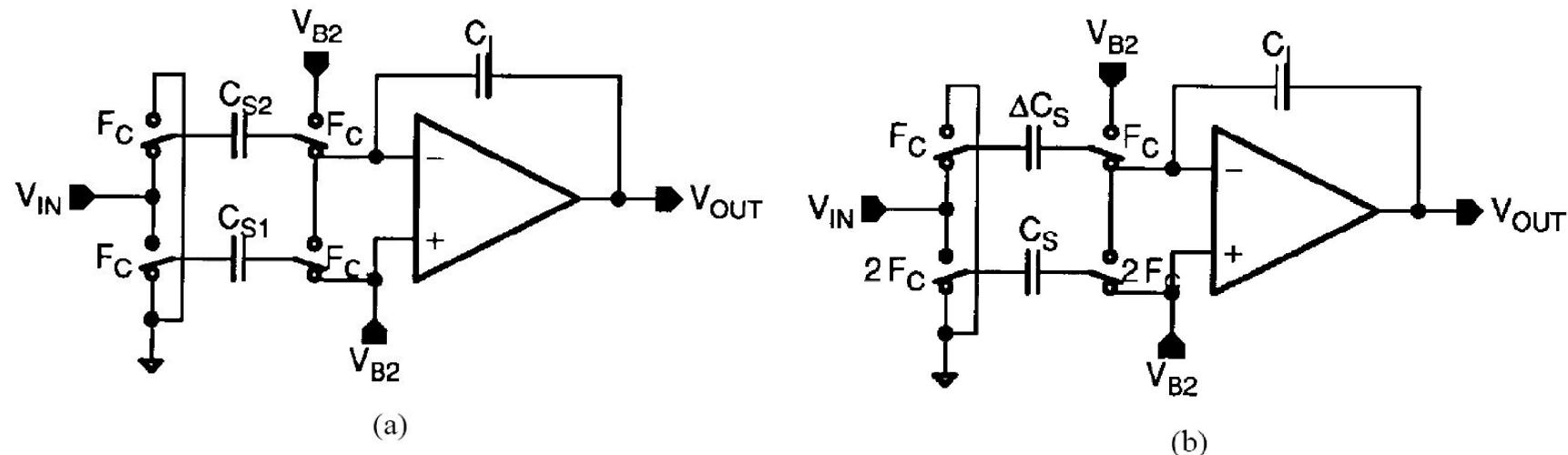
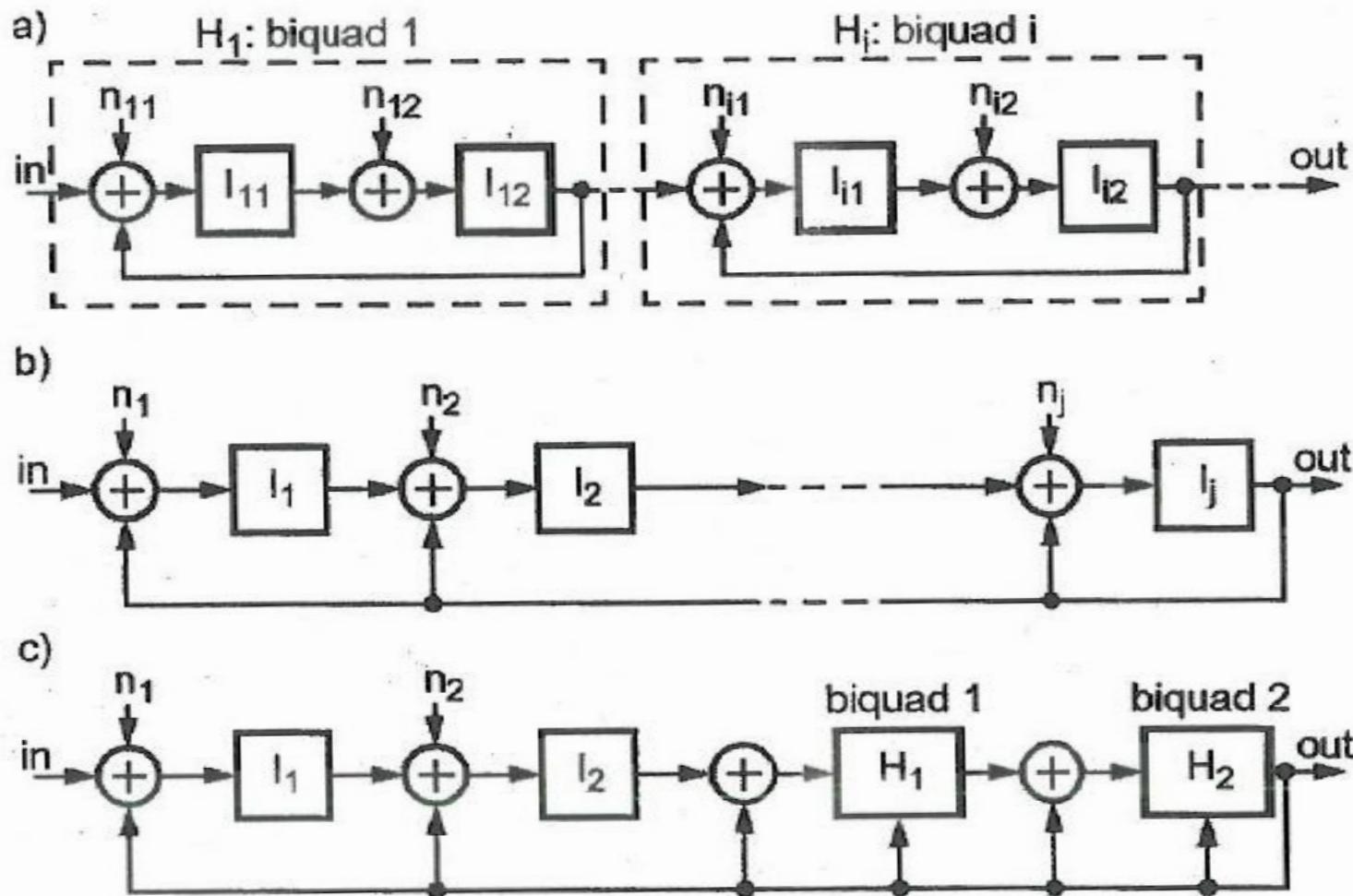


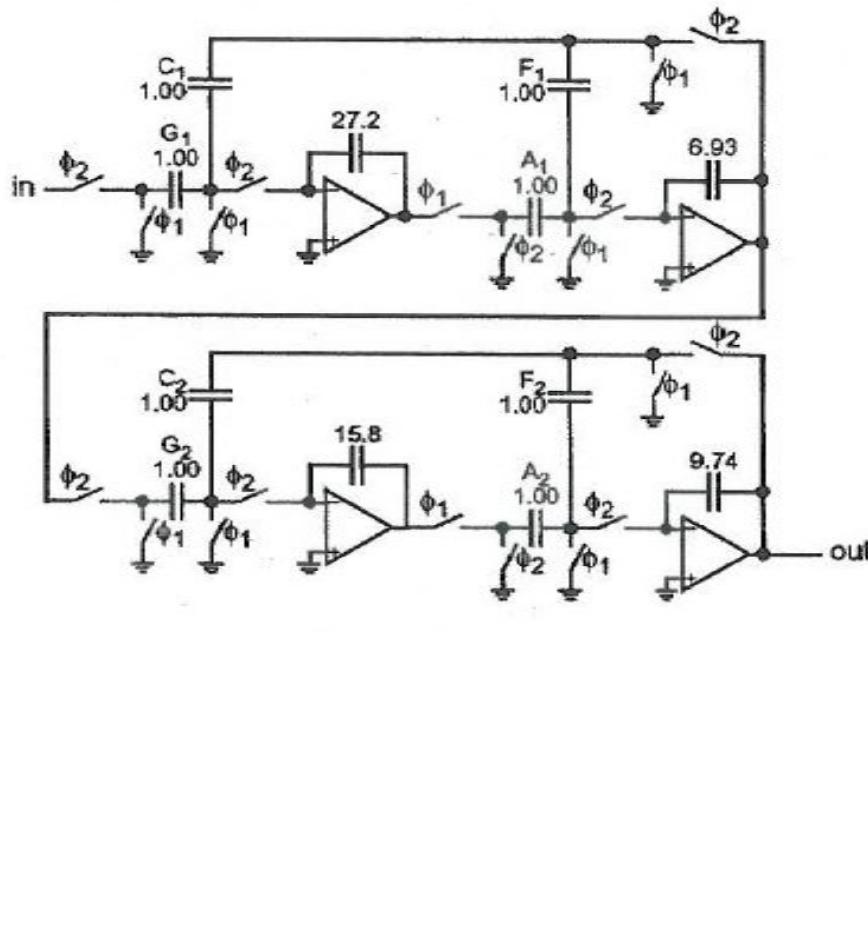
Fig. 2. (a) Simplified conventional double-sampled SC integrator. (b) Equivalent conventional double-sampled SC integrator.

Reconstruction Filter Architectures

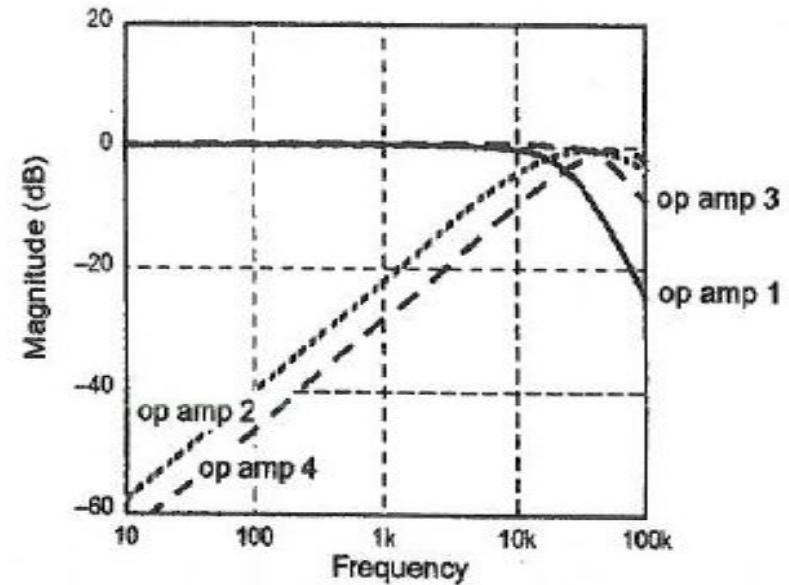


Post-Filter Examples (1)

A 4th-order Bessel filter implemented with a cascade of biquads

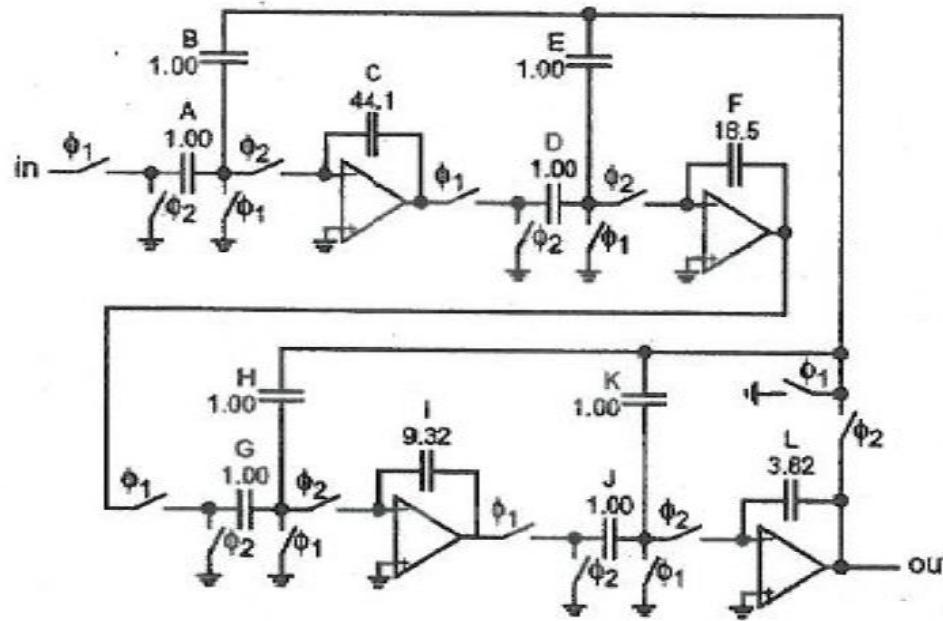


Noise gains from each op-amp input

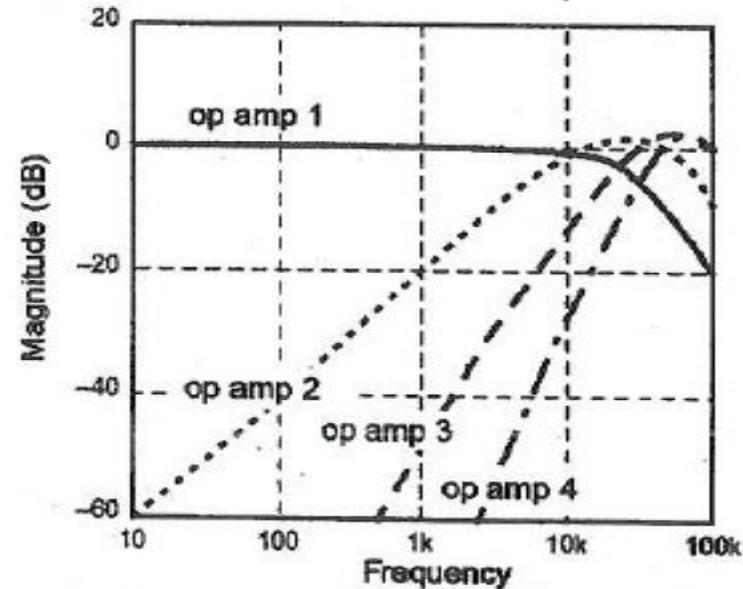


Post-Filter Examples (2)

A 4th-order Bessel filter implemented with the inverse follow-the-leader topology



Noise gains from each op-amp input



References

- [1] R. Schaumann et al., Design of Analog Filters (2nd edition), Oxford University Press, 2010.
- [2] D. A. Johns and K. Martin, Analog Integrated Circuits, Wiley, 1997. 2nd ed., 2012.
- [3] R. Gregorian and G. C. Temes, Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986.
- [4] Introduction to Circuit Synthesis and Design, G. C. Temes and J. W. LaPatra, McGraw-Hill, 1977.
- [5] John Khoury, Integrated Continuous-Time Filters, Unpublished Lecture Notes, EPFL, 1998.
- [6] P. Kurahashi et al., “A 0.6-V Highly Linear Switched-R-MOSFET-C Filter, CICC, Sept. 2006, pp. 833-836.

Nonidealities in SC Circuits

- **Switches:**

- Nonzero “on”-resistance

- Clock feedthrough / charge injection

- Junction leakage, capacitance

- Noise

- **Capacitors:**

- Capacitance errors

- Voltage and temperature dependence

- Random variations

- Leakage

- **Op-amps:**

- DC offset voltage

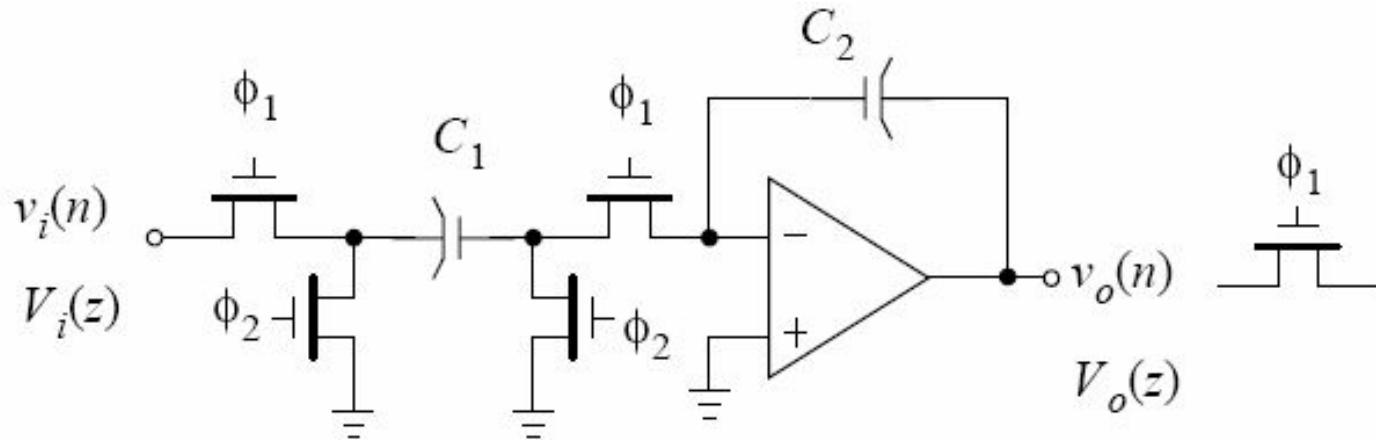
- Finite dc gain

- Finite bandwidth

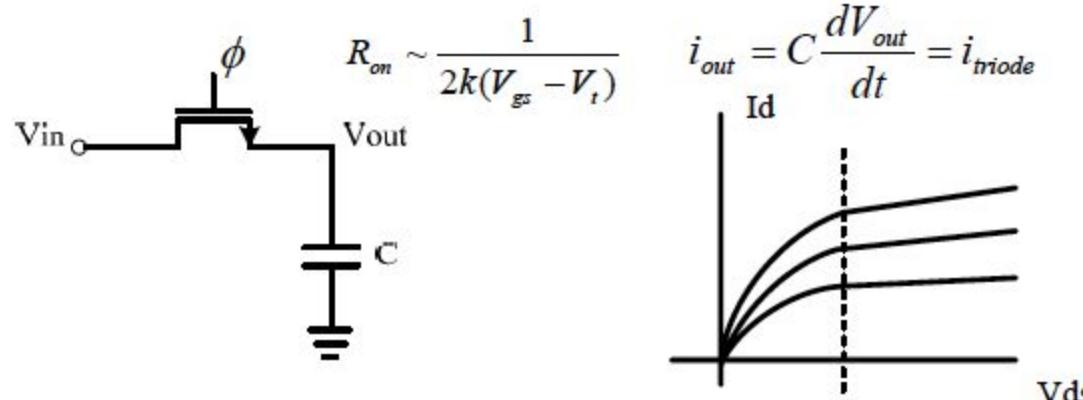
- Nonzero output impedance

- Noise

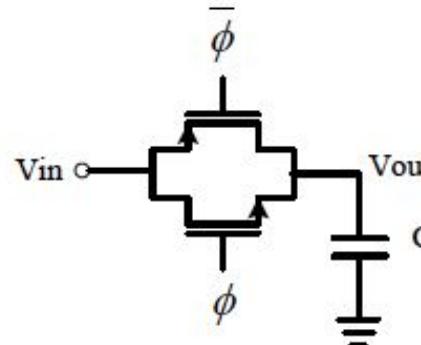
Switched-Capacitor Integrator



Nonzero Switch “On”-Resistance

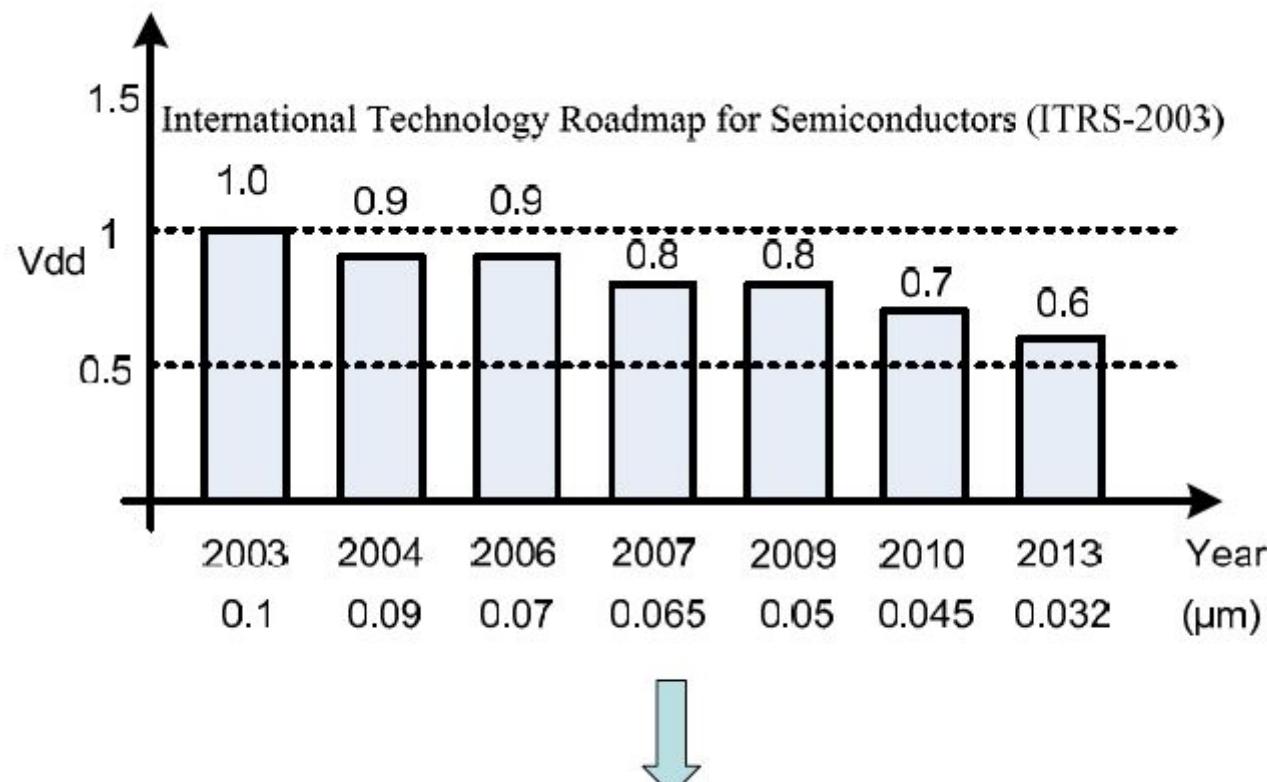


C is charged exponentially. Time constant must be sufficiently low.
Body effect must be included!

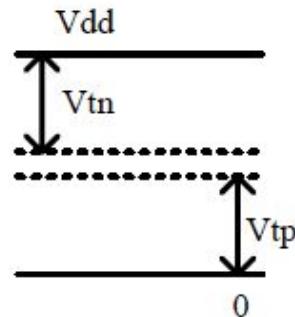
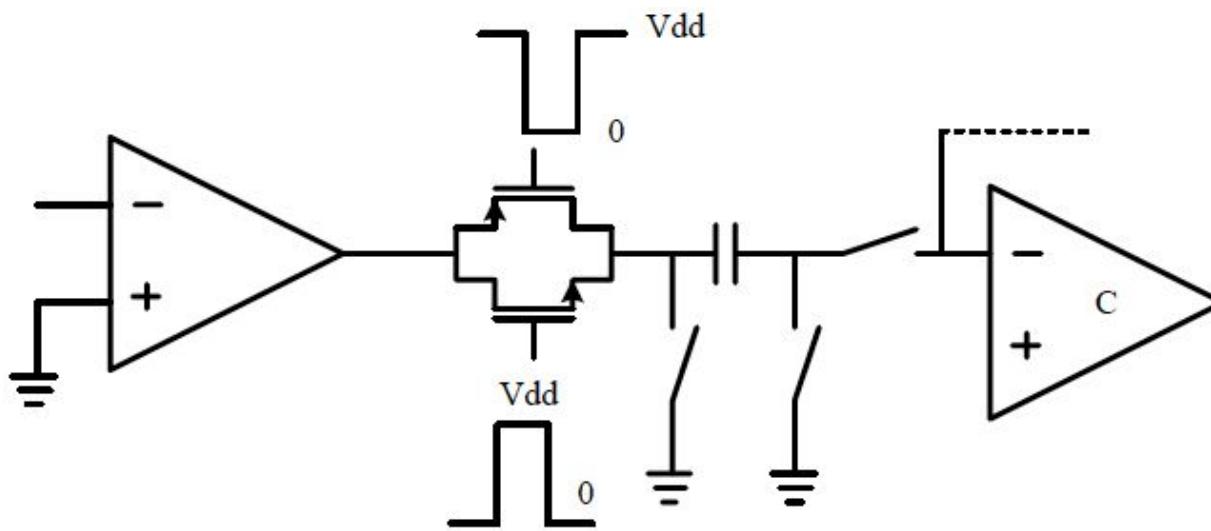


To lower on-resistance and clock feedthrough: CMOS gate; $W_p, L_p = W_n, L_n$. For settling to within 0.1%, $T_{\text{settling}} > 7R_{\text{on}}C$ (worst-case R_{on}).

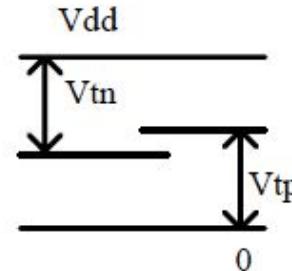
Digital CMOS Scaling Roadmap



Floating Switch Problem in Low-Voltage



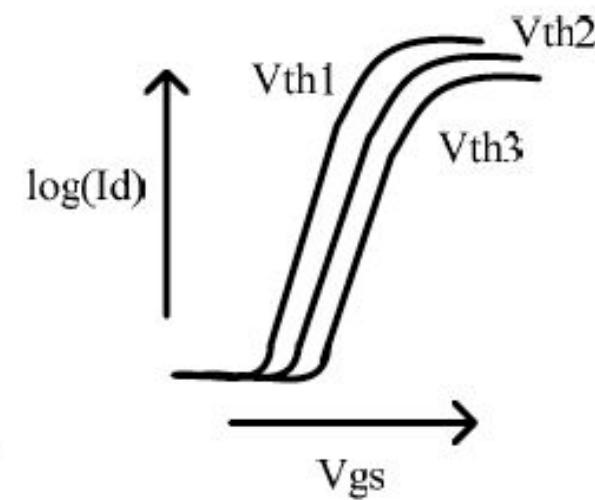
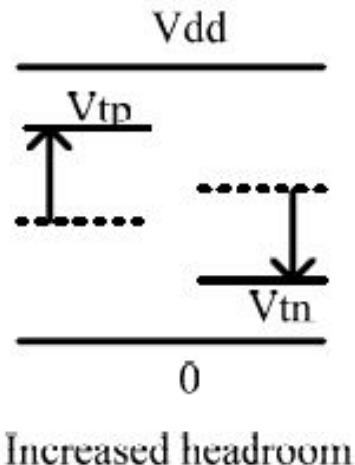
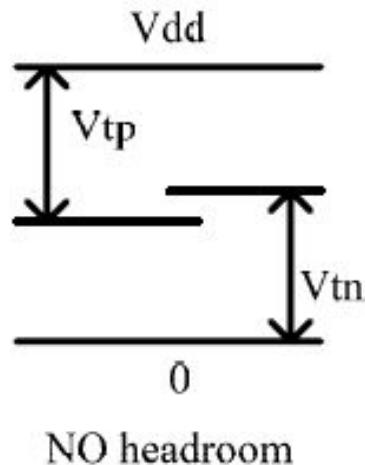
Small headroom



NO headroom

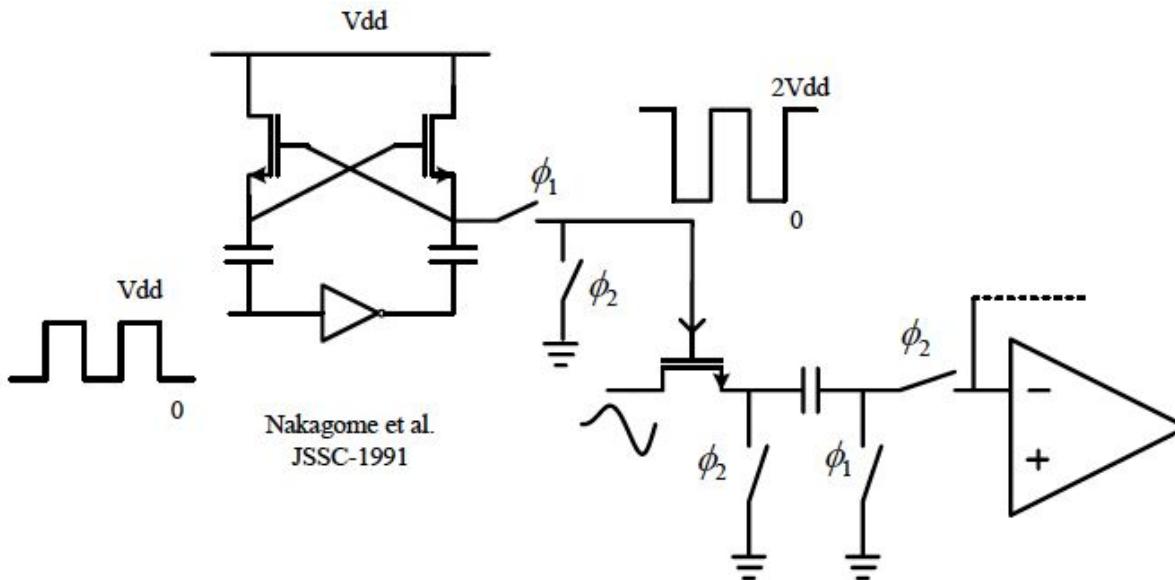
Using Low-Threshold Transistors

- Precise control over process and temperature difficult
- Switch leakage worsens as threshold voltage is lowered (i.e. hard to turn off)



Using Clock Voltage Booster

- Boosted clock voltage (e.g. $0 \square 2V_{dd}$) is used to sufficiently overdrive the NMOS floating switch – useful in systems with low external power supply voltage and fabricated in high-voltage CMOS process
 - Voltage limitation is violated in low-voltage CMOS



Floating Switch Driver

Replacing Vdd by Vin, circuit:

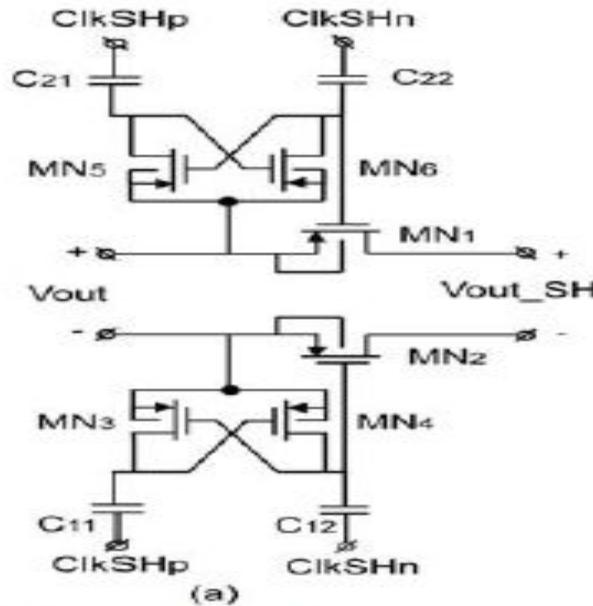
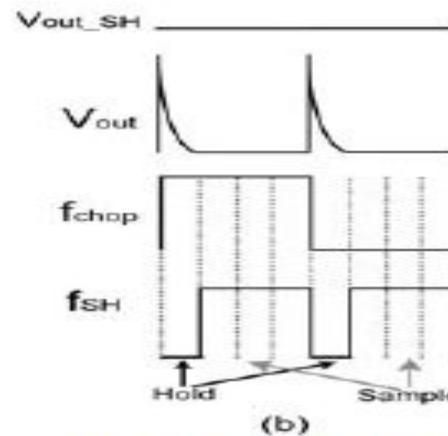


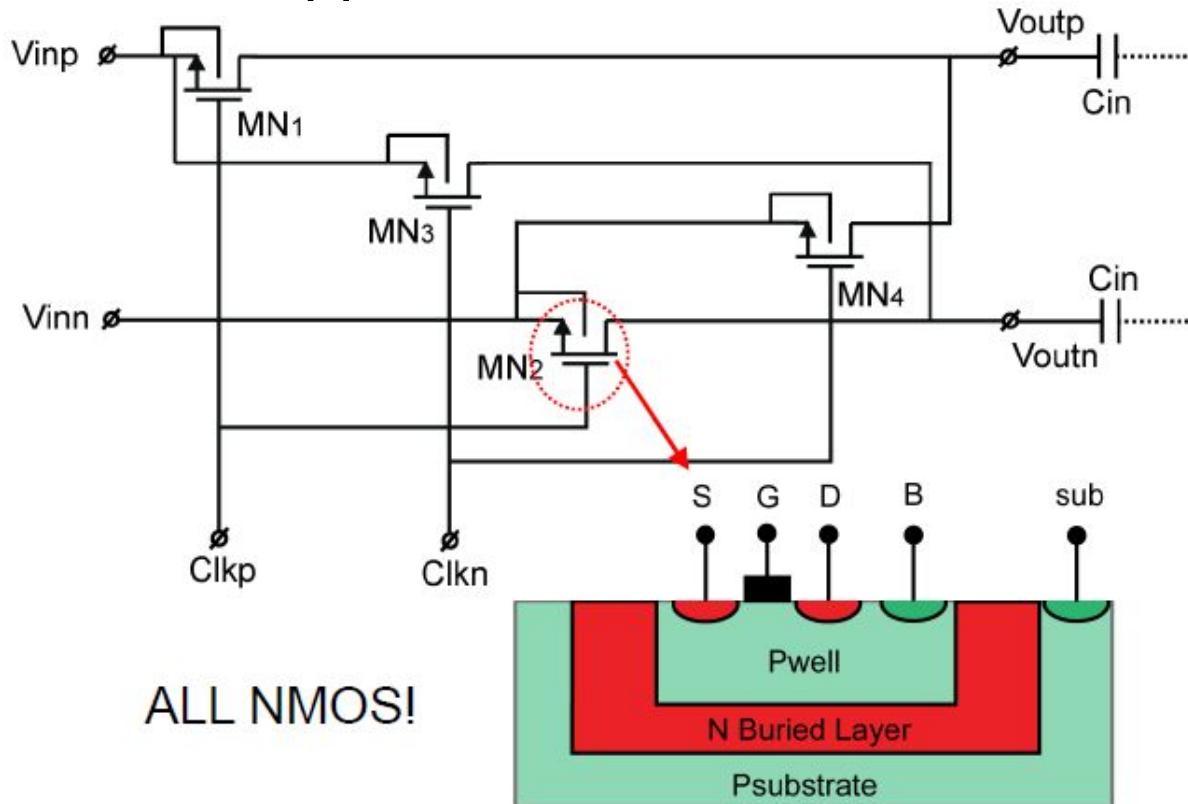
Figure 21.9.3: Schematic of the output sample and hold switches (a) and their timing diagram (b).

Q. Fan, Huijsing and K. Makinwa, "A capacitively coupled ...", Digest ISSCC 2012, pp. 374-375.



Application to Chopper

- All NMOS chopper:

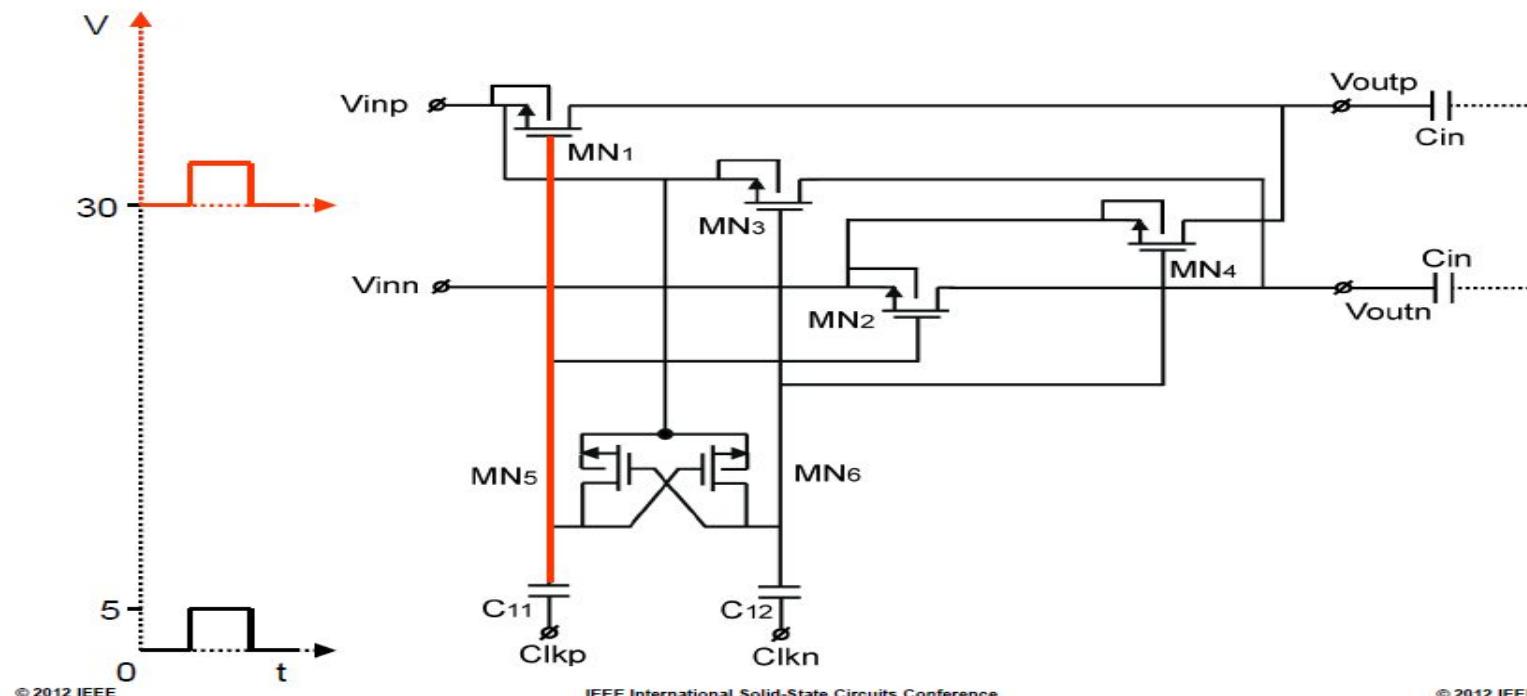


- Q. Fan, H. Jiang and R. Makihara, "A capacatively coupled ... , Digest ICSC 2012, pp. 374-375

Chopper Switch Driver

- Using the cross-coupled switch drivers:

High-voltage Input Chopper



- Q. Fan, Huijsing and K. Makinwa, "A capacitively coupled ...", Digest ISSCC 2012, pp. 374-375

Using Bootstrapped Clock

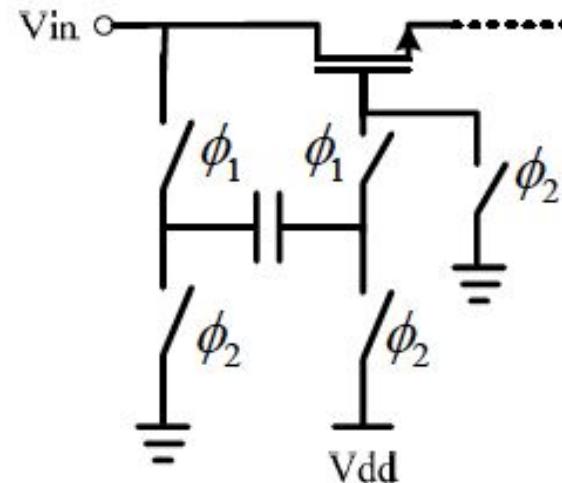
Abo et al., JSSC-1999

Steensgaard, ISCAS-1999

Singer et al., ISSCC-2000

Dessouky et al., JSSC-2001

(fast) Hernes et al., ISSCC-2004

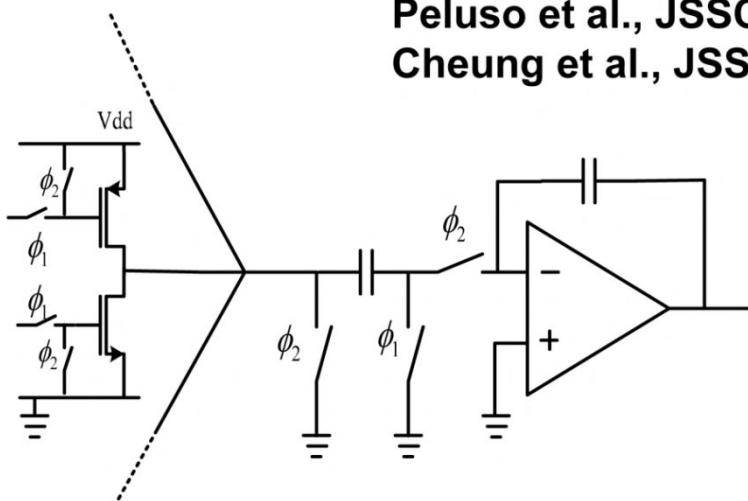


- Principle: pre-sample V_{dd} before placing it across V_{gs} (various low-voltage issues complicate implementation)
- Input sampling such as this can be used for low-voltage CMOS or for high-linearity sampling
- No fundamental or topological limitation on higher input signal frequency w.r.t. sampling frequency

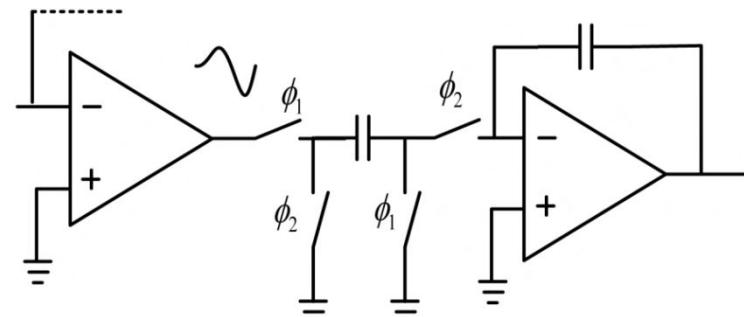
Switched-Opamp Technique

- Floating switch is eliminated
- Opamp output tri-stated and pulled to ground during reset ϕ_2
 - Slow transient response as opamp is turned back on during ϕ_1

Crols et al., JSSC-1994(1.5-V)
Peluso et al., JSSC-1997(1.5-V)
Baschirotto et al., JSSC-1997(1-V)
Peluso et al., JSSC-1998(1-V)
Cheung et al., JSSC-2002 (1-V)



Switched-opamp integrator



Conventional integrator

Switched-Opamp Example

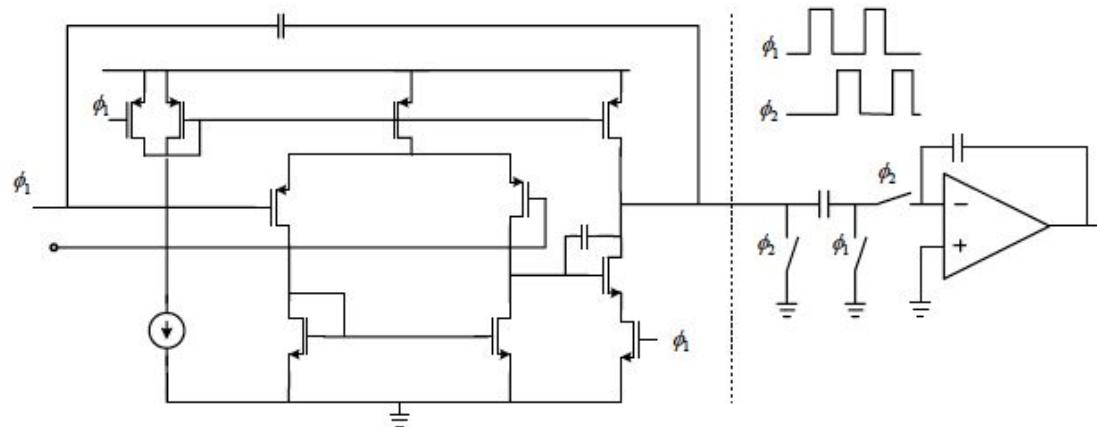
Crols et al., JSSC-1994

Peluso et al., JSSC-1997

The entire opamp is turned off during ϕ_2 .

Demonstrated 1.5-V operation ($\Delta\Sigma$) with $V_{tn}=|V_{tp}|=0.9V$.

115kHz at -60dB THD & 500kHz at -72dB THD.



→ Baschirotto JSSC-1997: 1-V operation

→ Peluso JSSC-1998: 0.9-V operation

1.8MHz at -40dB THD

Cheung et al., JSSC-2002(1-V)

Opamp-Reset = Unity-Gain Configuration

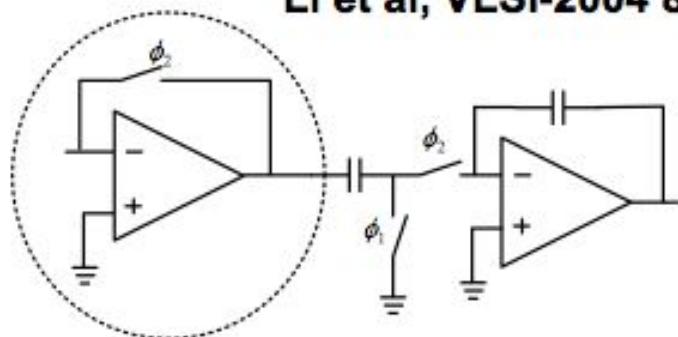
Bidari et al., ISCAS-1999

Keskin et al, ESSCIRC-2001 & JSSC-2002

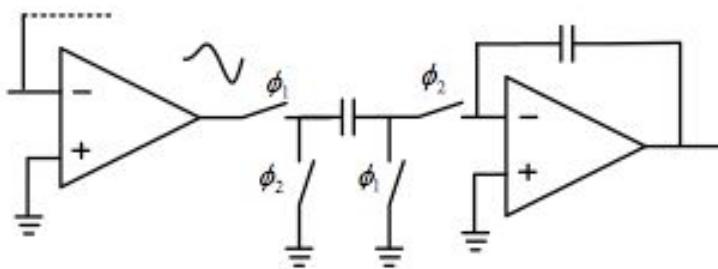
Chang et al, CICC-2002 & JSSC-2003

Chang et al, VLSI-2003 & TCAS1-2005

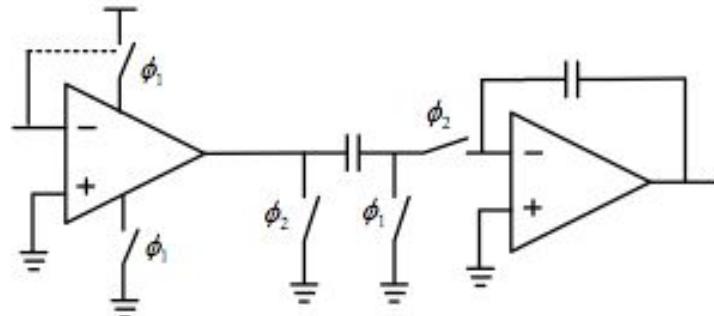
Li et al, VLSI-2004 & JSSC-2005



- High speed operation
- Free of reliability issues



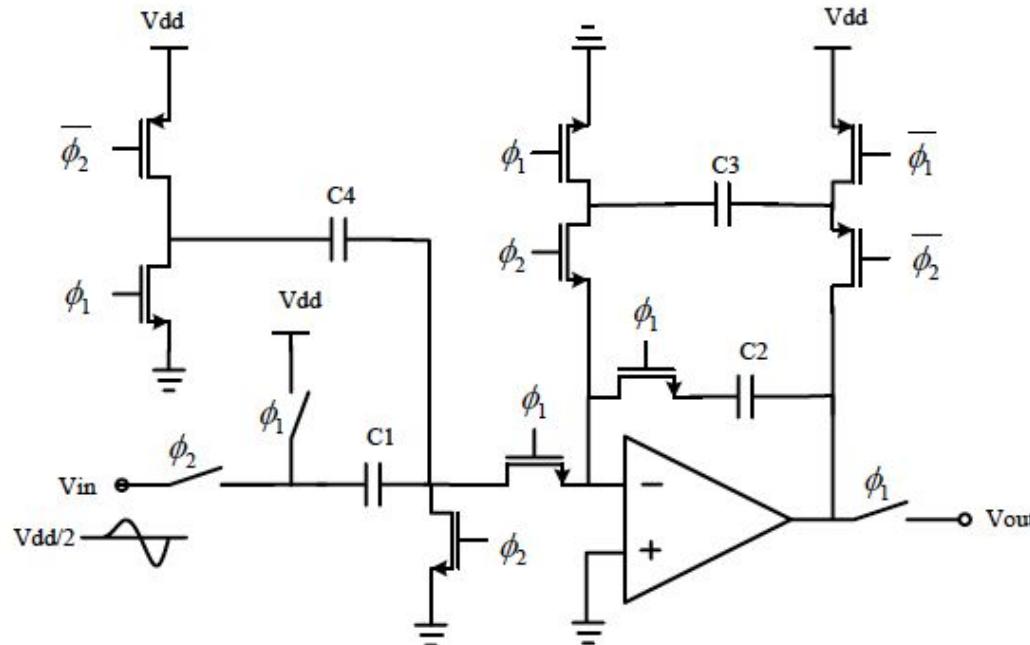
Conventional integrator



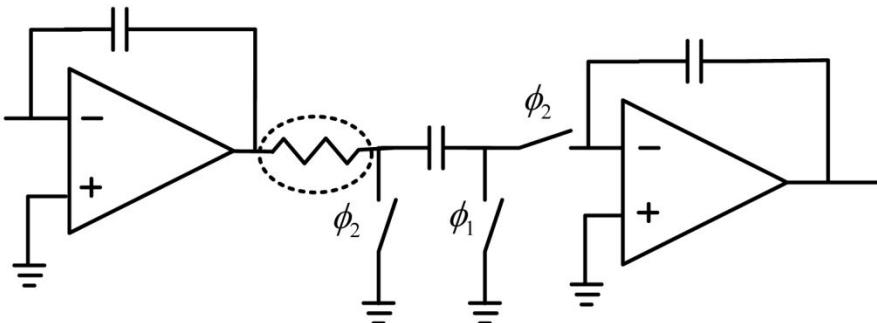
Switched-opamp integrator

Floating Reference Avoids Fwd Bias

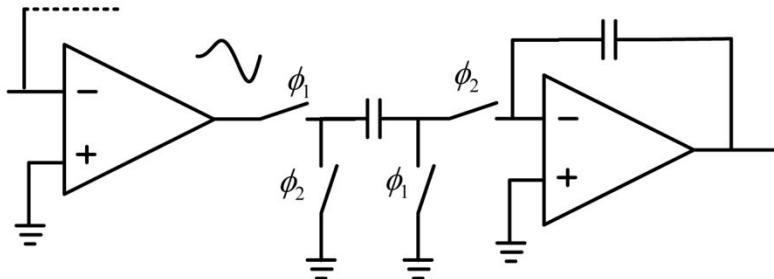
- C3 is precharged during ϕ_1
- C3 (floating reference) in feedback during ϕ_2
- DC offset circuit ($C4 = C1/2$) compensates for Vdd reset of C1
 - effective virtual ground = $Vdd/2$



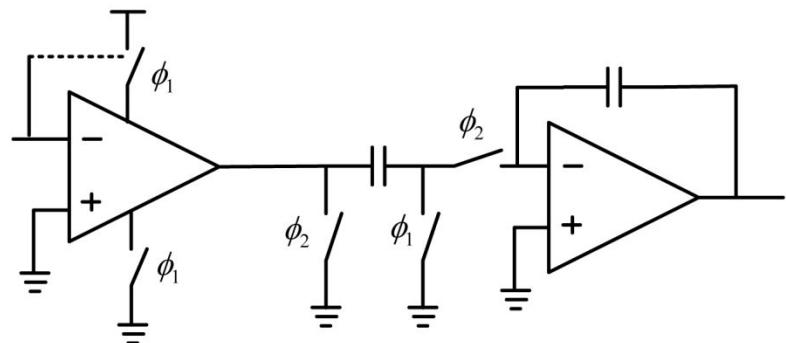
Switched-RC = Resistor Isolation



- No floating switch
- Highly linear sampling
- Free of reliability issues



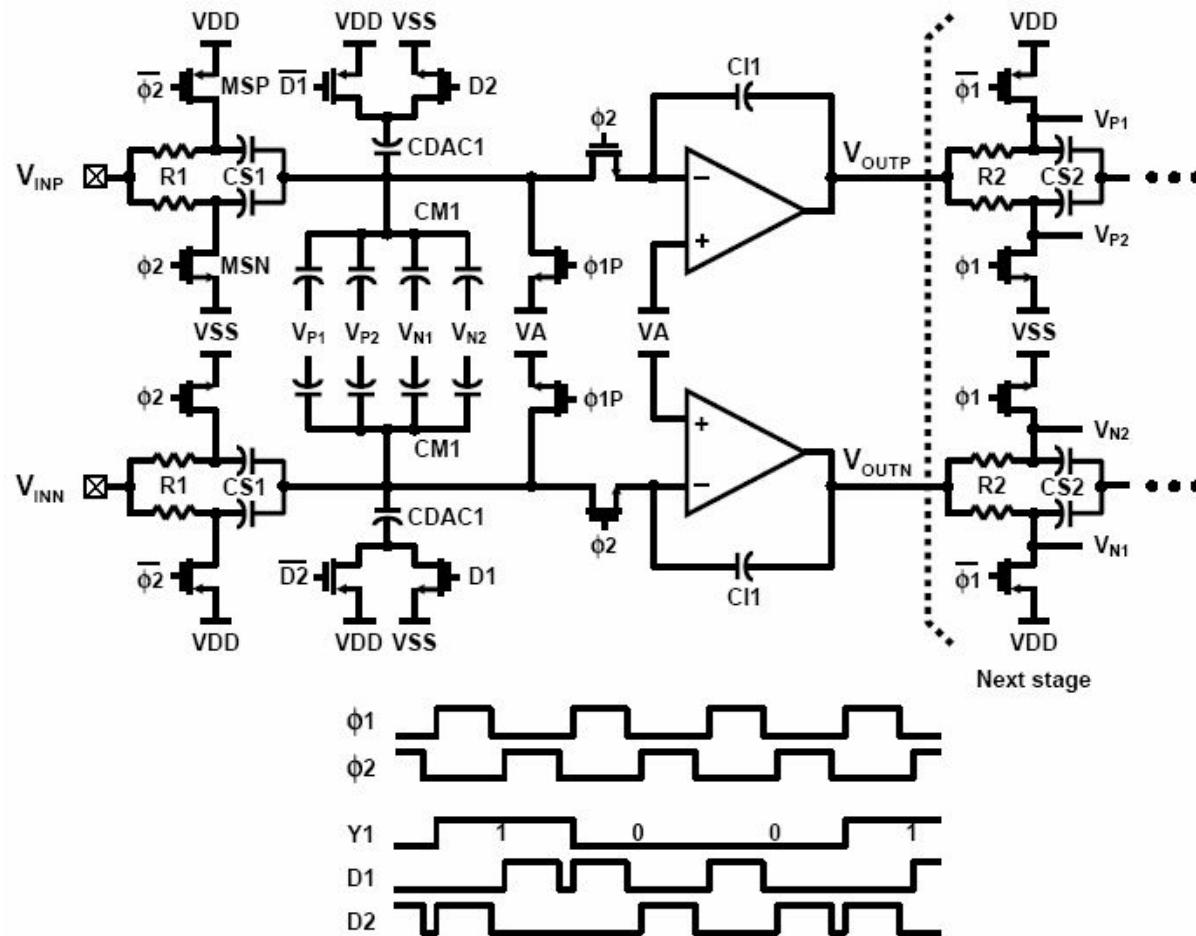
Conventional integrator



Switched-opamp integrator

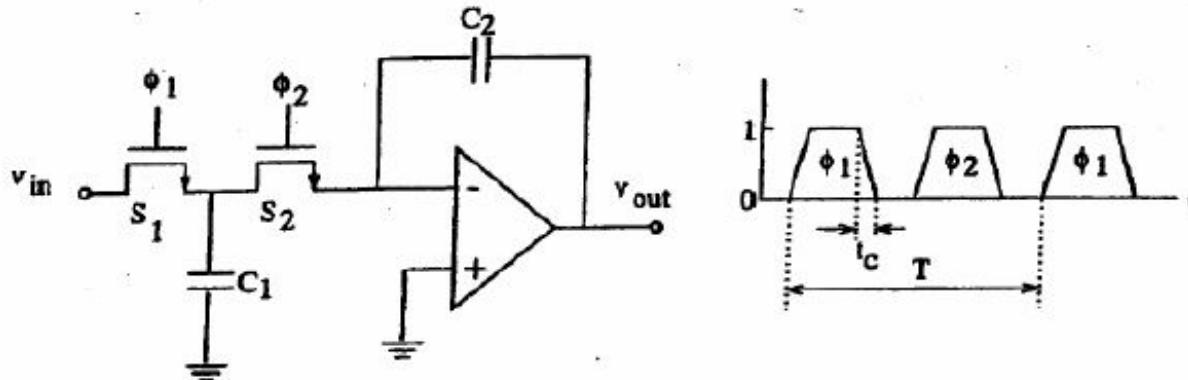
Switched-RC = Resistor Isolation

Ahn et al., ISSCC-2005 Paper 9.1

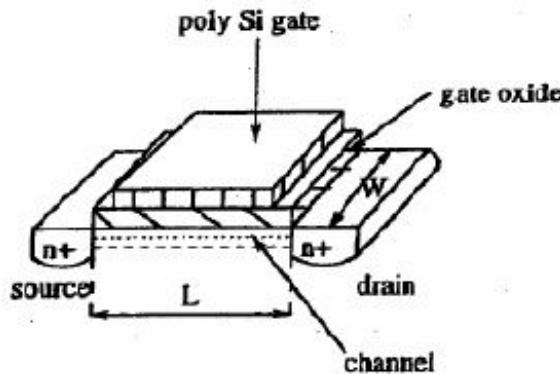


Charge Injection (1)

- Simple SC integrator



S₁ structure



Charge Injection (1) (Cont'd)

- The lateral field is v/L , the drift velocity is $\mu v/L$. Therefore, the current is

$$i = q_{ch} \cdot \mu \cdot v / L^2$$

- The on-resistance is

$$R_{on} = v / i = L^2 / (q_{ch} \cdot \mu)$$

- and hence

$$R_{on} \cdot q_{ch} = L^2 / \mu$$

holds.

Charge Injection (2)

From device physics,

$$q_{ch} = -W \cdot L \cdot C_{ox} \cdot (V_{dd} - v_{in} - V_{tn})$$

Unless S1 is in a well, connected to its source, V_{tn} depends on V_{in} , so q_{ch} is a mildly nonlinear function of V_{in} .

When S1 cuts off, part of $q_{ch}(q_s)$ enters C_1 and introduces noise, nonlinearity, gain and offset error.

To reduce q_s , choose L small, but R_{on} large. However, for 0.1% settling

$$R_{on} \cdot C_1 < T / 14 = 1 / (14 f_c)$$

Hence

$$q_{ch,\min} = L^2 / (R_{on,\max} \cdot \mu) = 14 \cdot L^2 \cdot f_c \cdot C_1 / \mu$$

and

$$v_{err,\min} = d \cdot q_{ch,\min} / C_1 = 14 \cdot d \cdot L^2 \cdot f_c / \mu$$

where $d = q_s / q_{ch}$

Clock Feedthrough

Capacitive coupling of clock signal via overlap Cov between gate and source. The resulting charge error is

$$q_{ov} = -V_{dd} \cdot C_{ov} \cdot C_1 / (C_1 + C_{ov})$$

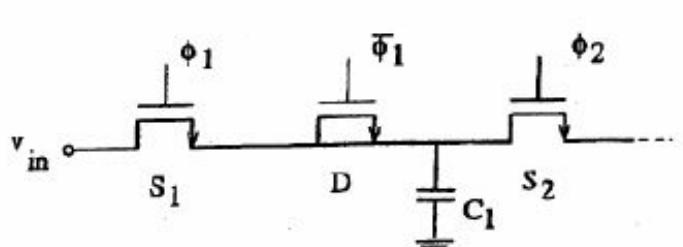
It adds to q_s . Usually, $|q_{ov}| \ll |q_s|$

Linear error.

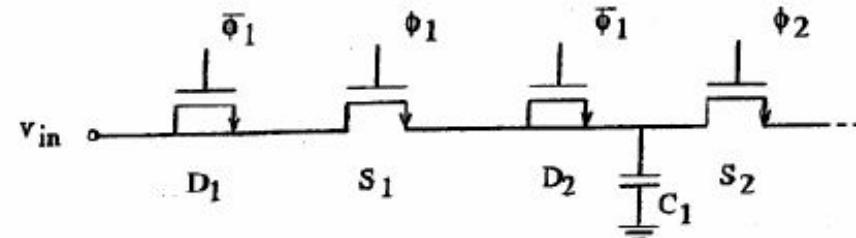
Same for S_1 and S_2 .

Methods for Reducing Charge Injection

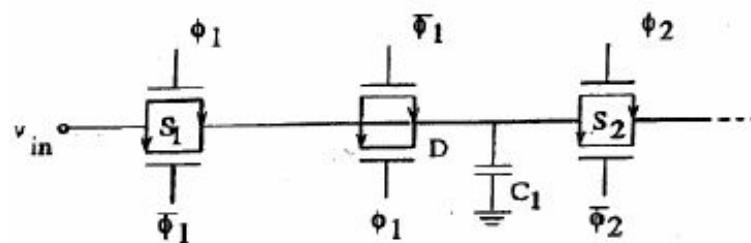
- Transmission gates: cancellation if areas are matched. Poor for floating switches, somewhat better for fixed-voltage operation.
- Dummy devices: better for $d \sim 0.5$.



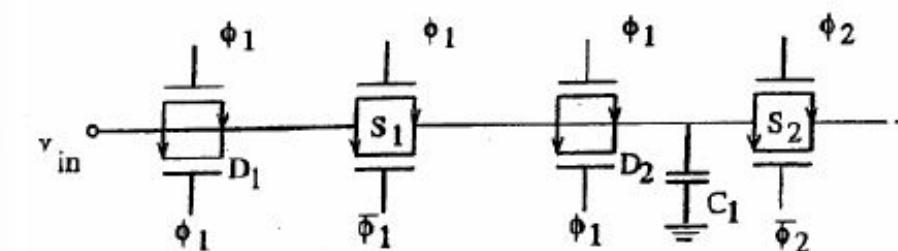
(a)



(b)



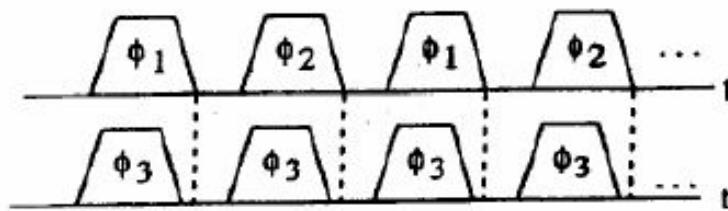
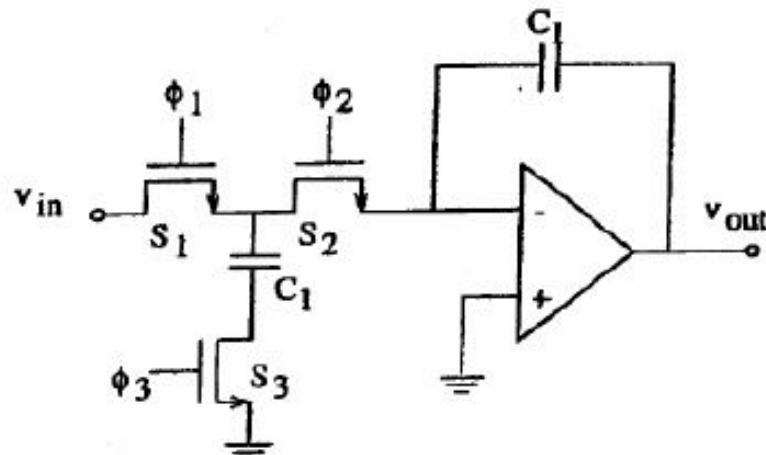
(c)



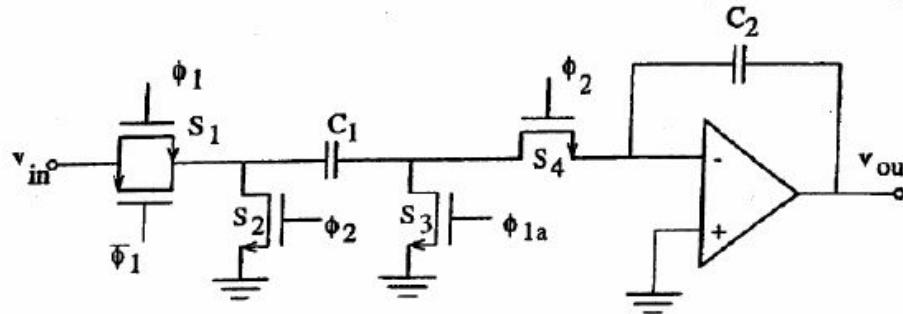
(d)

Advanced-Cutoff Switches

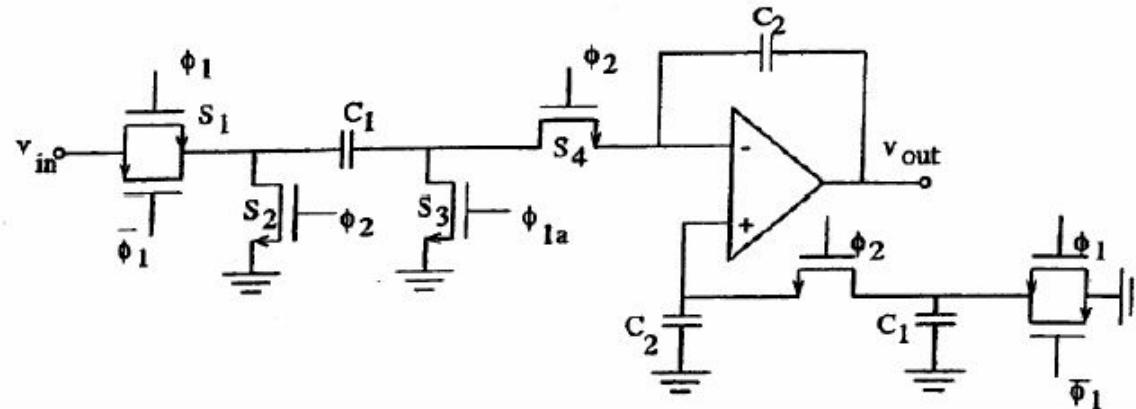
- Signal-dependent charge injection leads to nonlinear distortions; signal-independent one to fixed offset. Advanced-cutoff switches can reduce signal dependence.



Advanced-Cutoff Switches (Cont'd)

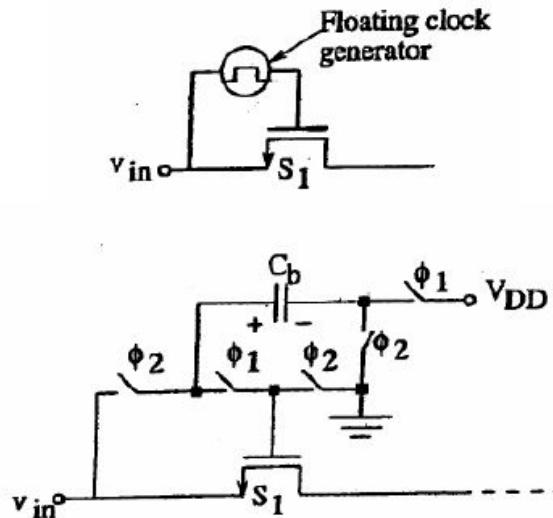


- Remaining charge injection is mostly common-mode in a differential stage.
- Suppressed by CMRR. In a single-ended circuit, it can be approximated by dummy branch:



Floating Clock Generator

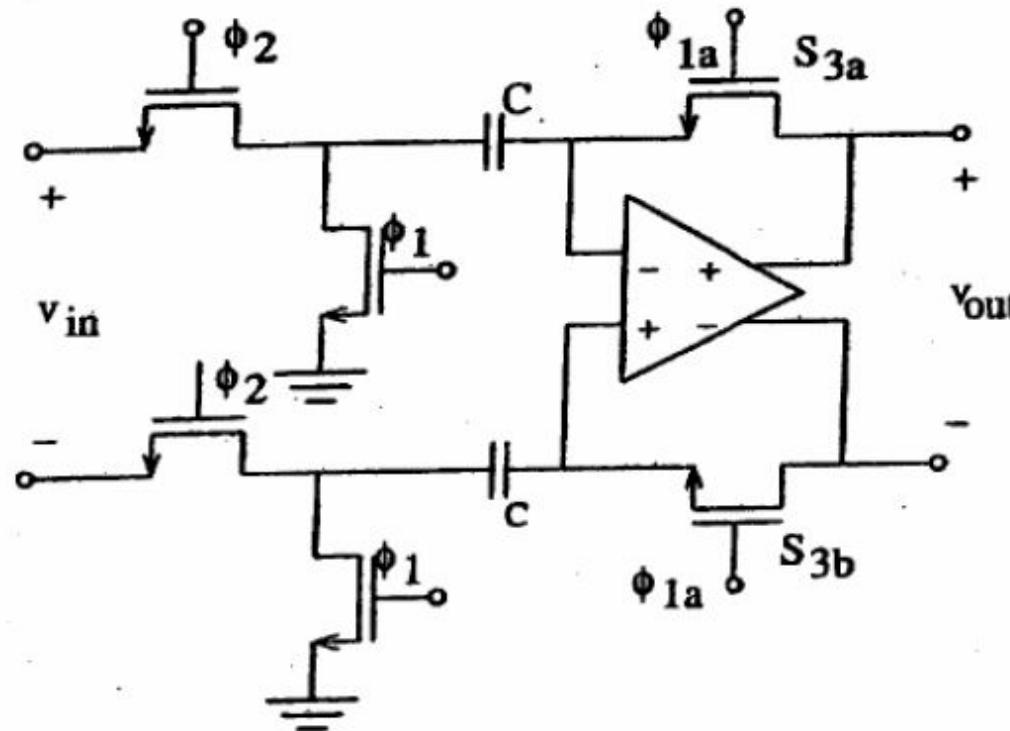
- To reduce signal dependence, reference the clock signal to v_{in} :



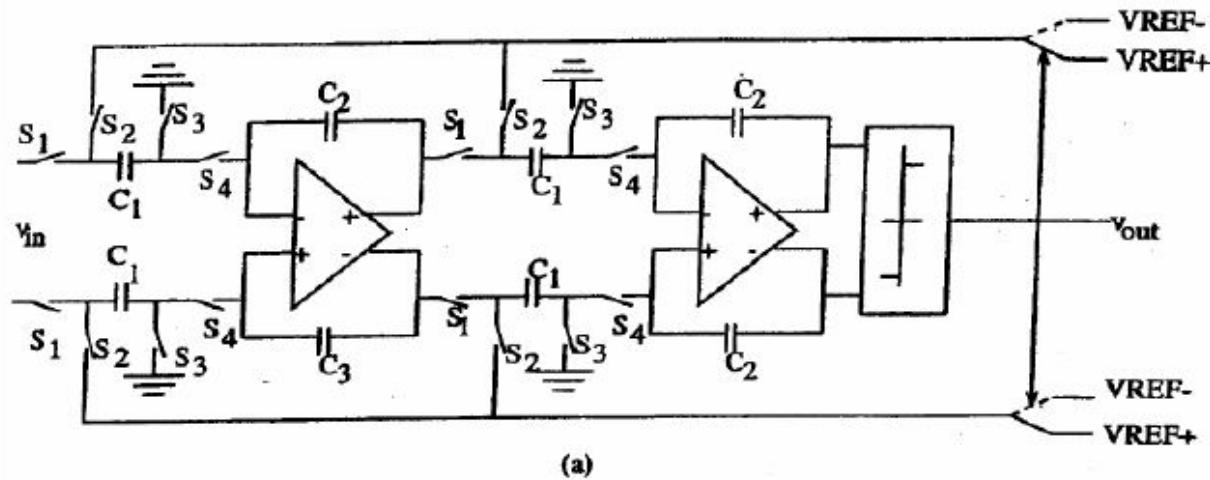
- This makes R_{on} also signal independent, so the settling is more linear. Clock feedthrough remains signal dependent, but it is a linear effect anyway. Better phasing : precharge C_b to VDD during phase 2, connect to v_{in} during phase 2.

Charge Injection in a Comparator

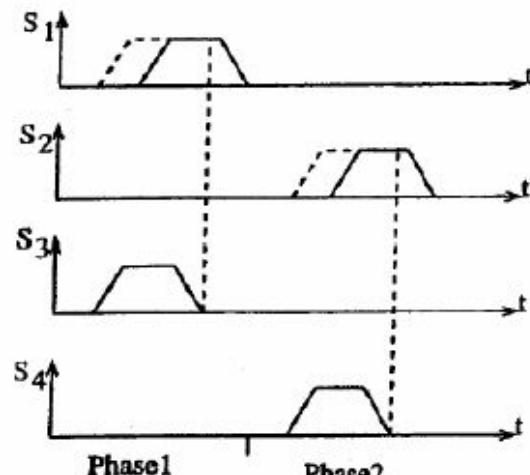
- Remains valid if input phases are interchanged.



Delta-Sigma ADC

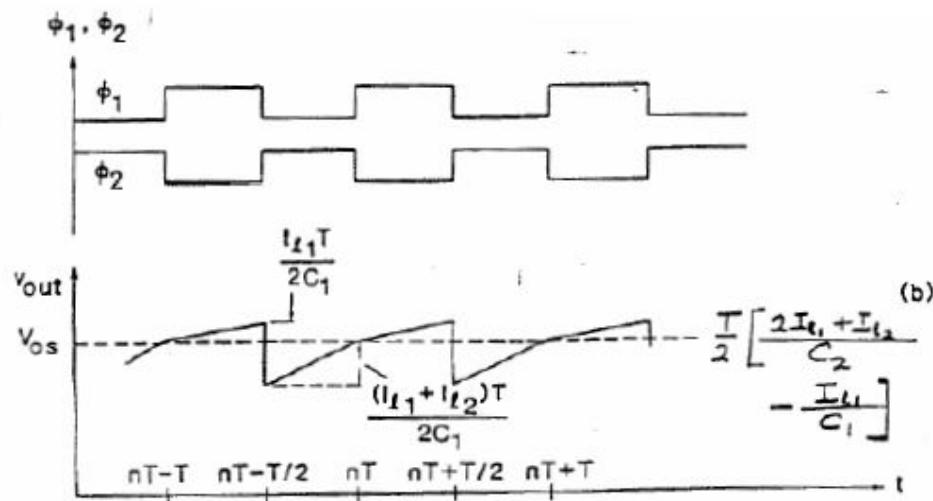
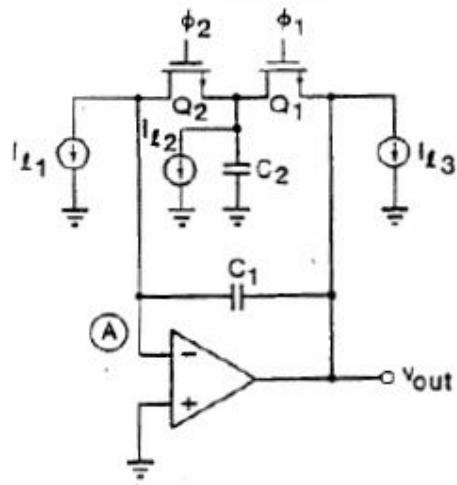


(a)



(b)

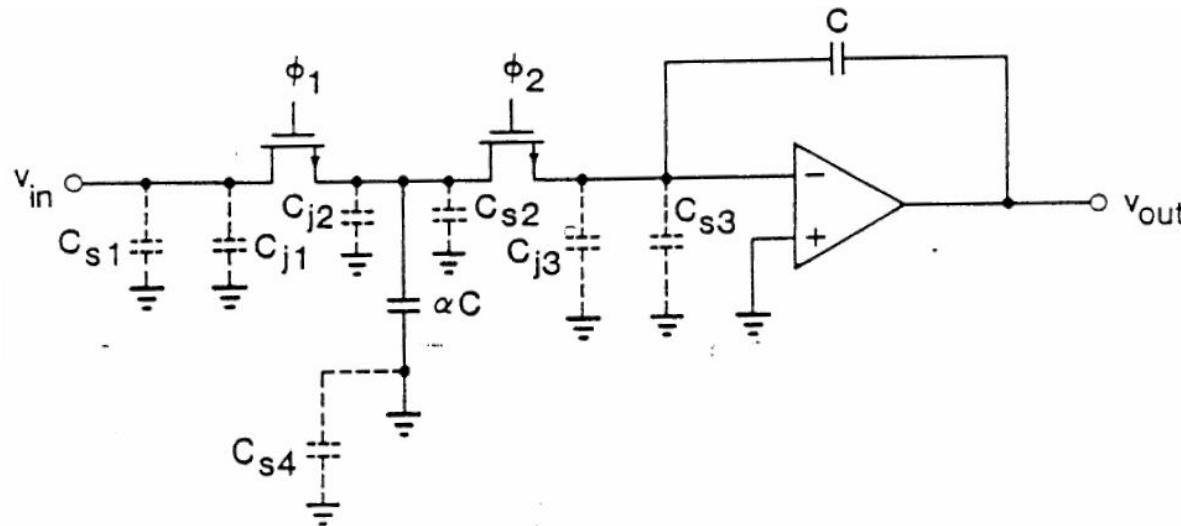
Junction Leakage



- $| \sim 10 \text{ pA/mil}^2$, $0.4 \text{ pA}/5\mu \times 5\mu$ but doubles for each 10°C .
- $f_{min} \sim 100\text{Hz}$ at 20°C , but 25KHz at 100° C .
- Fully differential circuit and Martin compensation converts it to common-mode effect.

Capacitances Inaccuracies

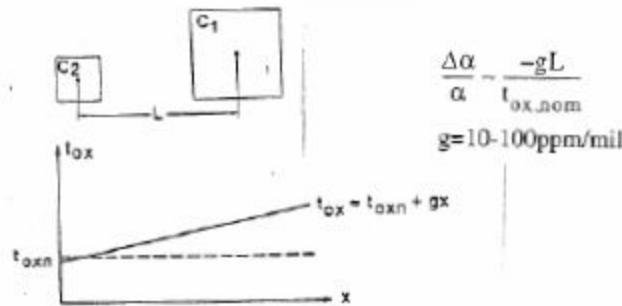
- Depends only on C ratios. Strays are often p-n junctions, leading to harmonic distortion also. For stray-sensitive integrator, all strays should be < 0.1% of αC .



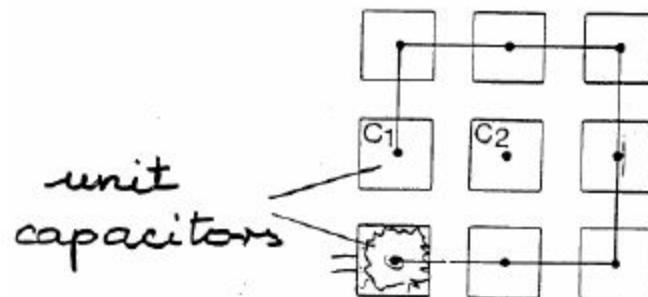
- ΔC can be systematic or random. Random effects (granularity, edge effects, etc.) cannot be compensated, but systematic ones can, by unit-capacitor/common-centroid construction of αC and C .

Capacitance Inaccuracies (Cont'd)

- Oxide gradient



- Common-centroid geometry



Compensated C₁/C₂ against linear variations of Cox, and edge related systematic errors (undercut, fringing)

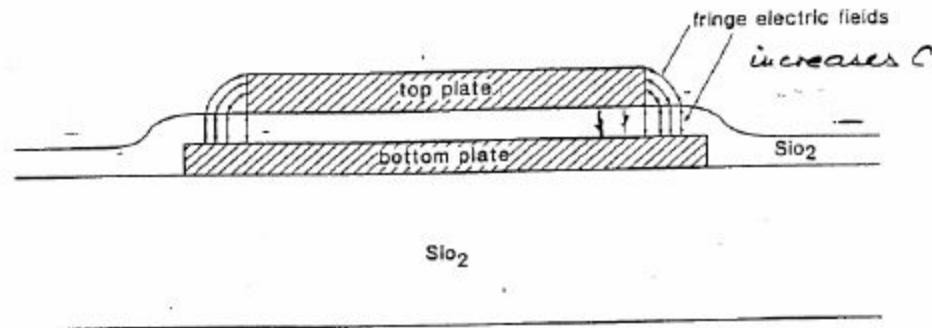
Capacitances Inaccuracies (Cont'd)

- Voltage and temperature coefficients

$$\gamma_v^c = \frac{1}{C} \frac{\partial C}{\partial v} \quad \text{usually} \quad |\gamma_v^c| \sim 10 \text{ ppm/V}$$

$$\gamma_T^c = \frac{1}{C} \frac{\partial C}{\partial T} \quad \text{usually} \quad |\gamma_T^c| \sim 20 \text{ ppm/V}$$

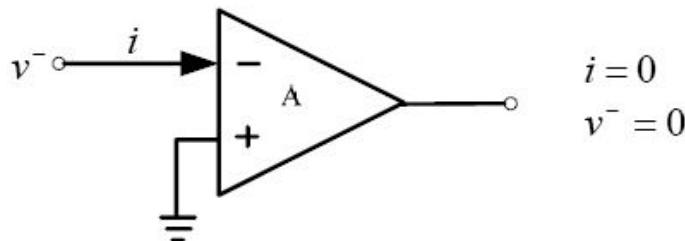
Smaller for ratios, especially for common-centroid layout:



Fringing, undercut: systematic edge effects. Reduced by commoncentroid geometry, since perimeter/area ratio is the same for C_1 and C_2 , $\Delta C \propto \text{perimeter}$, $C \propto \text{area}$

OPAMP Input Offset

- In most analog IC, the active element is the opamp. It is used to create a virtual ground (or virtual short circuit) at its input terminals:



- This makes lossless charge transfer possible. In fact, in a CMOS IC, $i \approx 0$ but $v \neq 0$ due to offset, 1/f and thermal noise and finite opamp gain A . Typically, $|v| = 5-10\text{mV}$. This affects both the dc levels and the signal processing properties. The effect of v is even more significant in a low-voltage technology where the signal swing is reduced, and A may be low since cascoding may not be available.

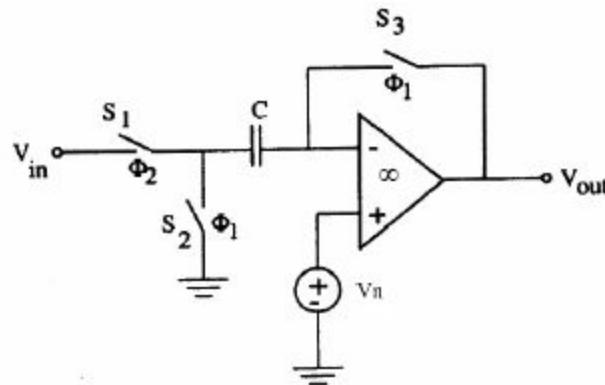
Improving the Virtual Ground

- Autozeroing or Correlated Double Sampling Schemes:
Scheme A: Stores and subtracts v at the input or output of the opamp;
Scheme B: Refers all charge redistributions to a (constant) v instead of ground;
Scheme C: Predicts and subtracts v , or references charge manipulations to a predicted.
- Compensation using extra input: An added feedback loop generates an extra input to force the output to a reset value for zero input signal.
- Chopper stabilization: The signal is modulated to a “safe” (low-noise) frequency range, and demodulated after processing.
- Mixed-mode schemes: Establish a known analog input, use digital output for correction.

Circuits Using Autozeroing

- Comparators
- Amplifiers
- S/H, T/H, delay stages
- Data converters
- Integrators
- Filters
- Equalizers

Simple Autozeroed Comparator



Nonidealities represented by added noise voltage:

$$v_n = v^- = V_{os} + v_{1/f} + v_{thermal} - \mu v_{out}; \quad \mu = 1/A_{opamp}$$

Input-referred noise at the end of interval:

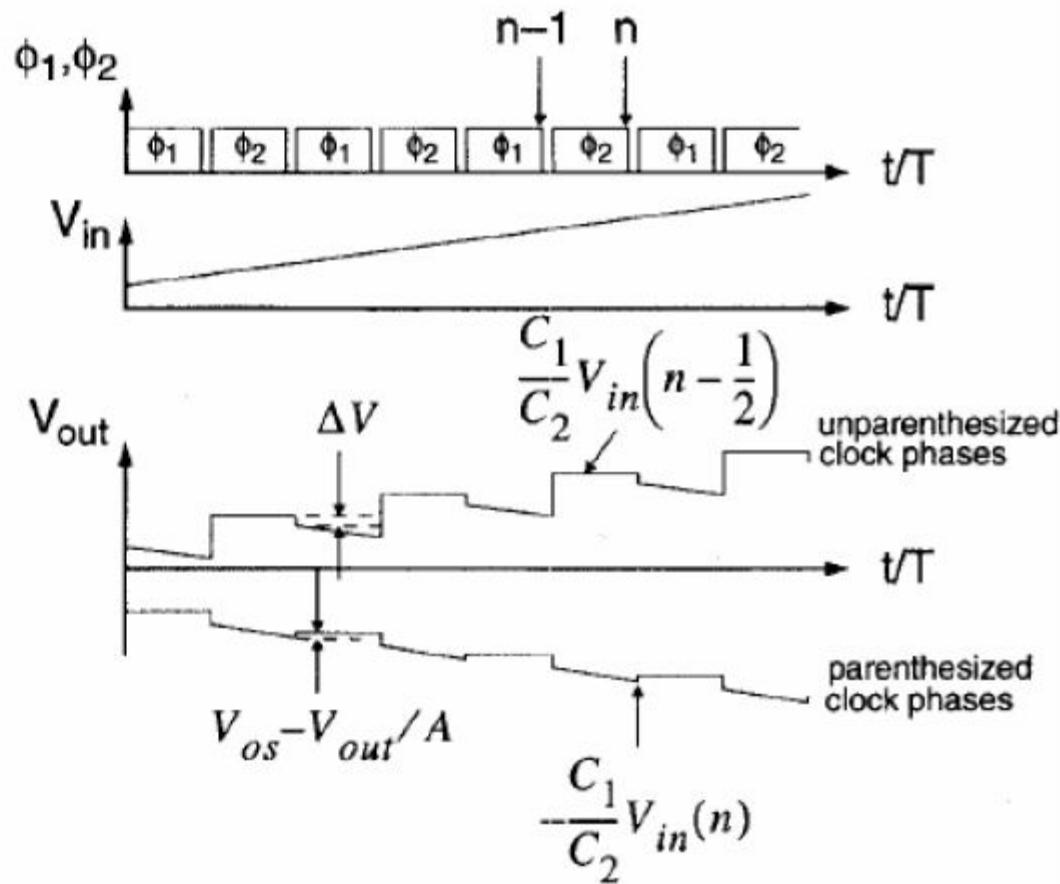
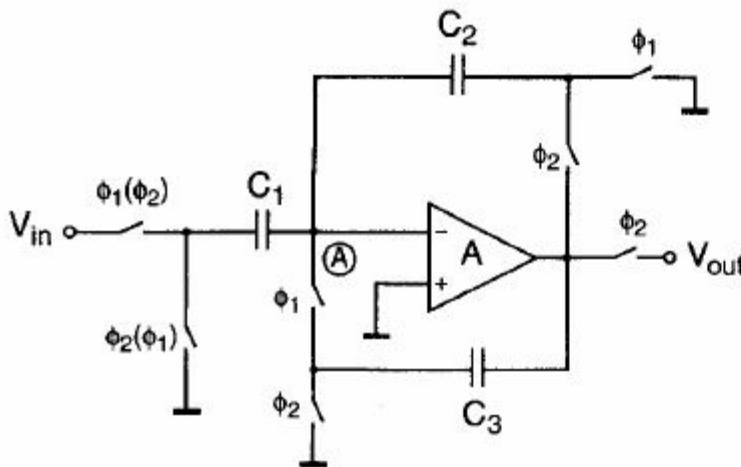
$$v_{n,in}(n) = v_n(n) - v_n(n-1/2);$$

Transfer function without folding: $|H_N|^2 = 4 \sin^2(\omega T / 4)$

V_{os} , $V1/f$ and (for oversampled signals) μV_{out} may be reduced by H_N . Here, μV_{out} is not considered, since it is not important for a comparator.

An Offset- and Finite-Gain-Compensated SC Amplifier

Haug et al., 1984 ISCAS



Analysis of Compensated Gain Amplifier

Input-output relation for inverting operation:

$$v_{out}(n) = -C_1 / C_2 v_{in}(n) + (1 + C_1 / C_2)[v^-(n) - v^-(n-1/2)]$$

The S/H capacitor switches from 0 to

$$v^-(n) = V_{os} - \mu v_{out}(n-1/2) \quad \text{as } \phi_1 \rightarrow 1. \text{ Hence,}$$

$$v_{out}(n-1/2) - v_{out}(n-1) = V_{os} - \mu v_{out}(n-1/2), \text{ where } \mu = 1/A.$$

At low signal frequencies where $v_{out}(n) \approx v_{out}(n-1)$,

the error term is only $(1 + C_1 / C_2)\mu^2 v_{out}$. The dc gain is

$$H(1) = \frac{-C_1 / C_2}{(1 + C_1 / C_2)\mu^2}$$

The output step at reset is only $A_v \approx V_{os} - \mu v_{out} - (C_1 / C_3)\Delta v_{in}$,
where the last term enters for noninverting operation only. A_v is usually
1~10 mV. The slewing required is minimal. The output offset is $\mu(1 + C_1 / C_2)V_{os}$.

Error in H(1): denom. should have + 1. Clock feedthrough generates some residual offset. Can be used as a compensated delay stage.

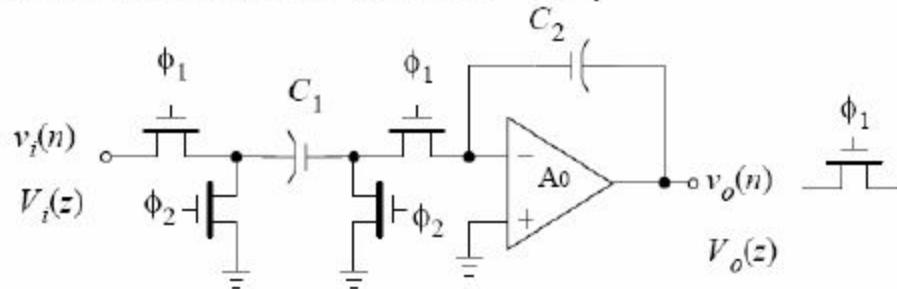
Finite Opamp DC Gain Effect

For $A_0 \rightarrow \infty$, $H_i(e^{j\omega t}) = \frac{-(C_1/C_2)e^{(j\omega T)/2}}{2 \sin((\omega T)/2)}$

For $A_0 < \infty$, $H(e^{j\omega t}) = (1 + m(\omega))e^{j\theta(\omega)}H_i(e^{j\omega T})$.

Here, the relative gain error $m \equiv -(1/A_0)(1 + C_1/(2C_2))$
the relative phase error $\theta \equiv (C_1/C_2)/(A_0\omega T)$.

(Martin, PhD thesis, U of Toronto, 1980)



Equations valid only for high frequencies.

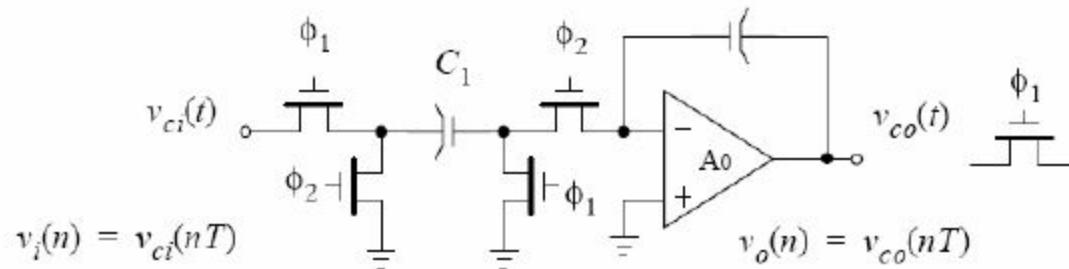
At unity-gain freq. ω_i : $2 \sin(\omega_i T/2) = C_1/C_2$, $m(\omega_i) \sim \theta(\omega_i) \sim -1/A_0$

Usually, the magnitude error is smaller than the (C_1/C_2) error and is negligible. The phase error shifts poles/zeros horizontally, like dissipation: important!

Finite Opamp DC Gain Effect (Cont'd)

Non-inverting integrator: similar derivation, same $m(\omega), \theta(\omega)$. In a biquad, $s_p \rightarrow s_p(1 - 1/A_0)$ due to $m(\omega)$. The phase errors result in

$$\frac{1}{Q_p} \rightarrow \frac{1}{Q_p} + \theta_1(\omega_0) + \theta_2(\omega_0) \sim \frac{1}{Q_p} + \frac{2}{A_0}$$



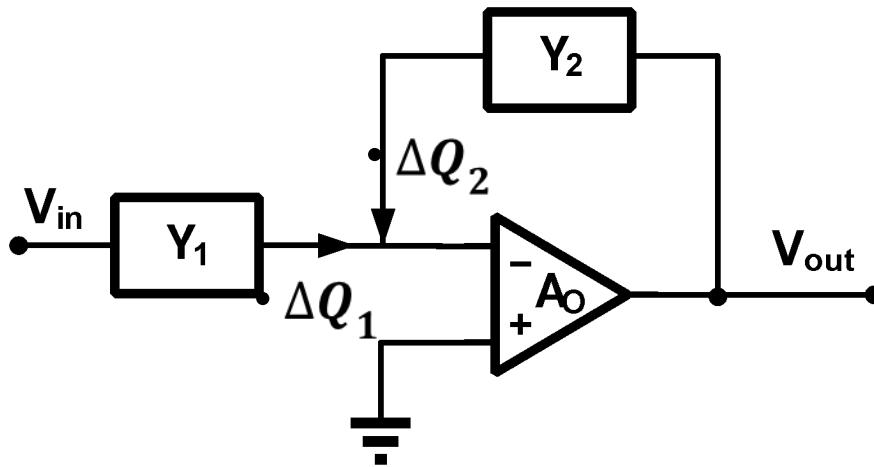
Change in peak gain: $-20\lg(1+2Q_p/A_0)$ (in dB)

can be large for $Q_p \gg 1$!

For $Q_p = 15, A_0 = 1000, \Delta G \sim -0.26dB$

High $Q_p \rightarrow$ use high A_0 opamp! Gain-squaring integrators!

Model for Finite Opamp Gain Effect



- $\Delta Q_i = Y_i(V_i^+ - V_i^-)$

is the charge flow in one clock period

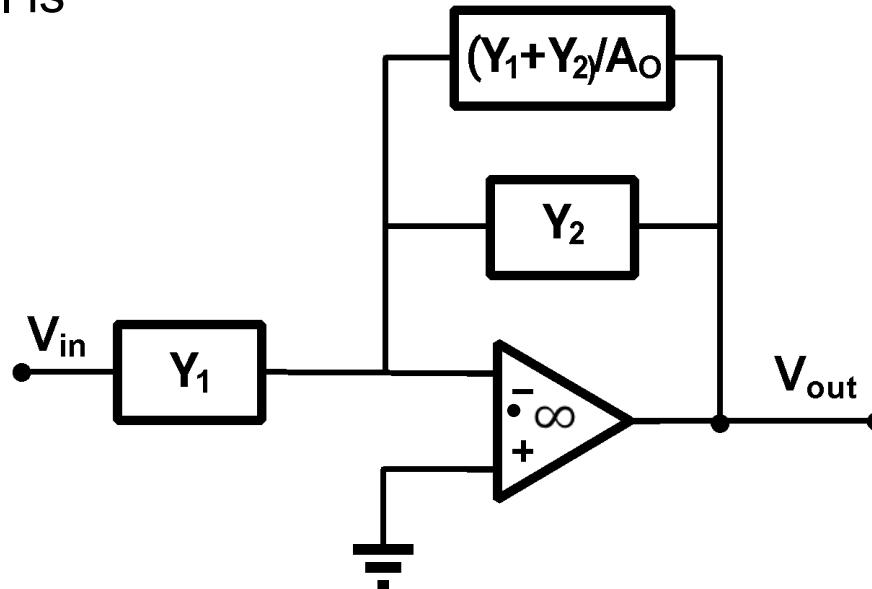
- For $A_o \rightarrow \infty$, $\Delta Q_1 = Y_1 V_{in} = -\Delta Q_2 = -Y_2 V_o$
- so $H(z) = V_o/V_{in} = -Y_1/Y_2$

Model for Finite Opamp Gain Effect

For finite A_o ,

- $\Delta Q_1 = Y_1(V_{in} + V_o/A_o) = -Q_2 = -Y_2(V_o + V_o/A_o)$
- $H(z) = -Y_1/(Y_2 + Y_1/A_o + Y_2/A_o)$

so the model is



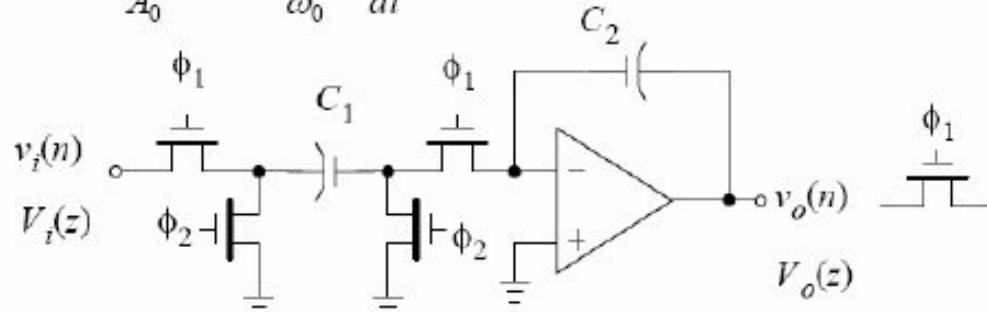
Finite Opamp Bandwidth Effect

One-pole opamp model:

$$A_v(s) = \frac{-\omega_0}{s - s_1} \approx \frac{-1}{s/\omega_0 + 1/A_0} = \frac{V_o(s)}{V(s)}$$

Or, in time domain,

$$\frac{1}{A_0} v_o(t) + \frac{1}{\omega_0} \frac{dv_o(t)}{dt} = -v(t)$$



Combine with KVL, charge conservation. Finding and sampling $v_o(t)$, calculating $V_o(z)/V_i(z)$, and setting $z = e^{j\omega T}$, for an inverting integrator results in

$$m(\omega) = -e^{-k_1} (1 - k \cos \omega T)$$

$$\theta(\omega) = -e^{-k_1} k \sin \omega T$$

Where $k = C_2 / (C_1 + C_2)$ is the feedback factor. $k_1 = k\omega_0 T / 2 = k\pi f_0 / f_c$ should be $\gg 1$.

Time constant: $\tau = 1/(k\omega_0)$ should be $\ll T/2$.

Finite Opamp Bandwidth Effect (Cont'd)

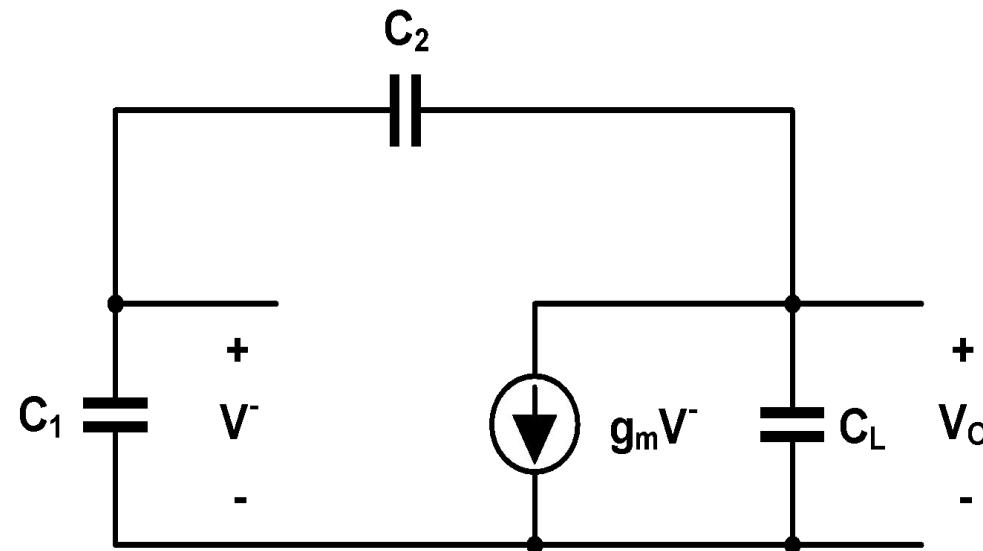
Since $k_1 = k\pi\omega_0 / \omega_c$, for $k \sim 1$, if $\omega_0 \geq 5\omega_c$ then $k_1 \geq 15$ and

$e^{-k_1} < 3 \cdot 10^{-7}$, so both m and θ are negligible. Hence, for $C_1 \ll C_2$, use
 $\omega_0 \geq 5\omega_c$.

For $k < 1$, even higher ω_0 may be needed. Due to the exponential behavior, the error increases rapidly if ω_0 is too small!

The derivation assumes $v_{in}(t)$ is constant. If several stages settle simultaneously, or if there is a continuous-time loop of opamp and coupling C's, then computer analysis (SWITCAP, Fang/Tsividis) is needed.

Time Constant of OTA-SC Integrator



- Open-loop Gain

$$\bullet\bullet g_m V^- + sC_L V_o + sC_S V_o = 0$$

$$\bullet\bullet C_S \triangleq \frac{C_1 C_2}{C_1 + C_2}$$

$$\bullet\bullet V_o = \frac{-g_m V^-}{s(C_L + C_S)}$$

$$\bullet\bullet V_1 = \beta V_o \quad \bullet\bullet \beta \triangleq \frac{C_2}{C_1 + C_2}$$

$$\bullet\bullet V_1 = \frac{-\beta g_m V^-}{s(C_L + C_S)}$$

- At pole S_p , $V_1 = V$

$$\bullet\bullet S_p = \frac{-\beta g_m}{C_L + C_S} = \frac{-C_2 g_m}{C_L (C_1 + C_2) + C_1 C_2}$$

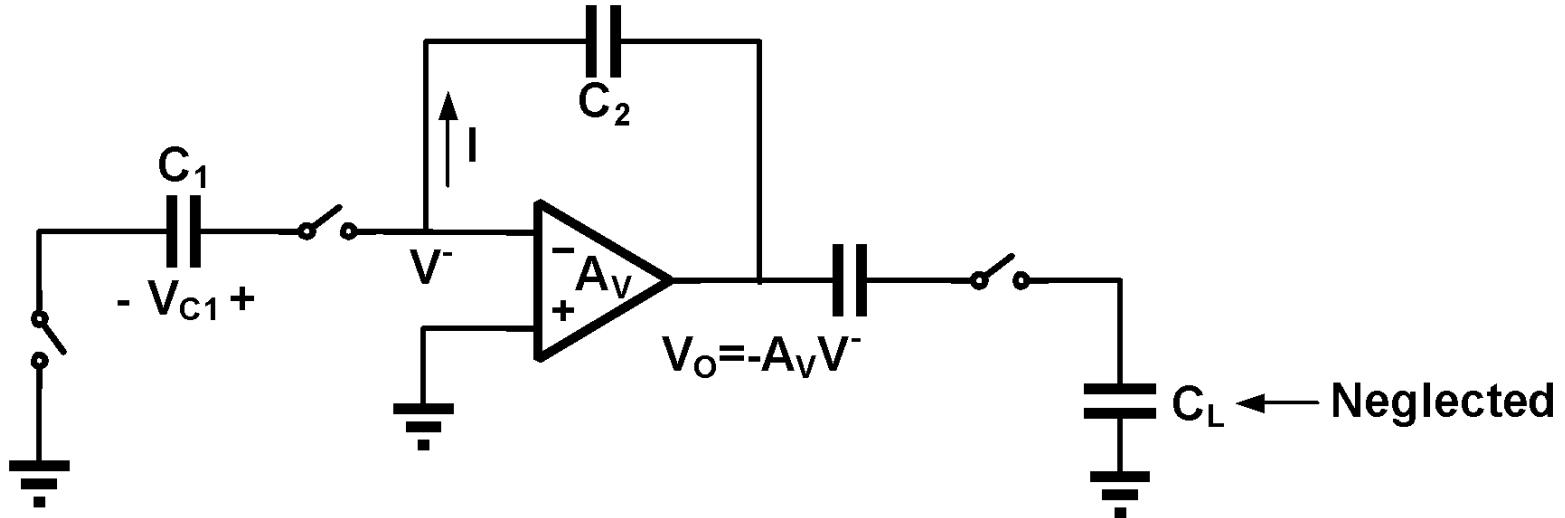
- Transient term:

$$\bullet\bullet e^{s_p t} = e^{-t/\tau} \quad \bullet\bullet \tau = \frac{1}{|s_p|} = \frac{C_L + C_S}{\beta g_m}$$

- Unity-gain conventional integrator, assuming all C is equal:

$$\bullet\bullet \tau = \frac{3C}{g_m}$$

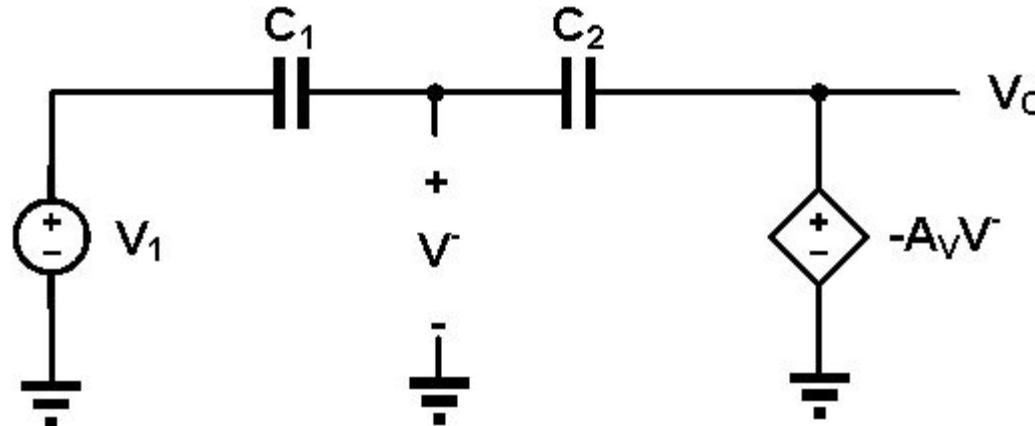
Integrator Using a Two-Stage (Buffered) Opamp



$$\bullet \cdot A_V = \frac{A_0}{s/\omega_p + 1} \quad \bullet \text{Let Initial Values be } V_{C1} = V_1, V_{C2} = 0$$

$$\bullet \cdot I = (V_1 - V_o) \frac{s C_1 C_2}{C_1 + C_2} = s C_2 (V^- - V_o)$$

Integrator Using a Two-Stage (Buffered) Opamp



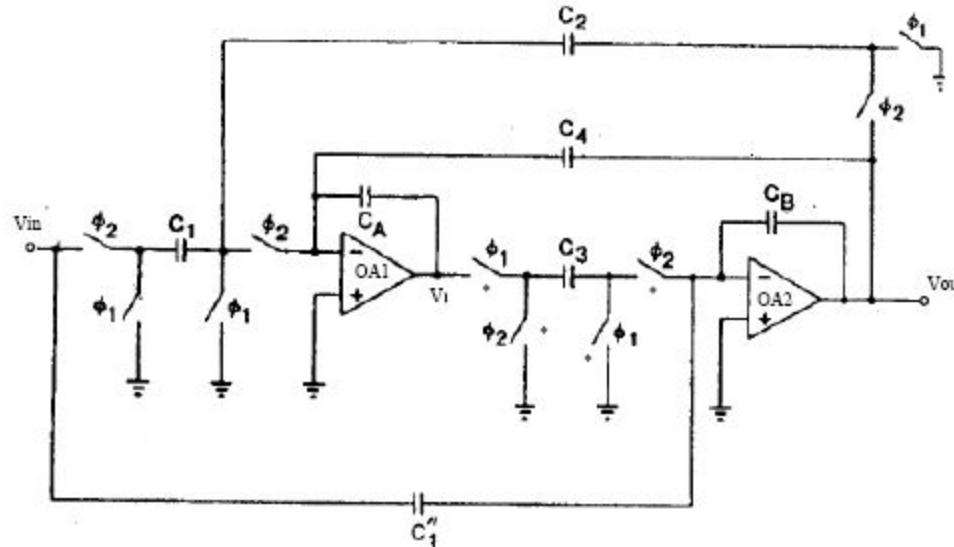
$$\bullet \bullet V_O = -A_V V^- \cong V_1 \frac{1-\beta}{s/(A_0 \omega_p) + \beta + 1/A_0} \quad \bullet \bullet \beta \triangleq \frac{C_2}{C_1 + C_2}$$

$$\bullet \bullet \text{Pole at:} \quad \bullet \bullet -(\beta + 1/A_0) A_0 \omega_p \cong -\beta \omega_u$$

$$\bullet \bullet \text{Time Constant:} \quad \bullet \bullet \tau \cong 1/\beta \omega_u$$

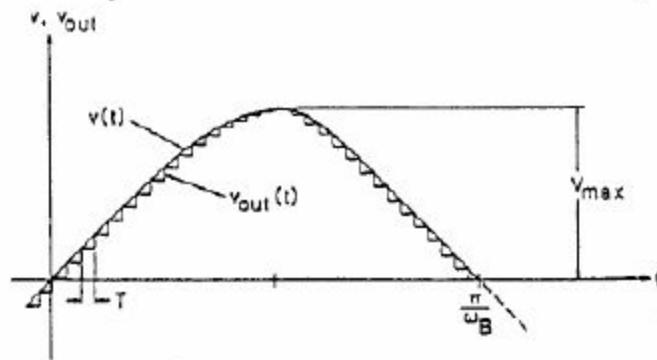
$$\bullet \bullet \text{Settling level:} \quad \bullet \bullet |V_O(S)|_{s=0} = \frac{1-\beta}{\beta + 1/A_0} \cong -\frac{C_1}{C_2}$$

High-Q Biquad

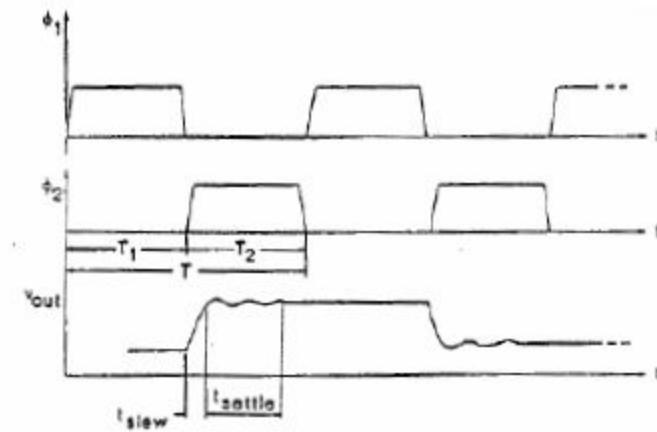


- For original phases, both opamps settle when $\phi_2 \rightarrow 1$. Changing the switches of C3, they settle separately. V₁ changes twice in one cycles, but OA1 still has the same T/2 time (T for the change at $\phi_1 \rightarrow 1$) to settle and to charge C3. The transient when $\phi_2 \rightarrow 1$ has a full period to settle in OA1 and OA2 .

Slew Rate Estimation (1)



Nonlinear slewing followed by linear settling:



$$t_{slew} = xT_2 \sim xT/2$$

$S_r = |(dv_{out})/(dt)|_{\max}$. For $v(t) = V_{\max} \sin \omega_B t$ where ω_B is the maximum sine wave freq. at input, the slope $|dv/dt|$ of the envelope $v(t)$ is $\leq \omega_B V_{\max}$. Then $S_r \sim 2\omega_B V_{\max}/x$, very pessimistic estimate!

Slew Rate Estimation (2)

- Much simpler estimate can be based on assuming that C_{in} is fully discharged in the slewing phase. Then the slew current can be found from
- $I_s \sim C_{in} \cdot V_{in,max} / [x \cdot T/2]$
- Less pessimistic than the previous estimate.

Noise Considerations

- Clock feedthrough from switches
 - External noise coupled in from substrate, power lines, etc
 - Thermal and 1/f noise generated in switches and opamps
- (1) Has components at $f=0$, f_c , can be reduced by dummy switches, differential circuit, etc. May be signal dependent!
- (2) Discussed elsewhere.
- (3) Thermal noise in MOSFETs: PSD is

$$S_T = \frac{\overline{v_{nT}^2}}{\Delta f} = 4\theta R \quad , \quad \theta = kT$$

For $f \geq 0$, only (one-sided distribution).

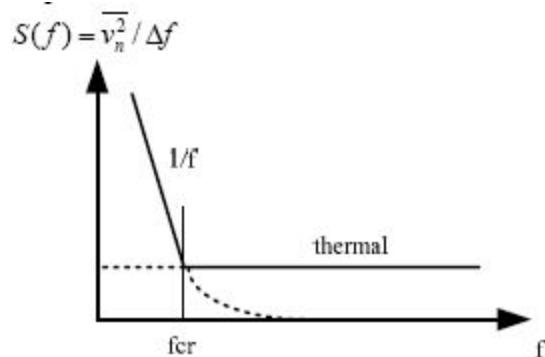
Flicker noise:

$$S_f = \frac{\overline{v_{nT}^2}}{\Delta f} = \frac{k}{C_{ox}WLf}$$

Total noise PSD: $S = S_T + S_f$.

Noise Considerations (Cont'd)

- Noise spectra



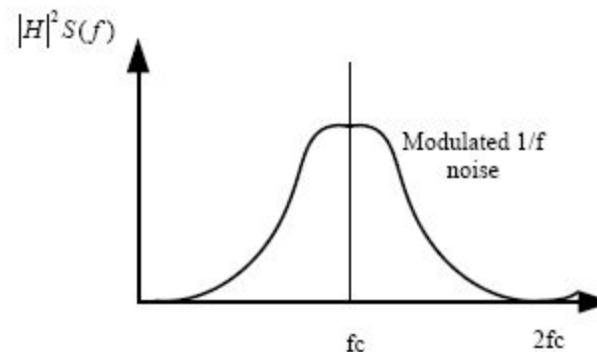
- Offset compensation (CDS—correlated double sampling); subtracts noise, T/2 second delayed.

$$H_{CDS} = 1 - e^{-j\omega T/2}$$

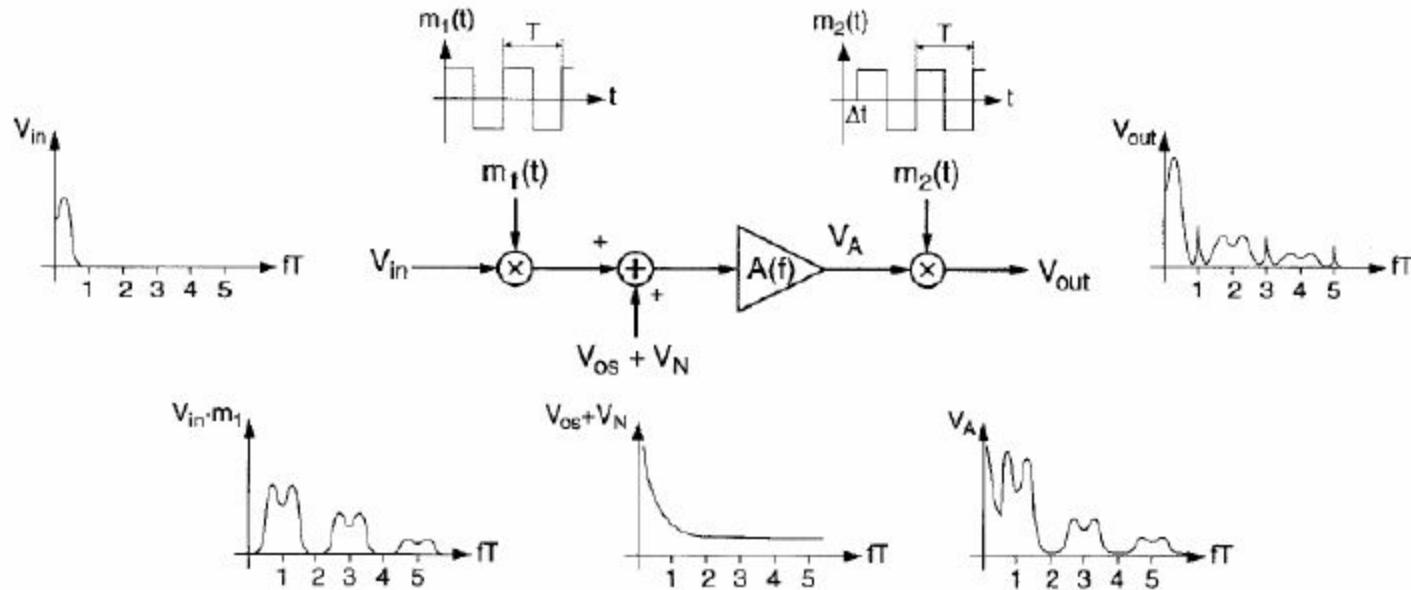
$$|H|^2 = 4 \sin^2(\omega T/4)$$

CDS:

1. Pick up noise, no signal;
2. Pick up noise, plus signal;
3. Subtract the two.

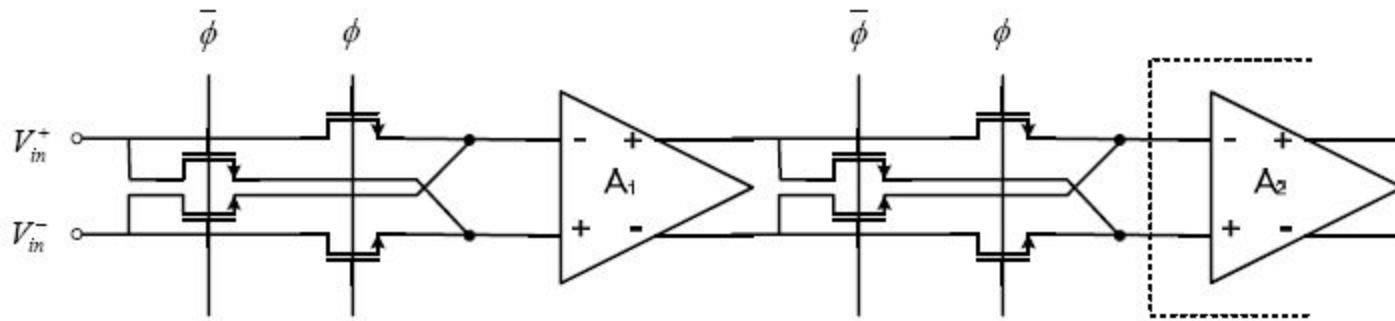


Chopper Stabilization



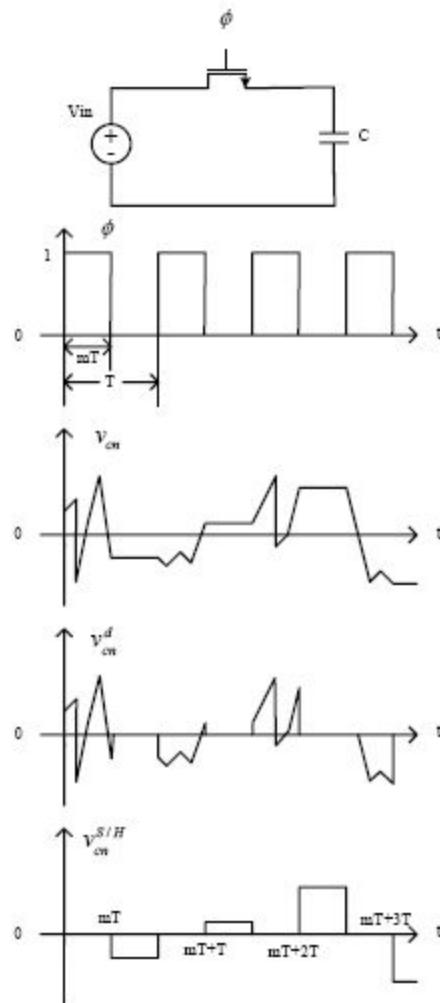
Fully differential circuits needed.

Chopper Stabilization (Cont'd)



Differential SC amplifier using chopping.

Noise Aliasing



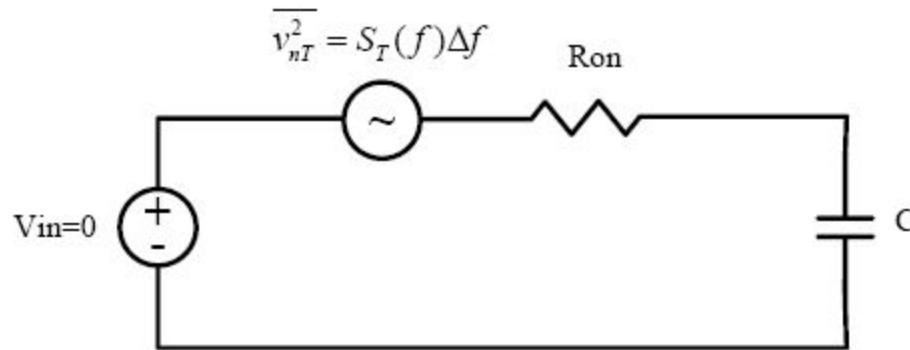
Mean-square values are the same (θ / C) within all windows.

Direct noise power: $\overline{(v_{cn}^d)^2} = \frac{m\theta}{C}$

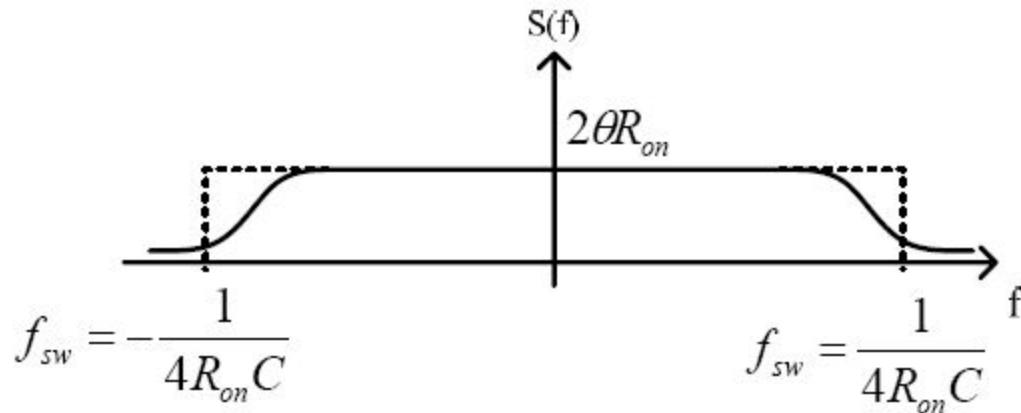
S/H PSD: $\frac{\overline{(v_{cn}^{S/H})^2}}{\Delta f} = \left(\frac{\tau \sin f \tau \pi}{T f \tau \pi} \right)^2 \cdot \sum_{k=-\infty}^{k=\infty} S(f - kf_c)$

$S(f)$: RC filtered direct noise
Most noise at dc!

Equivalent Circuit for Direct Noise



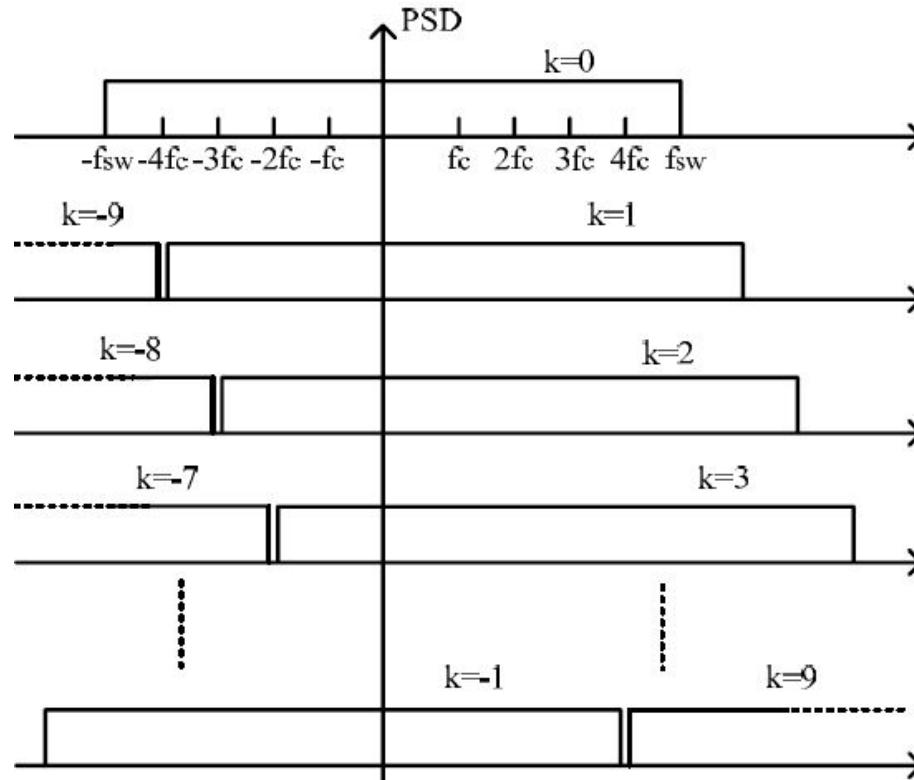
$S(f)$ for direct noise: low-pass filtered and windowed white noise.



For satisfactory settling (0.1%), $R_{on}C \leq mT/7 = m/(7f_c)$, $f_{sw} \geq 3.5f_c$.

Noise Aliasing

Aliasing for $f_{sw} = 5f_c$



S(f) is magnified by $2f_{sw}/f_c = 10$! The PSD is $\theta/(Cf_c)$ after aliasing (i.e. sampling but not holding).

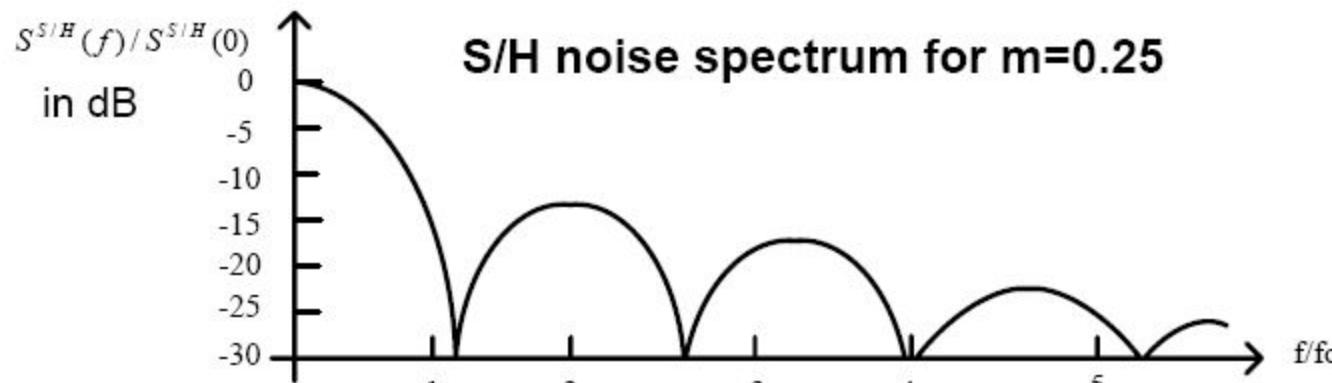
Noise power = kT/C .

Noise Spectra

For low frequencies ($f \ll f_c$)

$$S^{S/H}(f) \approx \frac{(1-m)^2 \theta}{f_c C} \text{ decreases with } m \uparrow$$

$$S^d(f) \approx 2m \theta R_{on} \text{ increases with } m \uparrow$$



Low frequency noise ratio

$$r = \frac{S^{S/H}}{S^d} \approx \frac{(1-m)^2}{2m} \frac{1}{f_c R_{on} C}$$

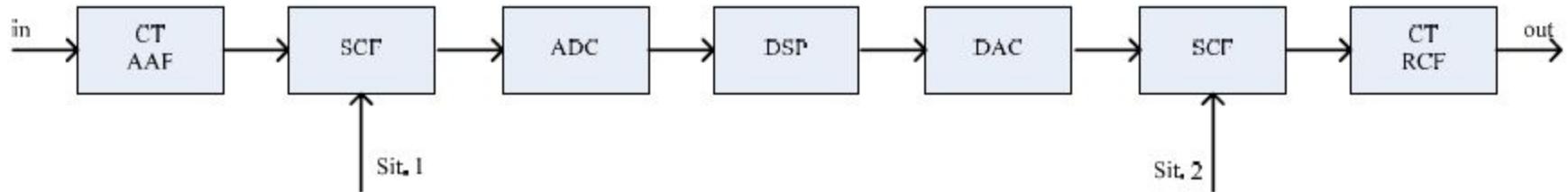
$$r \geq 3.5(1/m - 1)^2 > 3.5$$

For $m=0.25$, $r=31.5!$

Noise generated in stage independent of R_{on} , but the noise generated in preceding stages (direct noise) gets filtered, so the R_{on} should be as large as possible!

Switched-Capacitor Noise

Two situations; example:



Situation 1: only the sampled values of the output waveform matter; the output spectrum may be limited by the DSP, and hence $V_{RMS,n}$ reduced. Find V_{RMS} from \sqrt{KTC} charges; adjust for DSP effects.

Situation 2: the complete output waveform affects the SNR, including the S/H and direct noise components. Usually the S/H dominates. Reduced by the reconstruction filter.

Calculation of SC Noise (Summary)

- In the switch-capacitor branch, when the switch is on, the capacitor charge noise is lowpass-filtered by R_{on} and C . The resulting charge noise power in C is kTC . It is a colored noise, with a noisebandwidth $f_n=1/(4R_{on}C)$. The low-frequency PSD is $4kTR_{on}$.
- When the switch operates at a rate $f_c \ll f_n$, the samples of the charge noise still have the same power kTC , but spectrum is now white, with a $PSD=2kTC/f_c$. For the situation when only discrete samples of the signal and noise are used, this is all that we need to know.
- For continuous-time analysis, we need to find the powers and spectra of the direct and S/H components when the switch is active. The direct noise is obtained by windowing the filtered charge noise stored in C with a periodic window containing unit pulses of length m/f_c . This operation (to a good approximation)
 - simply scales the PSD, and hence the noise power, by m . The low-frequency PSD is thus $4mkTR_{on}$.

Calculation of SC Noise (Summary) (Cont'd)

To find the PSD of the S/H noise, let the noise charge in C be sampled and- held at f_c , and then windowed by a rectangular periodic window

$$w(t)=0 \text{ for } n/f_c < t < n/f_c + m/f_c$$

$$w(t)=1 \text{ for } n/f_c + m/f_c < t < (n+1)/f_c$$

$$n=0,1,2,\dots$$

Note that this windowing reduces the noise power by $(1-m)^2$, since the S/H noise is not random within each period.

Usually, at low frequencies the S/H noise dominates, since it has approximately the same average power as the direct noise, but its PSD spectrum is concentrated at low frequencies. As a first estimate, its PSD can be estimated at *for frequencies up to $f_c/2$* .

$$2(1-m)^2 kT / (f_c C)$$

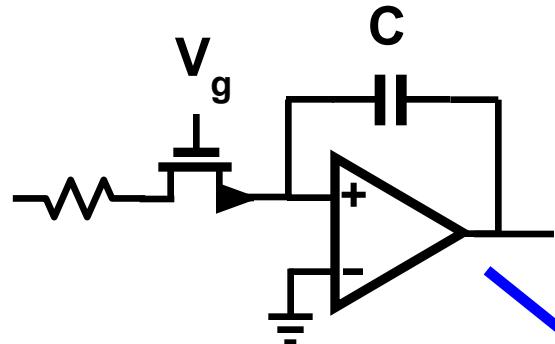
Switched R-MOSFET-C Filters

P. Kurahashi, P. Hanumolu, G. Temes and U.
Moon

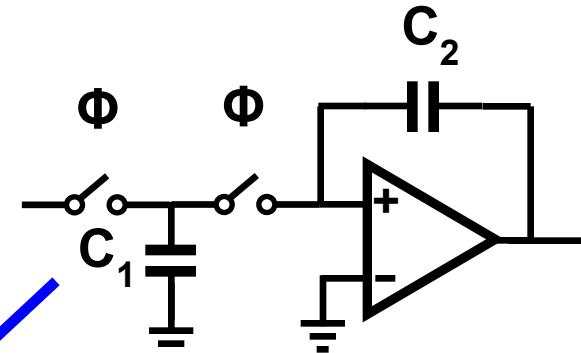
(JSSC, pp.1699-1709, Aug. 2007)

Switched R-MOSFET-C (SRMC) Filter

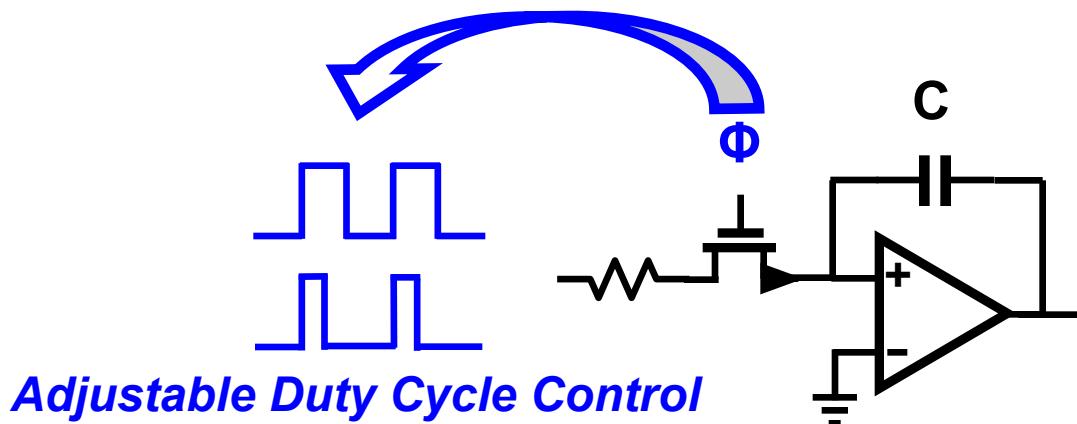
R-MOSFET-C



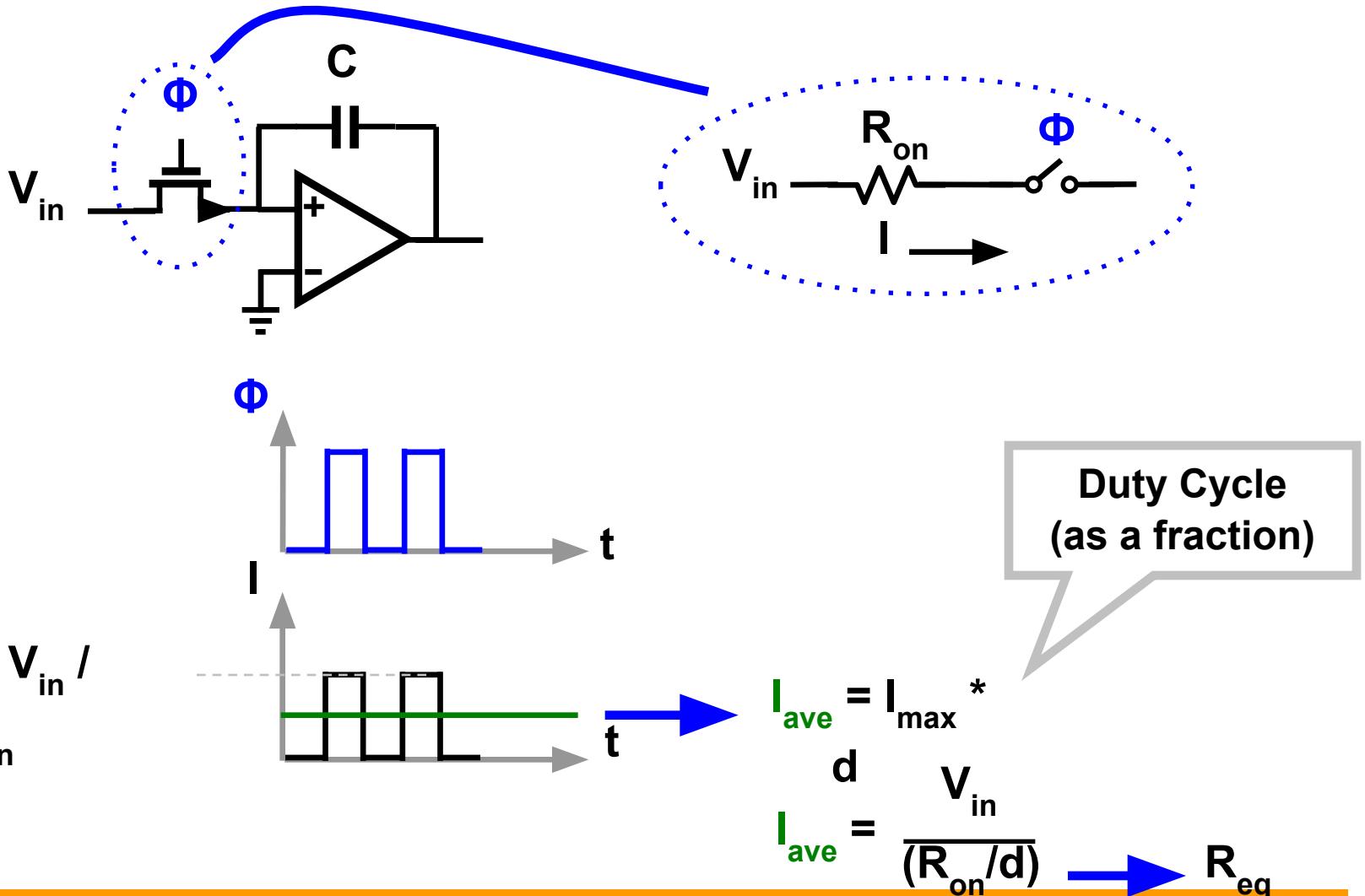
Switched Capacitor



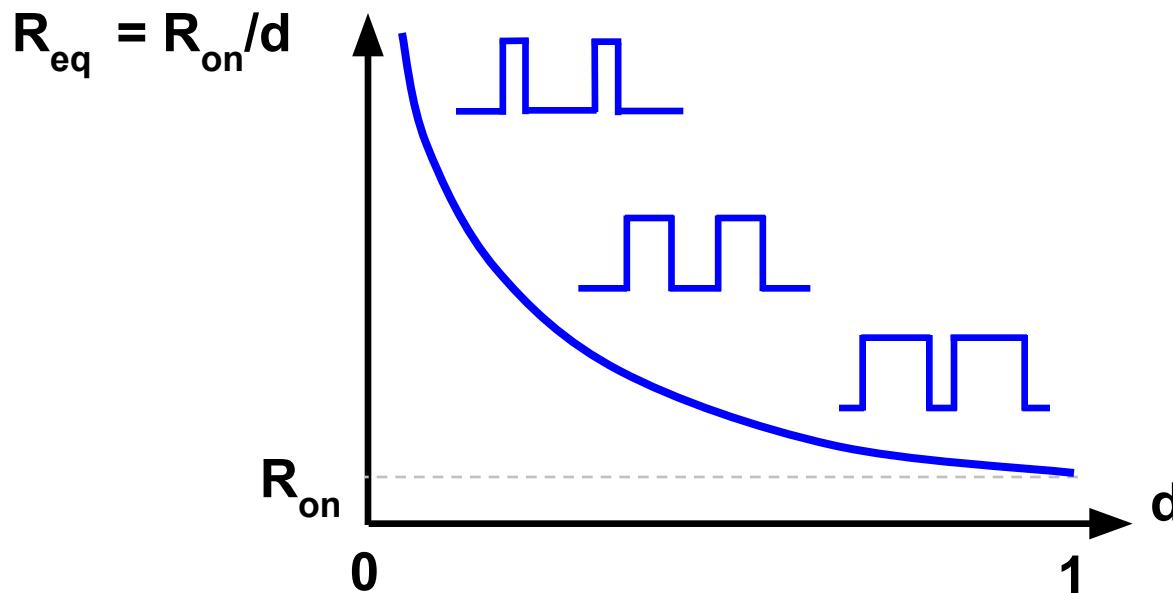
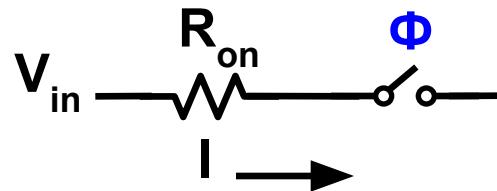
Switched R-MOSFET-C



Switched-MOSFET Equivalent Resistance

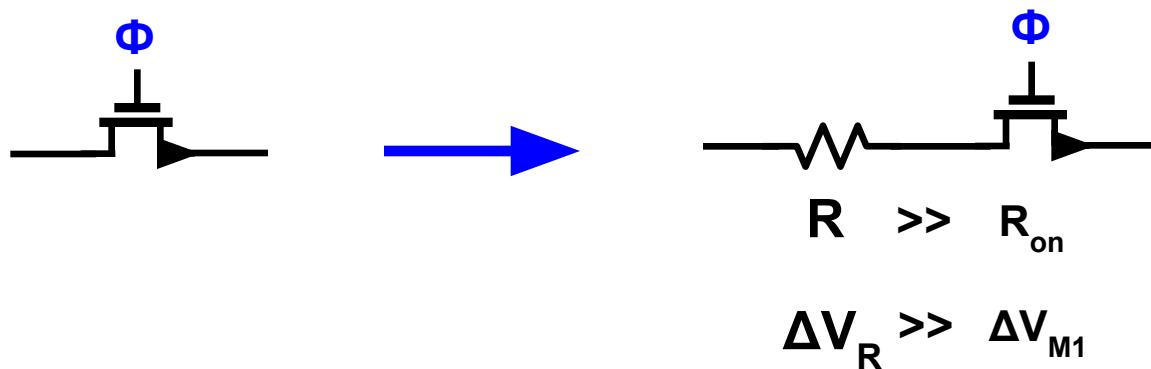


Switched-MOSFET Equivalent Resistance

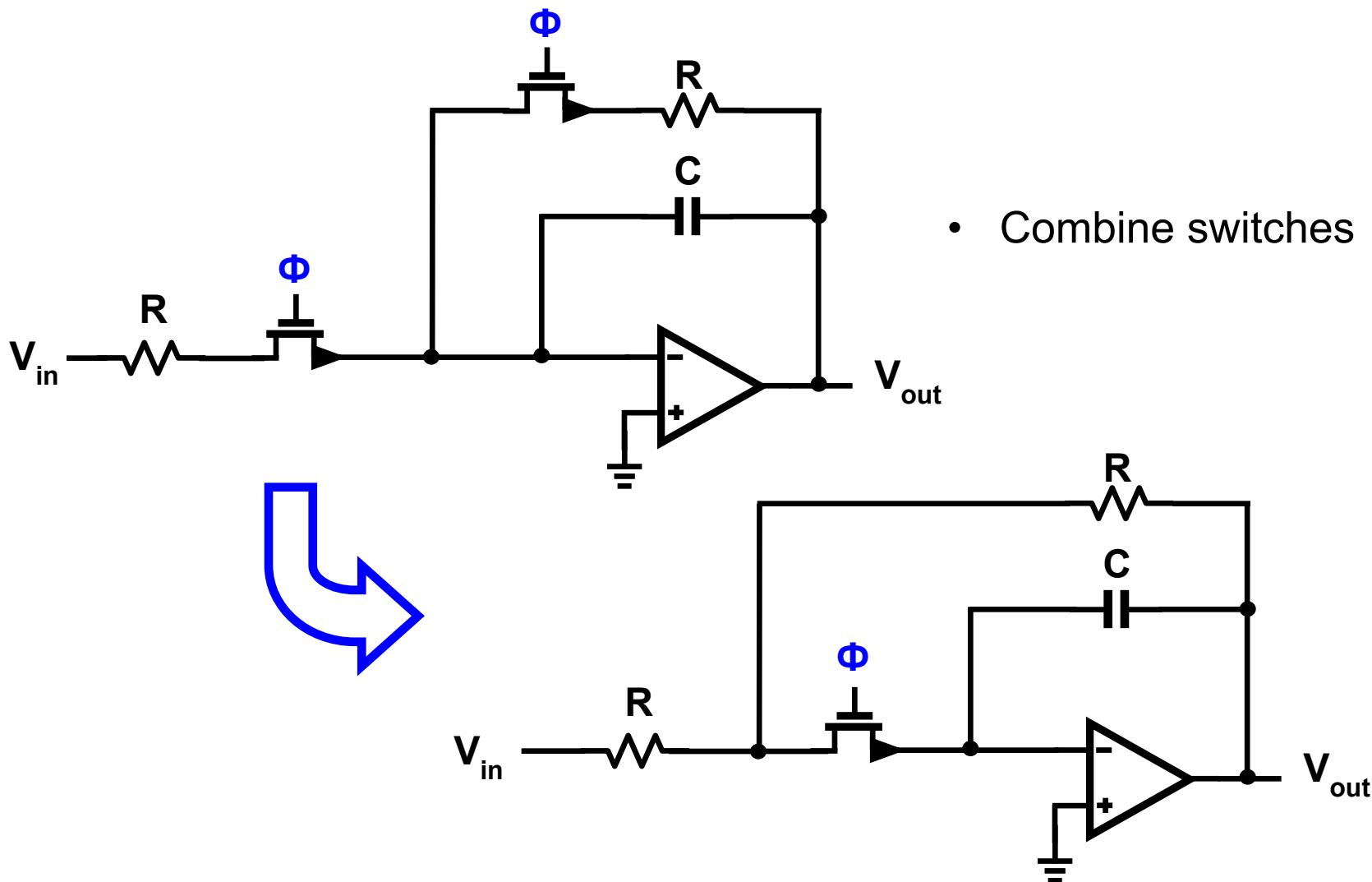


Switched R-MOSFET-C Filter

- MOSFET is a non-linear element
- Linearity can be improved by adding a resistance in series
- Voltage mostly dropped across linear resistor

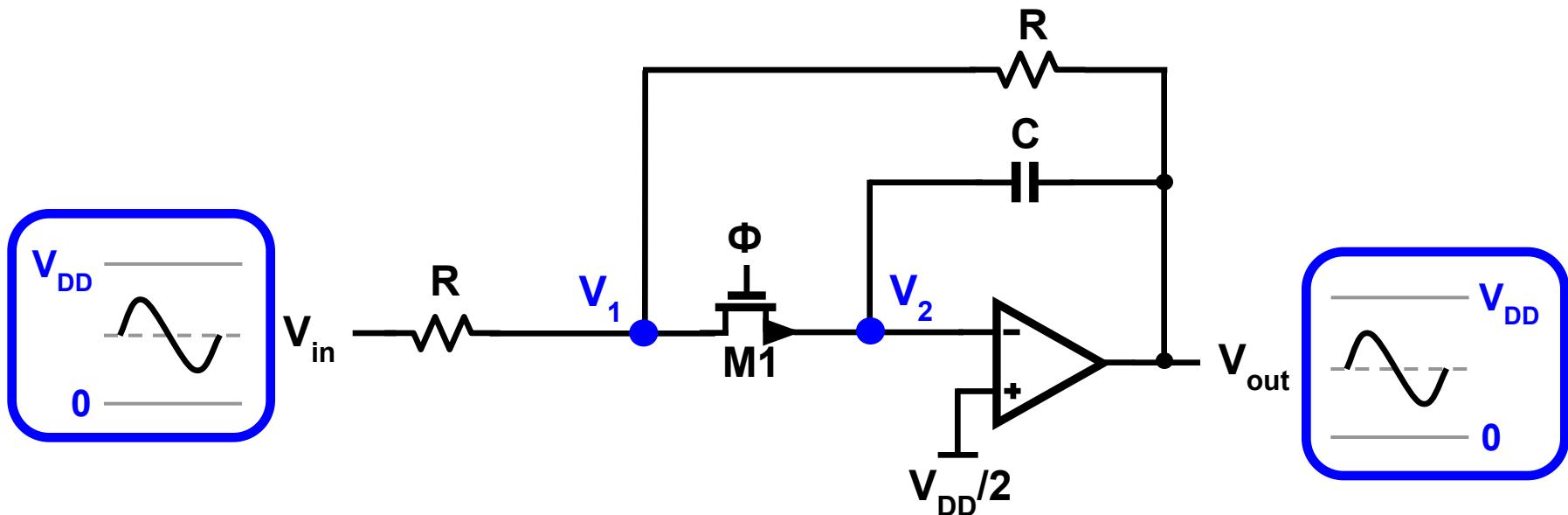


Switched R-MOSFET-C Filter



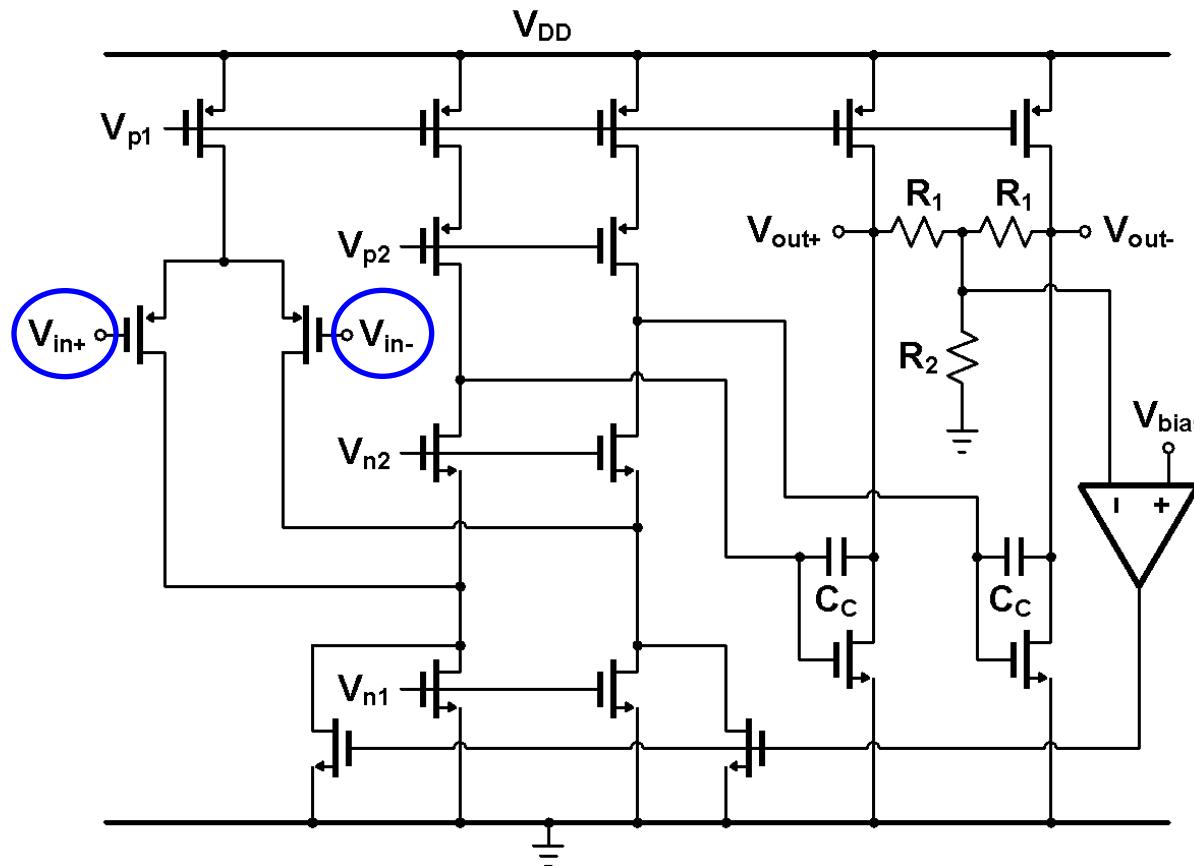
Standard Voltage Operation

- V_{in} and V_{out} should be at $V_{DD}/2$ for maximum signal swing
- But V_1 and V_2 should be near ground
 - for M1 to turn fully on
 - for the use of a low voltage opamp with PMOS inputs



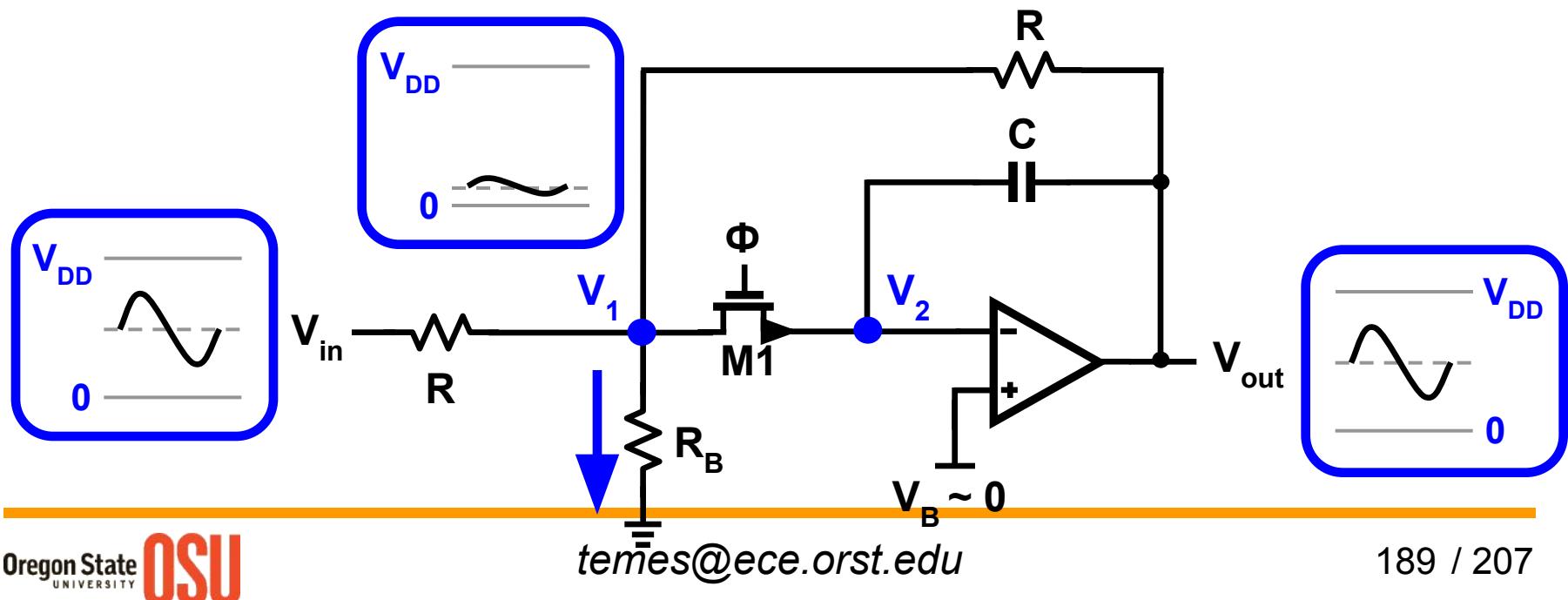
Low Voltage Opamp

- Input common mode is biased toward ground for low-voltage



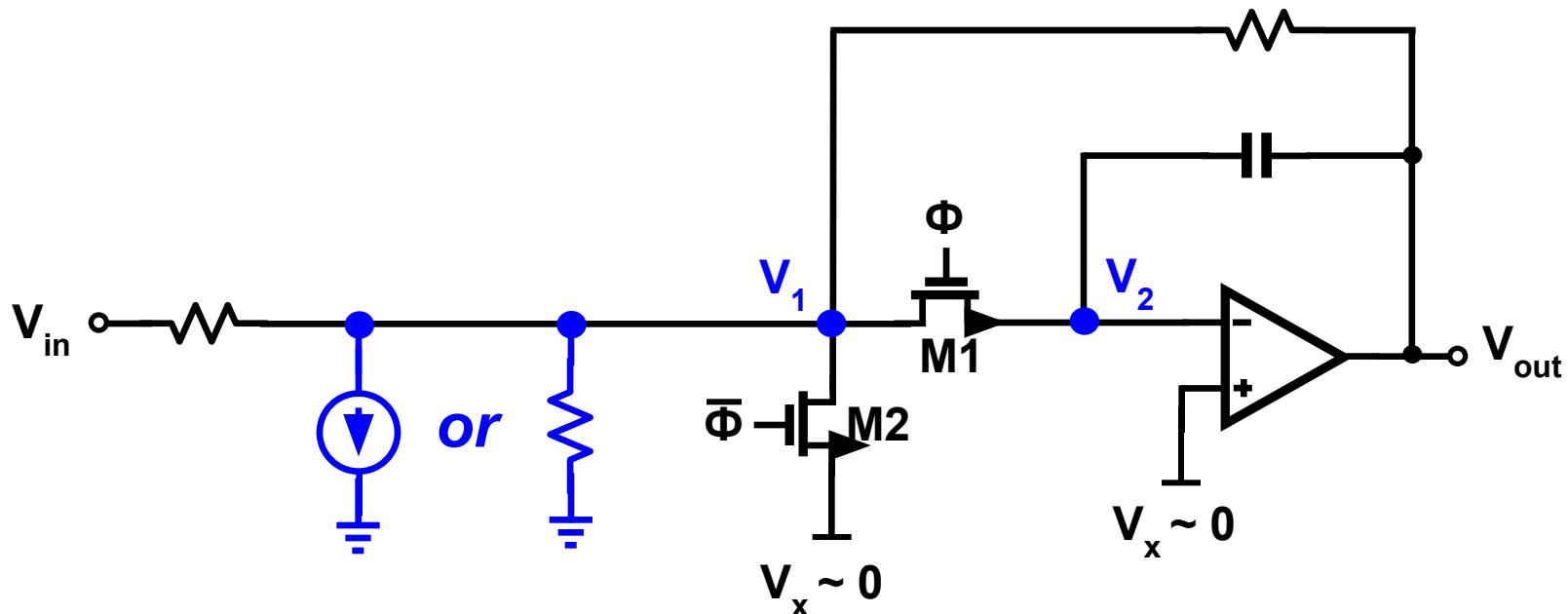
Low Voltage Operation

- V_1 and V_2 can be biased near ground using a resistor R_B (or a current source) [Karthikeyan *et al.*, 2000]
 - No floating switches and biases opamp but ...
 - Increases opamp noise gain



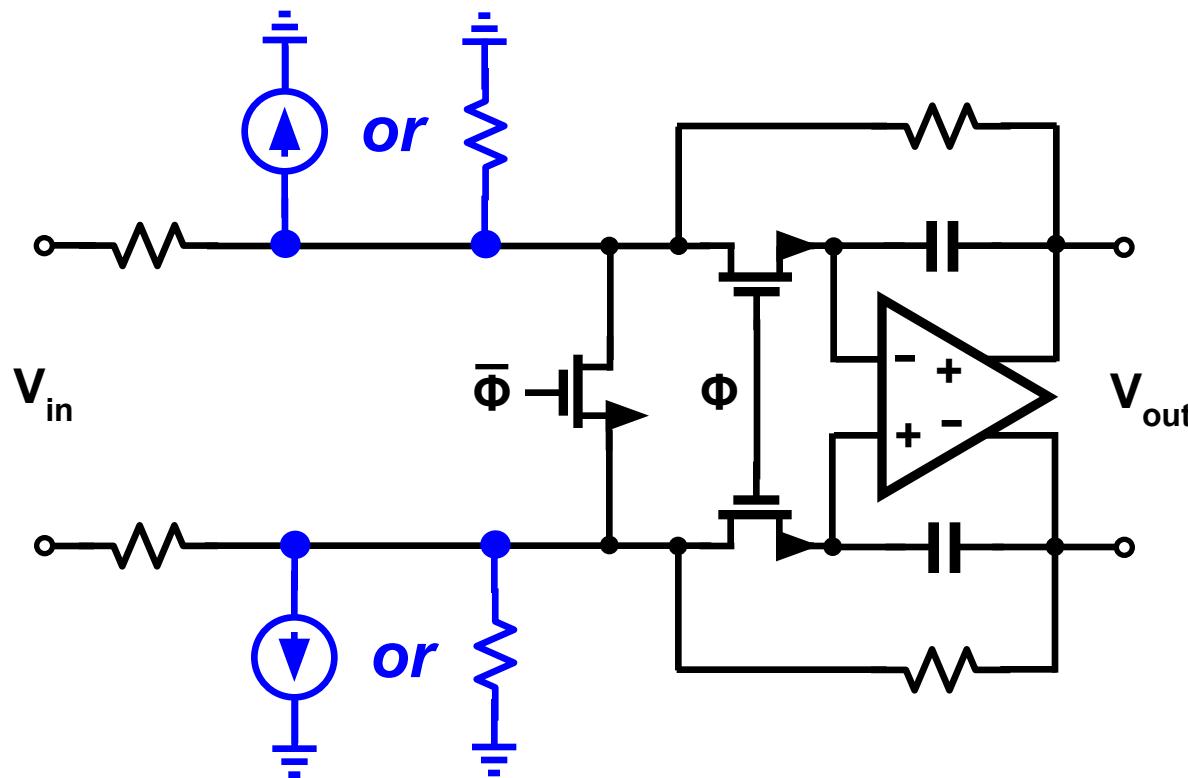
Level-Shifted Low Voltage Operation

- V_1 and V_2 can be biased near ground using a current source or resistor (Karthikeyan TCAS2-2000)
 - Maximizes gate voltage of switches
 - Biases opamp input (PMOS input pair)
- Noise trade-off



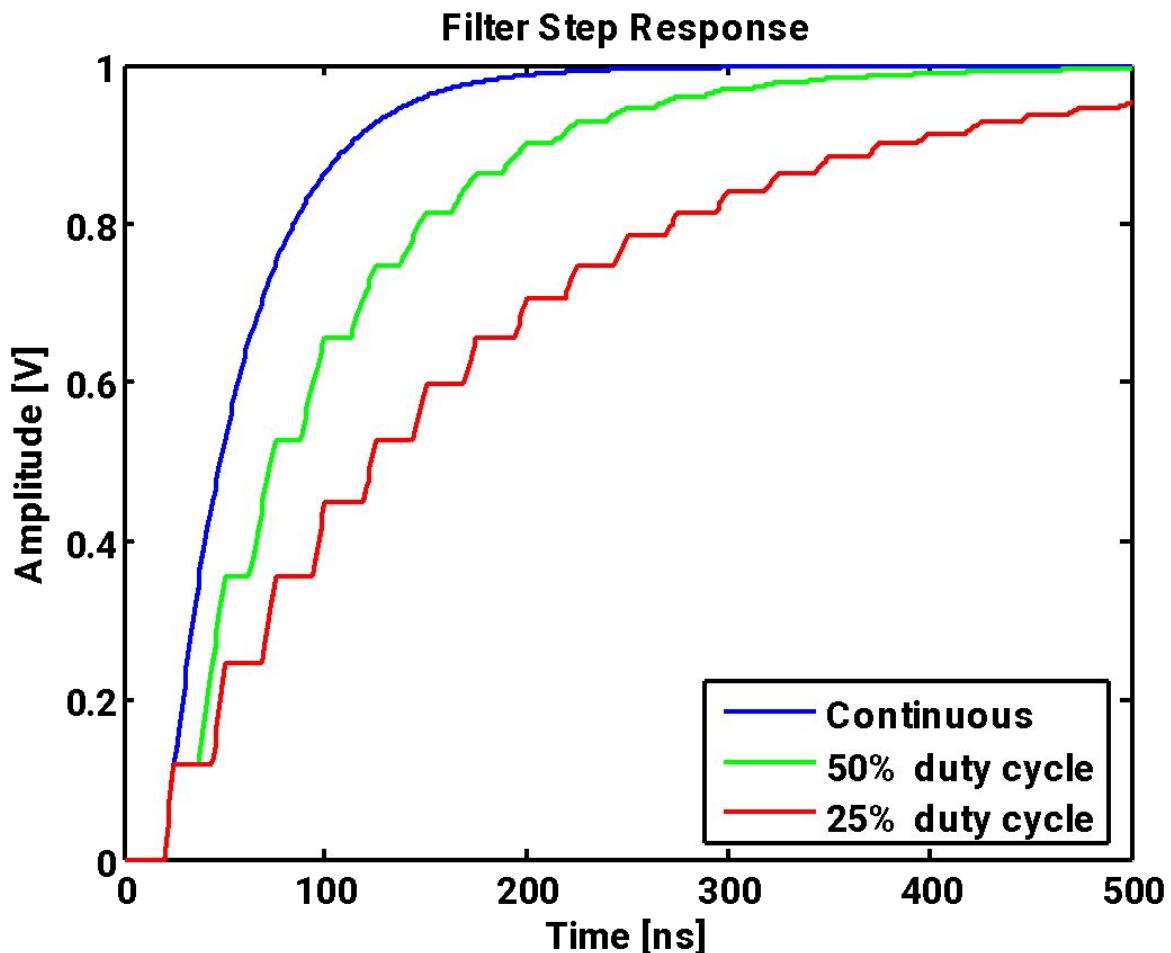
Low Voltage Operation (Differential)

- Voltage divider determines opamp input common-mode



Switching Dynamics

- Track and hold operation
- Time constant depends on duty cycle
- Time constant independent of clock frequency

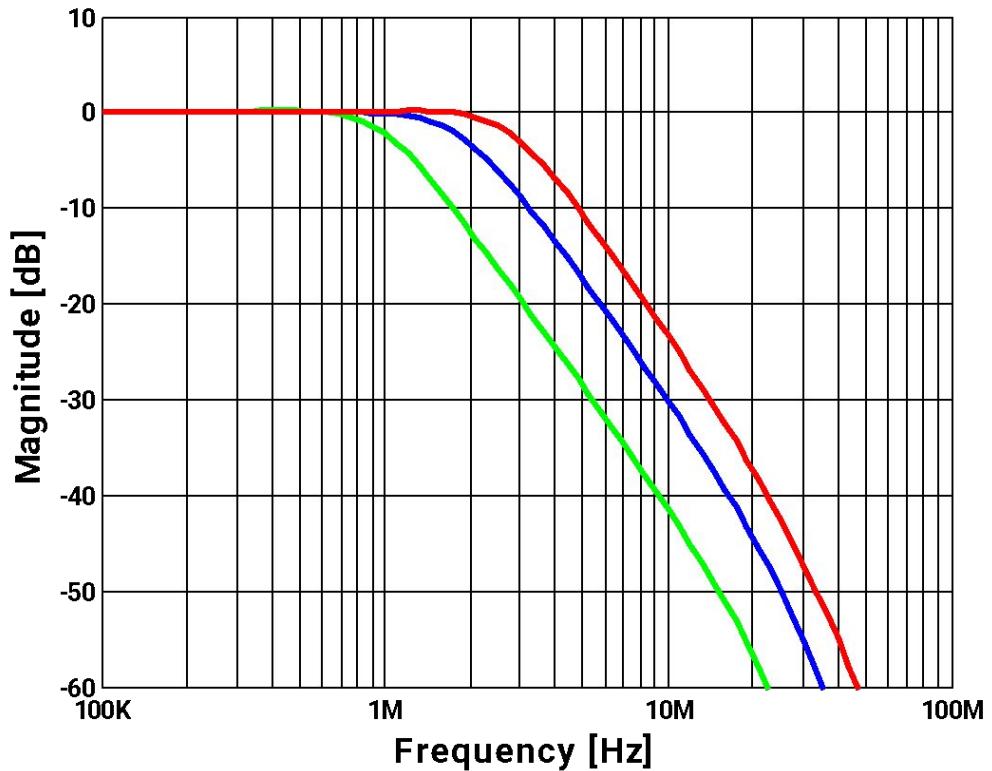


Corner Frequency Tuning

$$f_{\text{corner}} = f_{\text{continuous}} \times \text{duty cycle} / 100$$

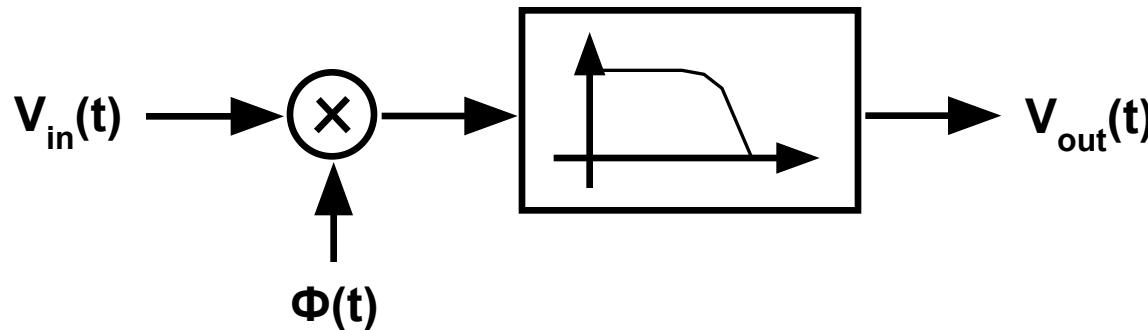
$$f_{\text{continuous}} = 4\text{MHz}$$

	f_{corne}	duty cycle
—	1MHz	25%
—	2MHz	50% nominal
—	3MHz	75%

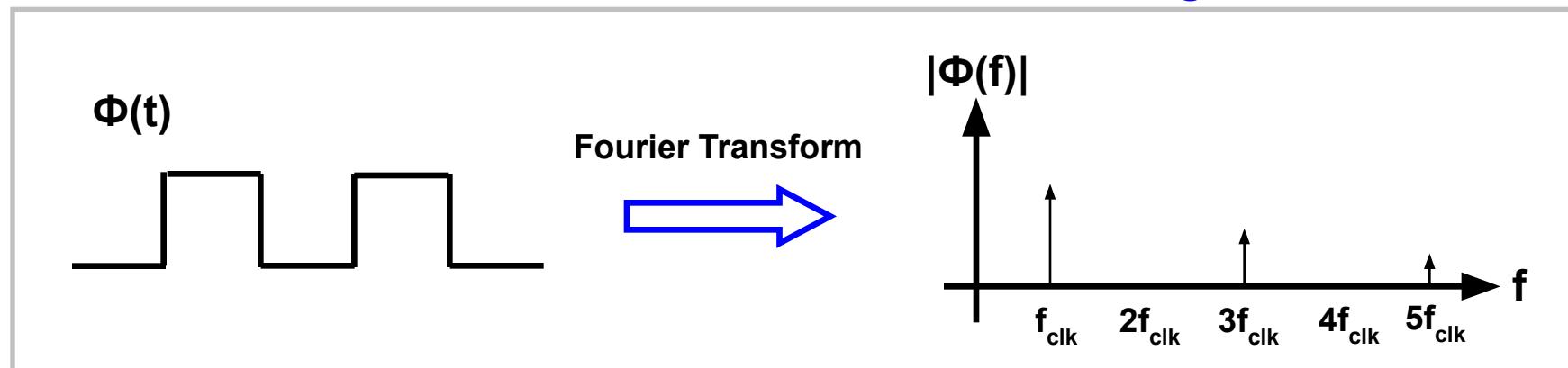


Signal Modulation Effect

- Filter model
- Modulation occurs before filtering

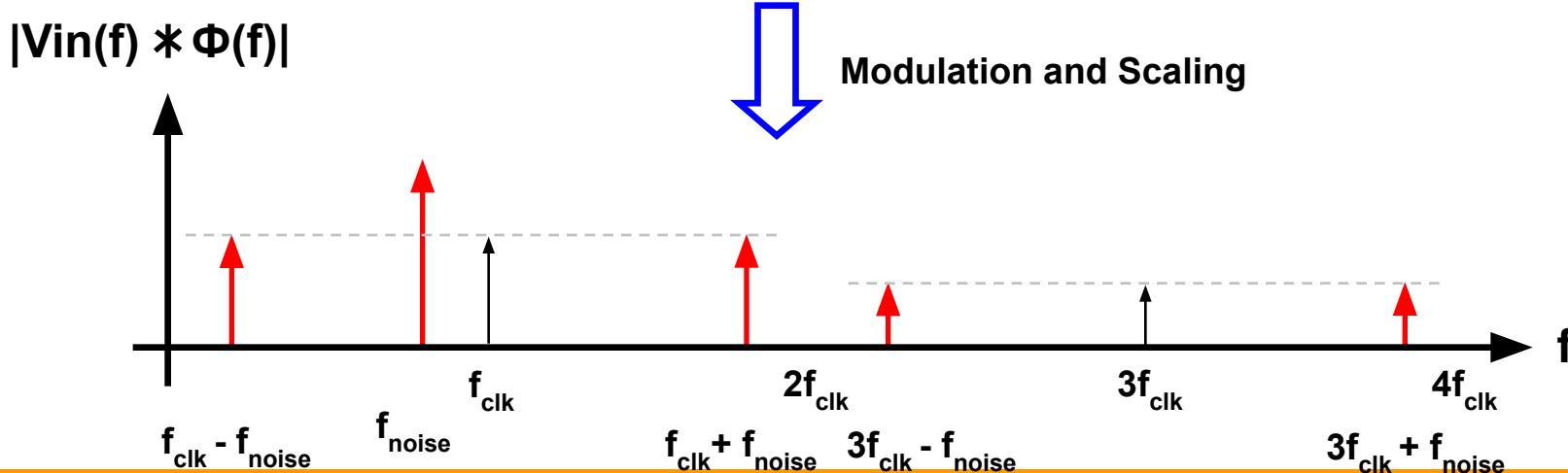
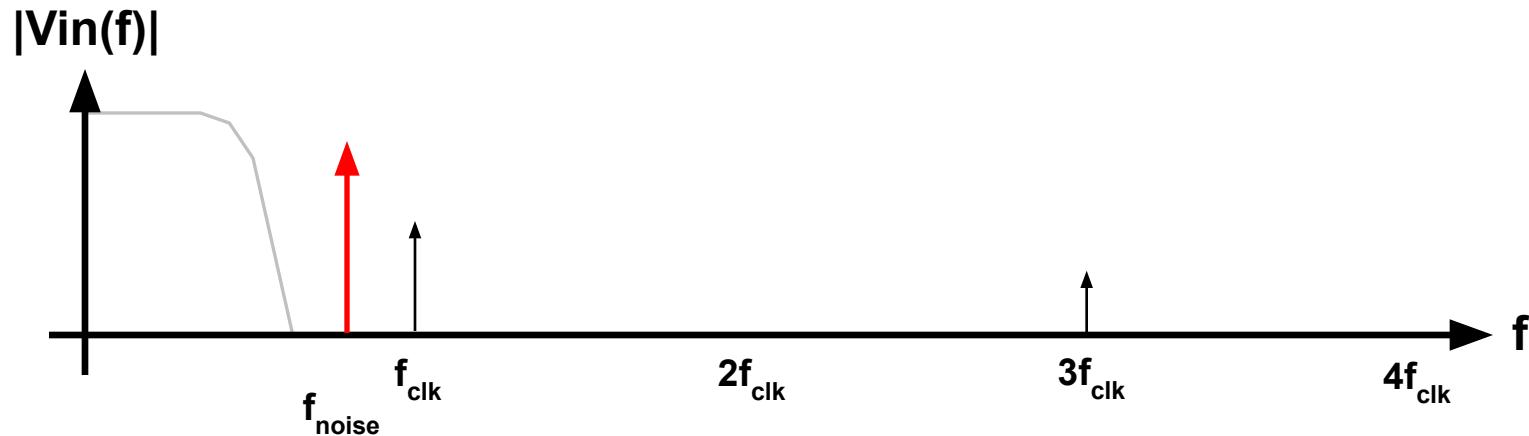


Anti-aliasing filter is needed



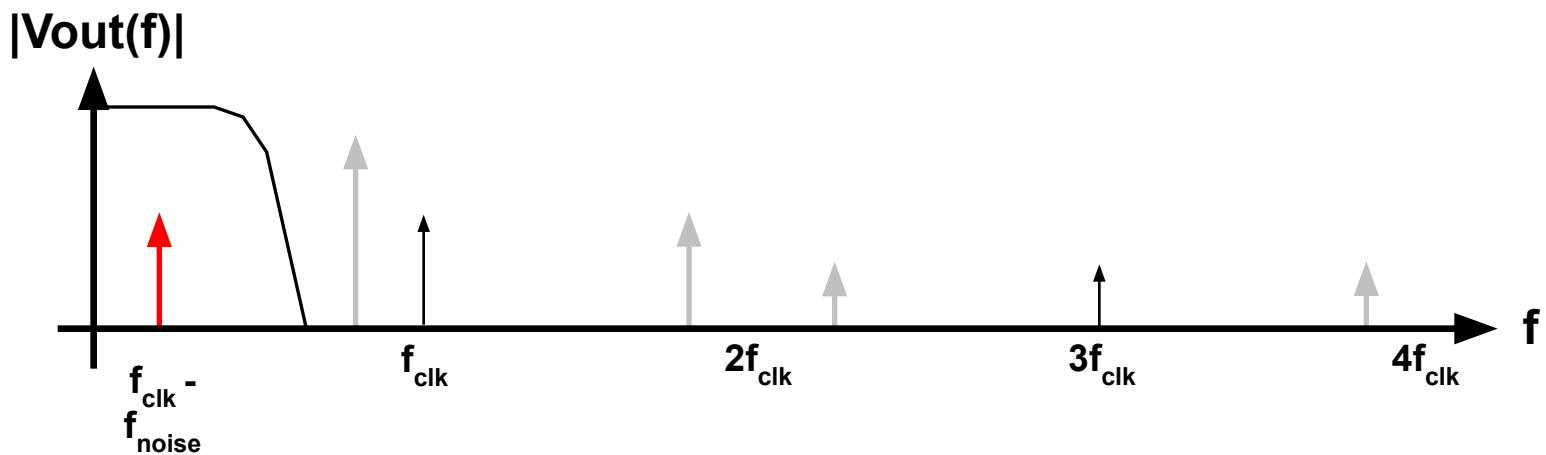
Signal Modulation Effect

Step 1) Input noise signal modulated by clock



Signal Modulation Effect

Step 2) Signal is filtered

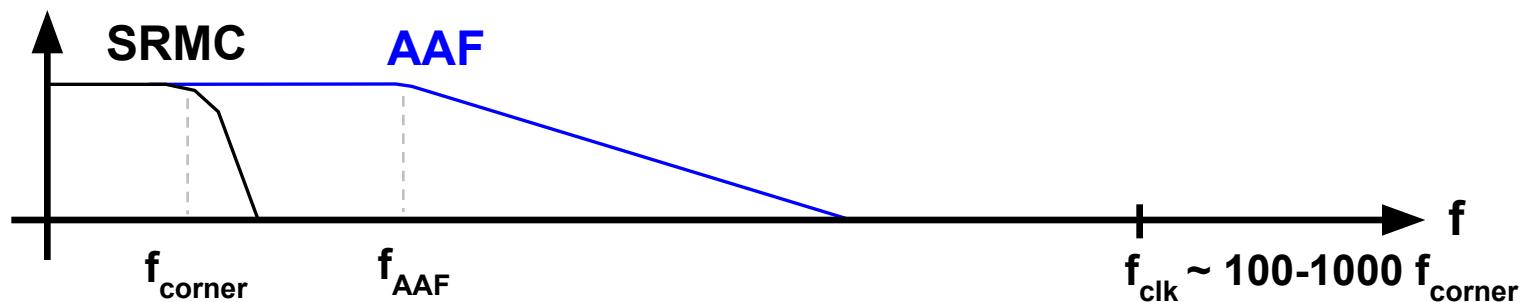


- ◆ Anti-aliasing filter is needed

Anti-Aliasing Filter

SRMC permits high clock frequency

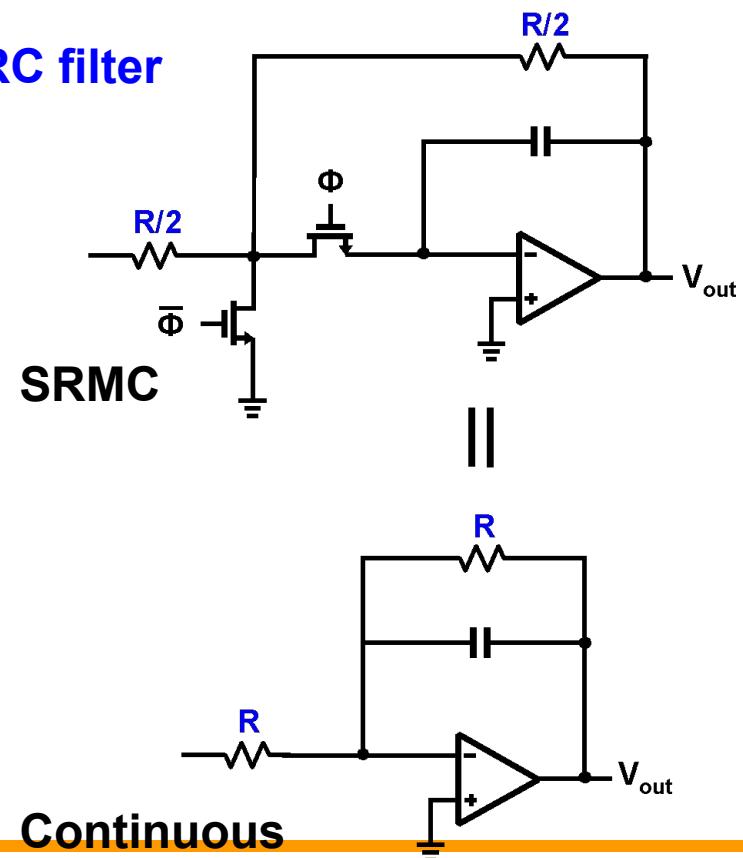
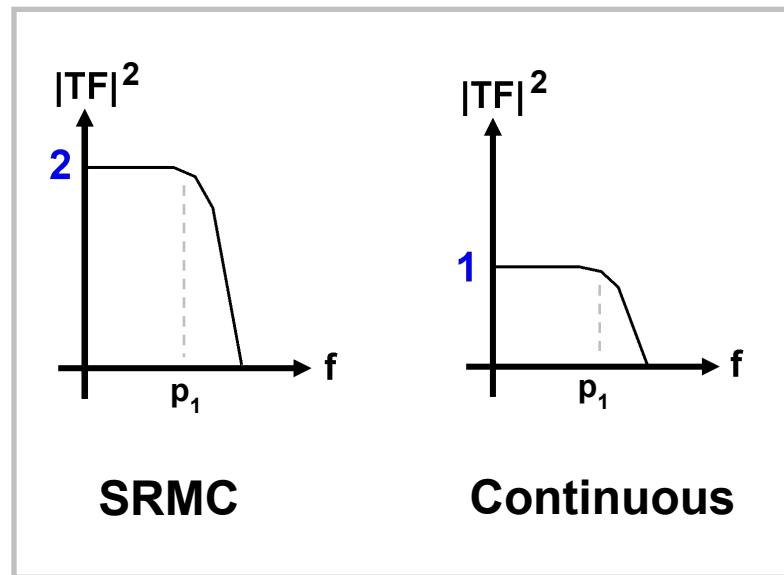
- No capacitor settling requirements
- Relaxed anti-aliasing filter requirements



Resistor Noise

- ◆ Modulation causes noise aliasing
- ◆ Continuous vs. SRMC
 - Noise aliasing causes noise transfer function to double (at 50% duty cycle)
 - Total noise is equivalent standard RC filter

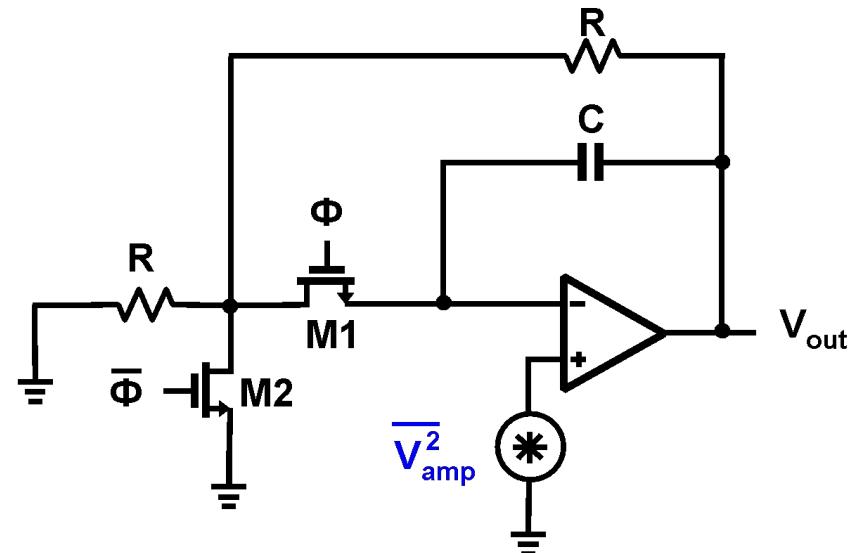
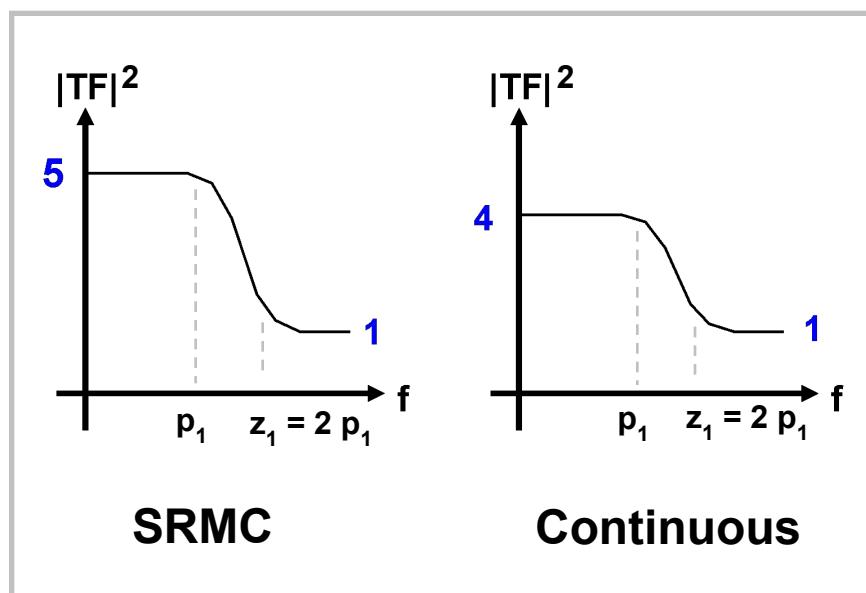
Noise Transfer Function



Opamp Noise

- Modulation Causes Noise Aliasing
- Opamp noise transfer function is 25% higher in SRMC (at 50% duty cycle)

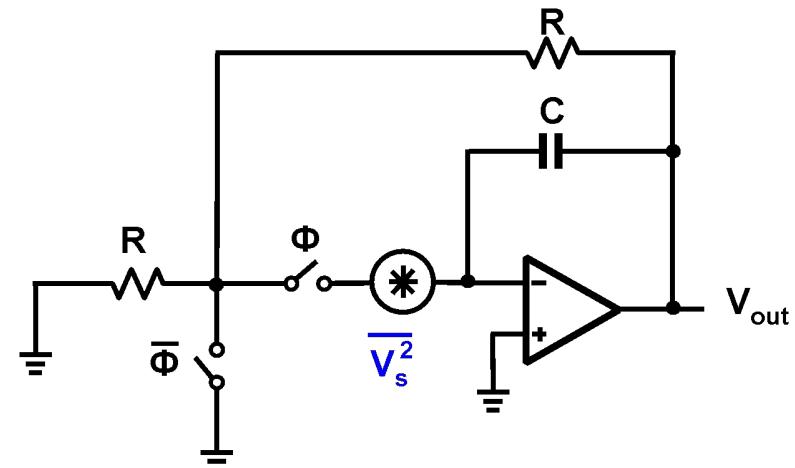
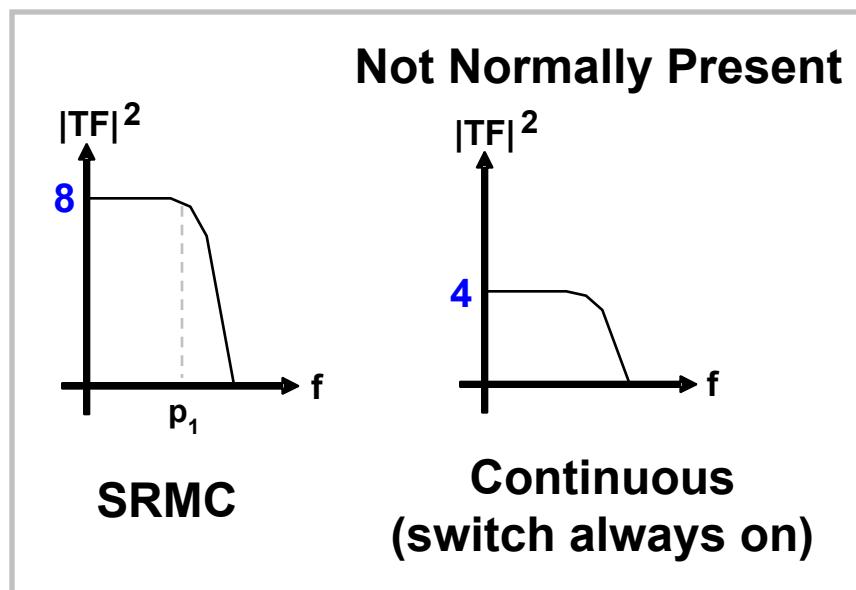
Noise Transfer Function



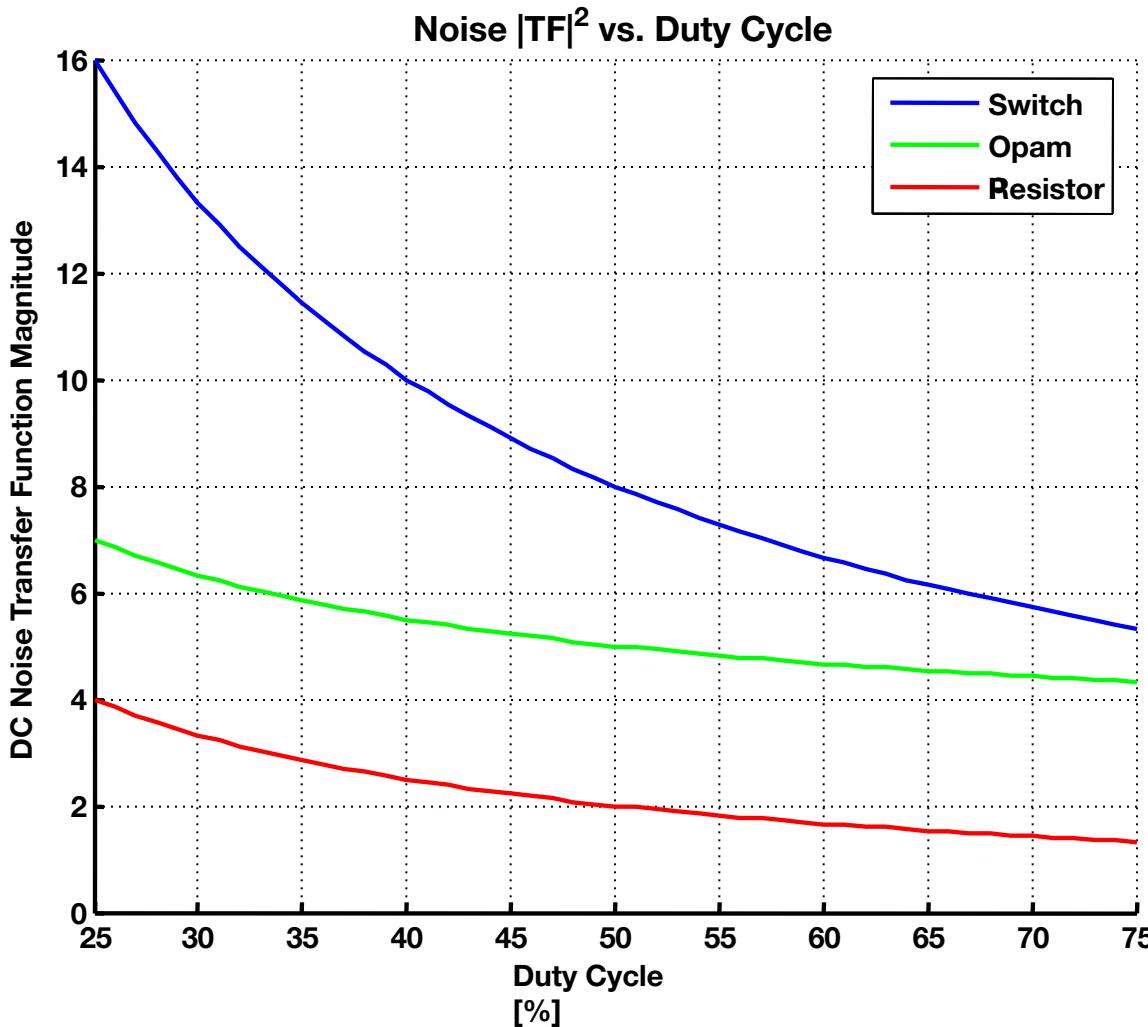
Switch Noise

- Modulation causes noise aliasing
 - Noise aliasing causes noise transfer function to double
- Switch not present in continuous case, but this noise adds little (negligible) in SRMC

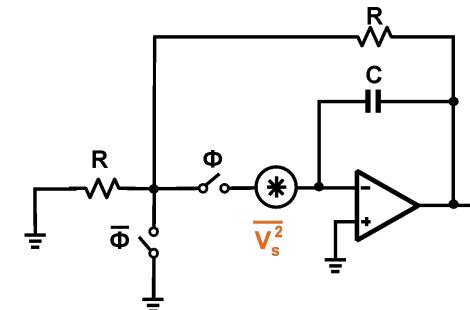
Noise Transfer Function



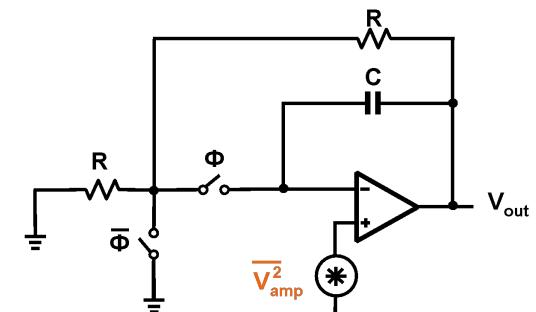
Noise Transfer Function



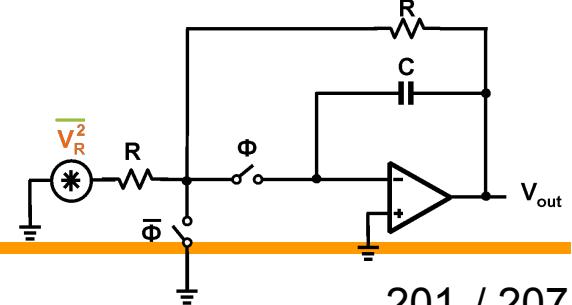
Switch



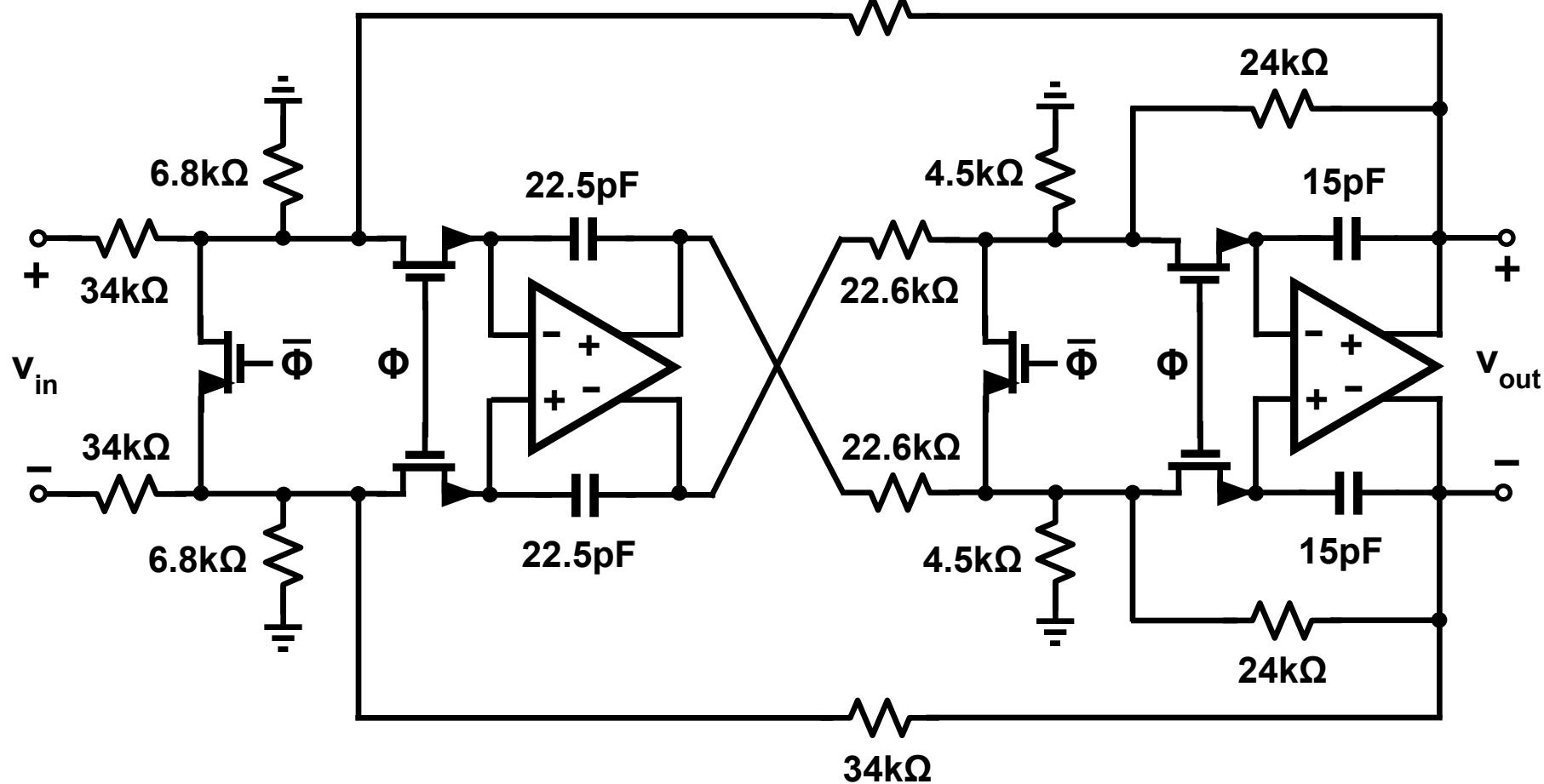
Opamp



Resistor



SRMC Biquad Implementation (Tow-Thomas)



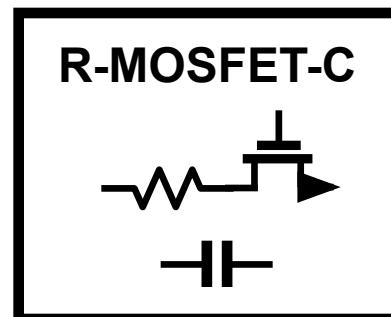
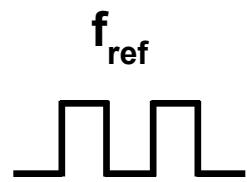
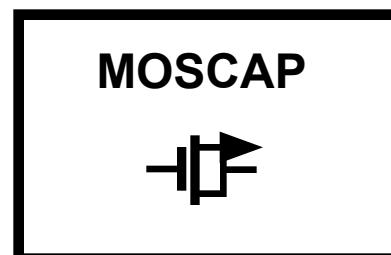
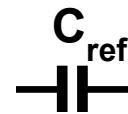
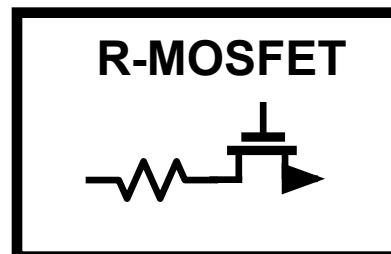
$$f_{-3\text{dB}} = 135\text{kHz} / f_{\text{clock}} = 128\text{MHz} / f_{\text{reference}} = 2\text{MHz}$$

References for Tuning

Off-chip Reference



On-chip Tuning Device



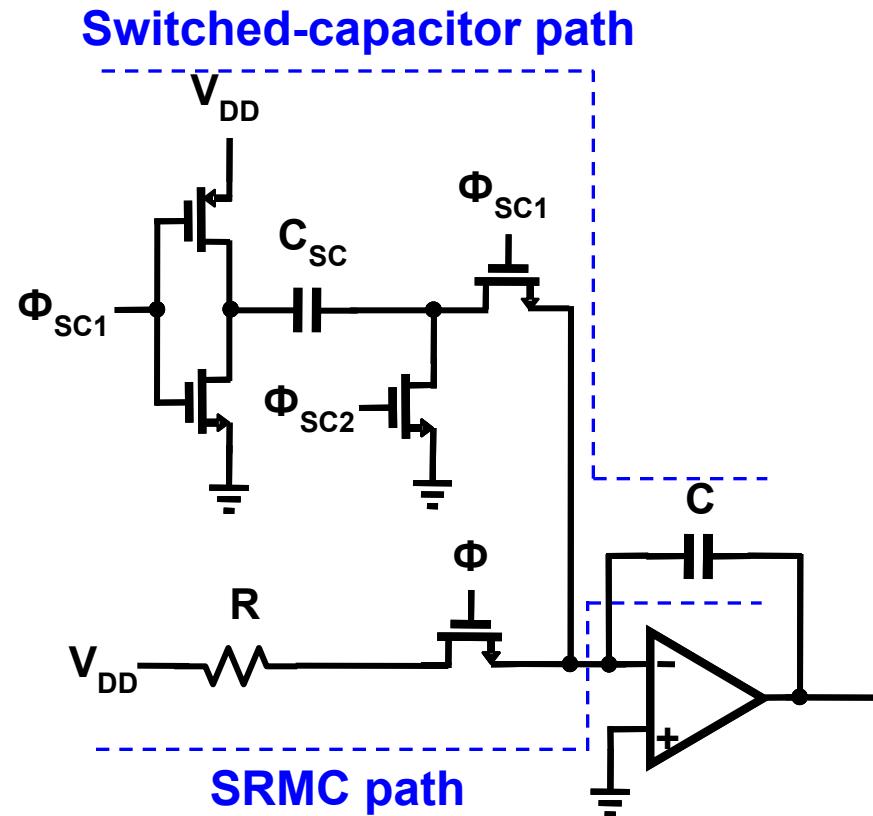
Duty Cycle Based Tuning Circuit (Master)

- Branch currents will be equal when:

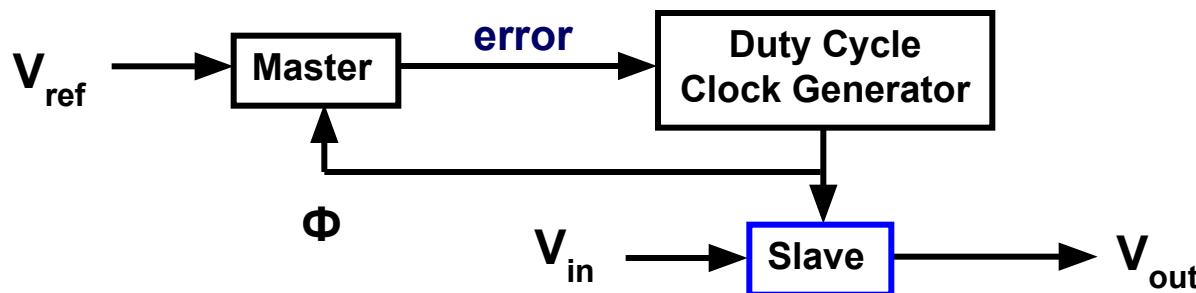
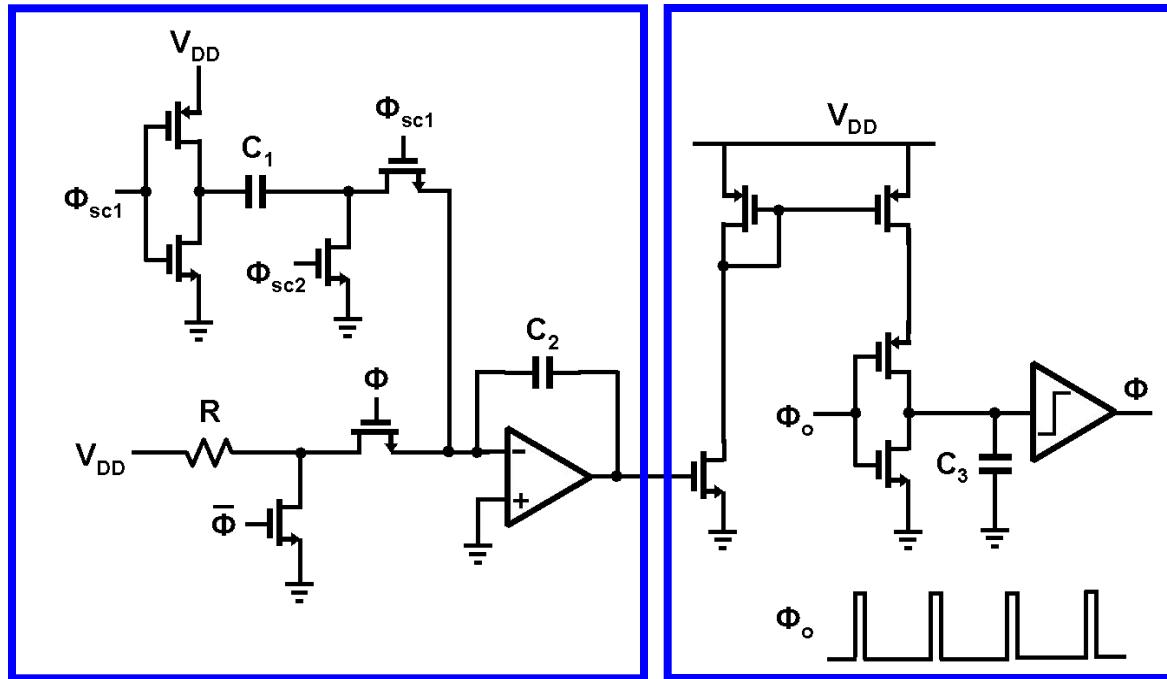
reference clock frequency

$$f_{sc} = \frac{1}{R_{eq} C_{sc}}$$

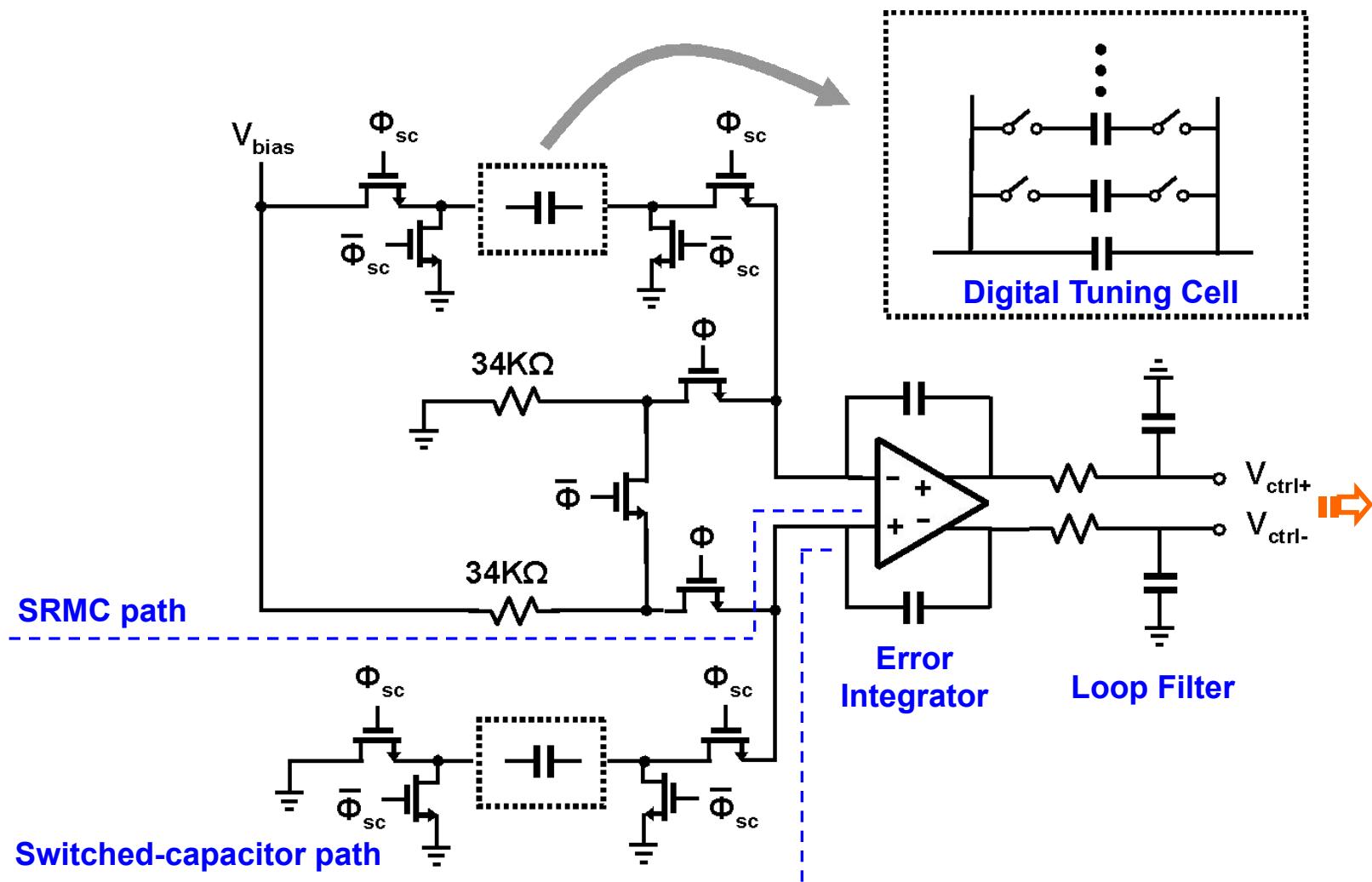
SRMC branch resistance



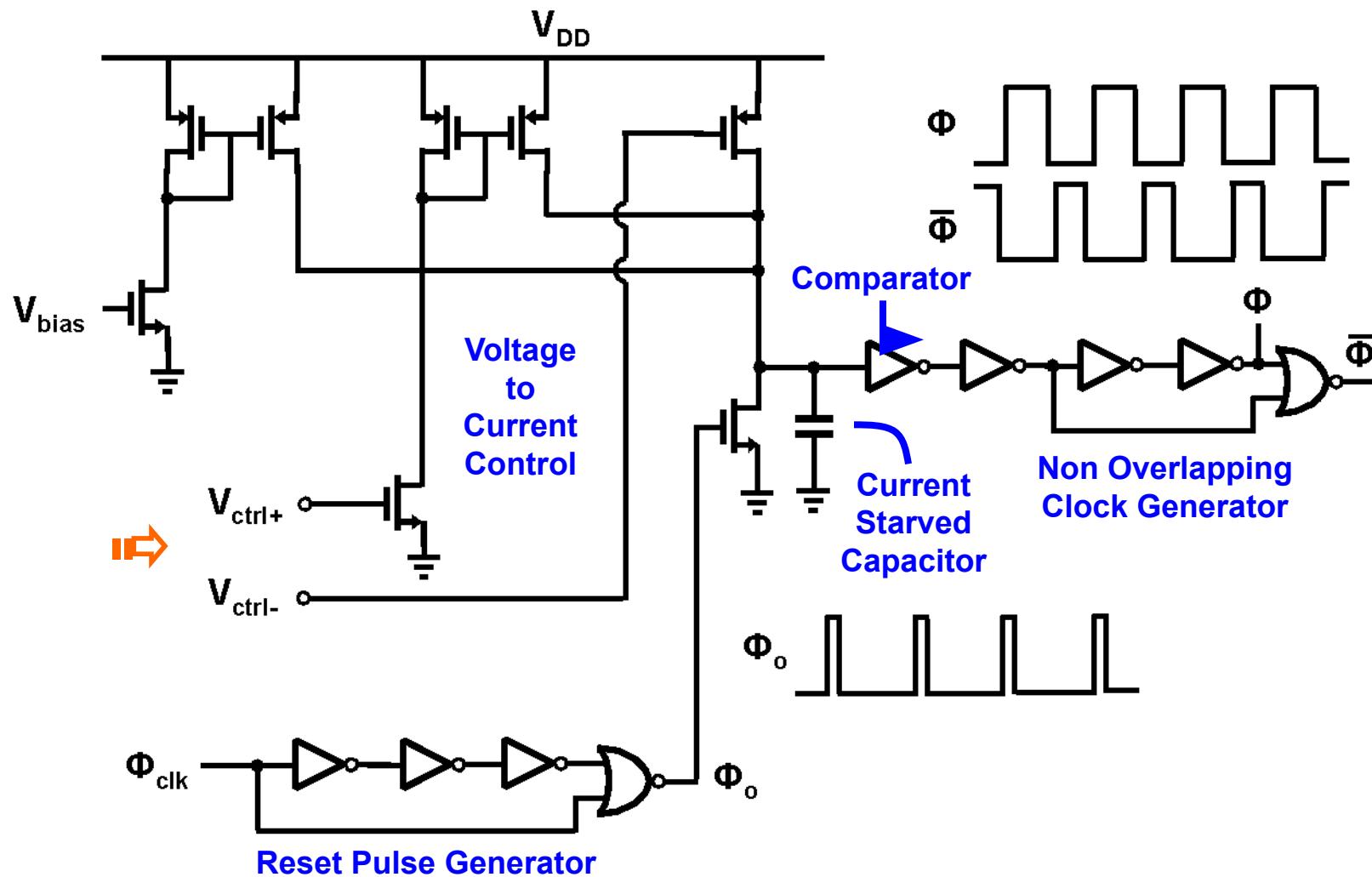
Master-Slave Tuning Circuit



Differential Time Constant Comparison

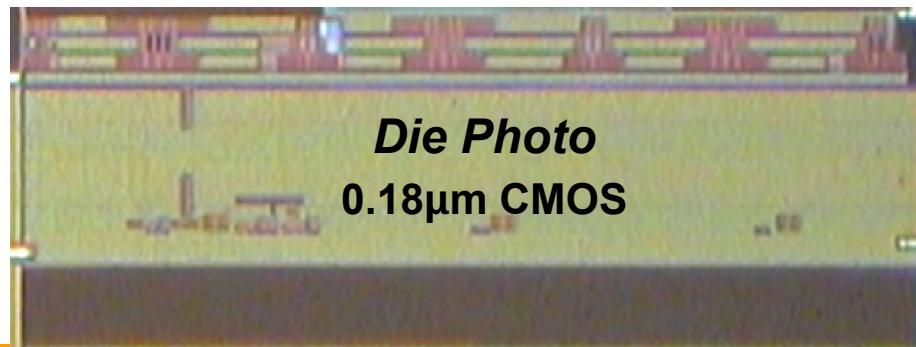
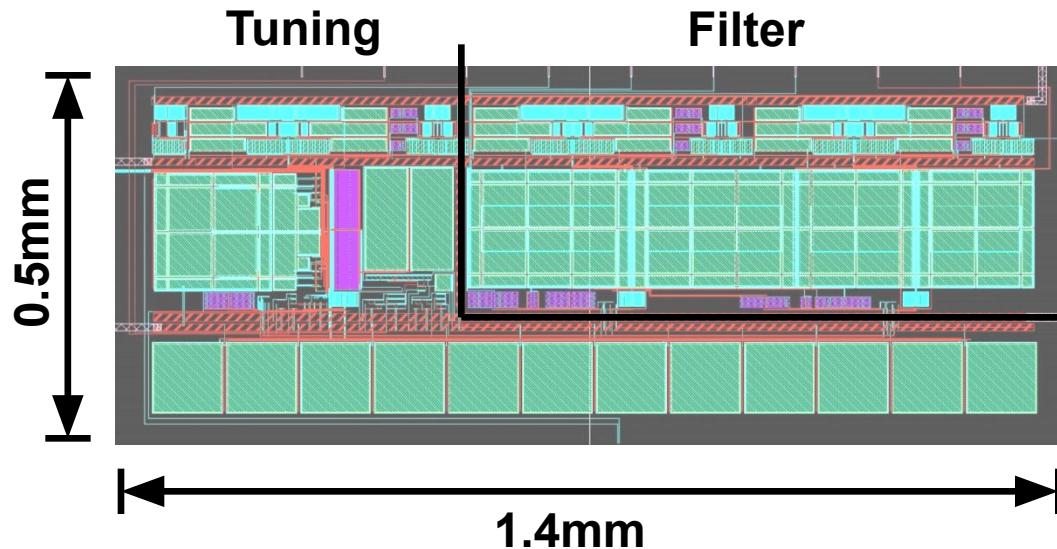


Duty Cycle Clock Generator Detail



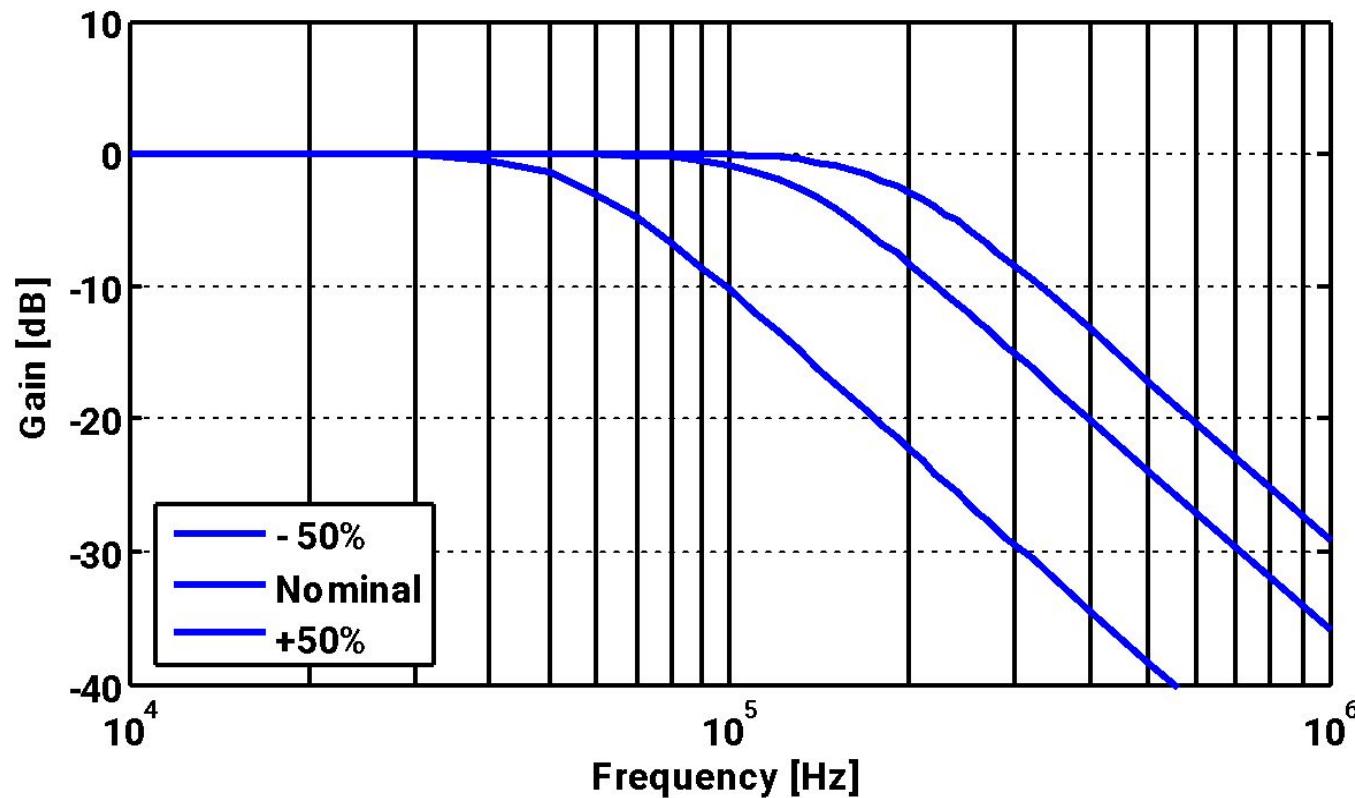
SRMC Filter Prototype IC Layout

Kurahashi *et al.*, CICC-2006 (to appear)



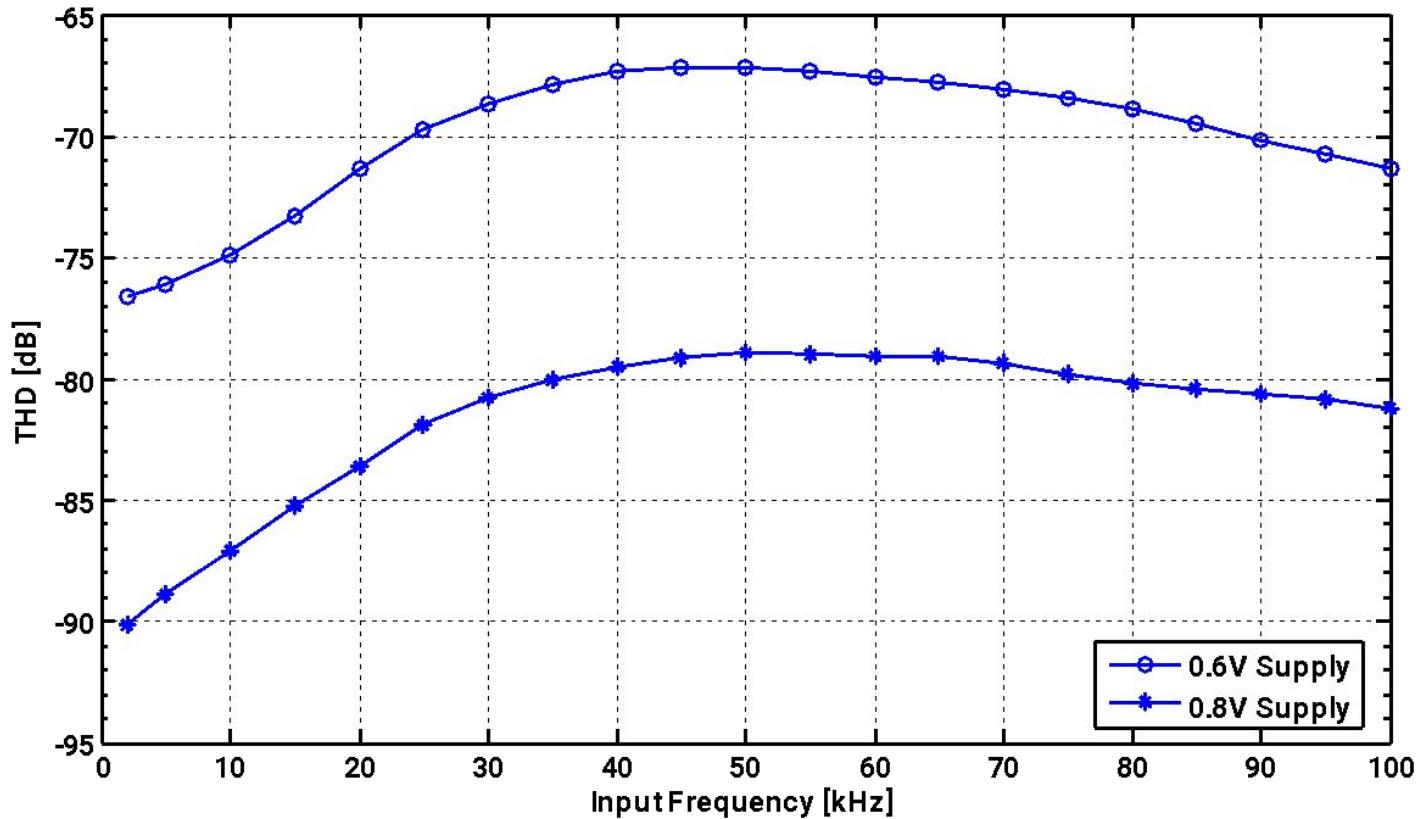
Measured Filter Response

135kHz cutoff frequency



Measured THD

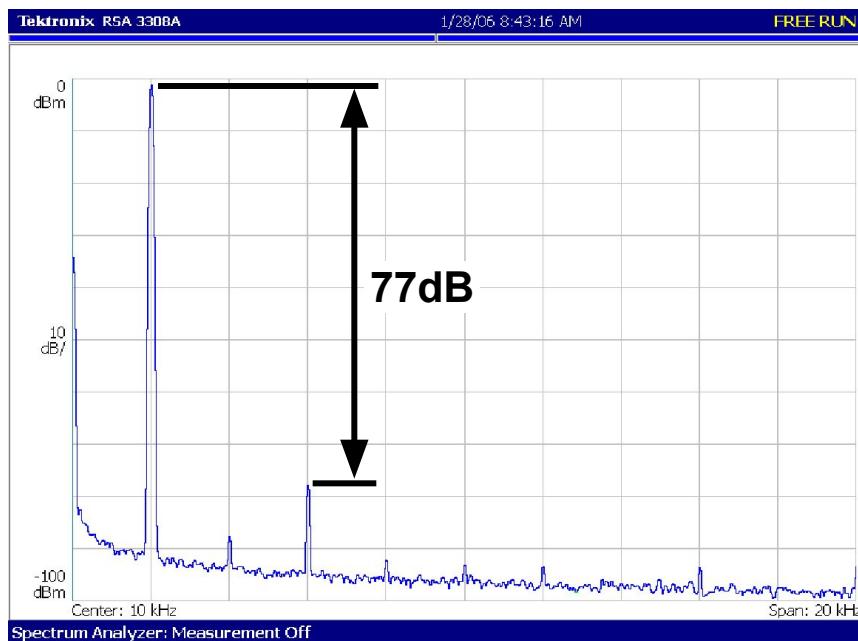
Input amplitude = 0.6Vpp (differential)



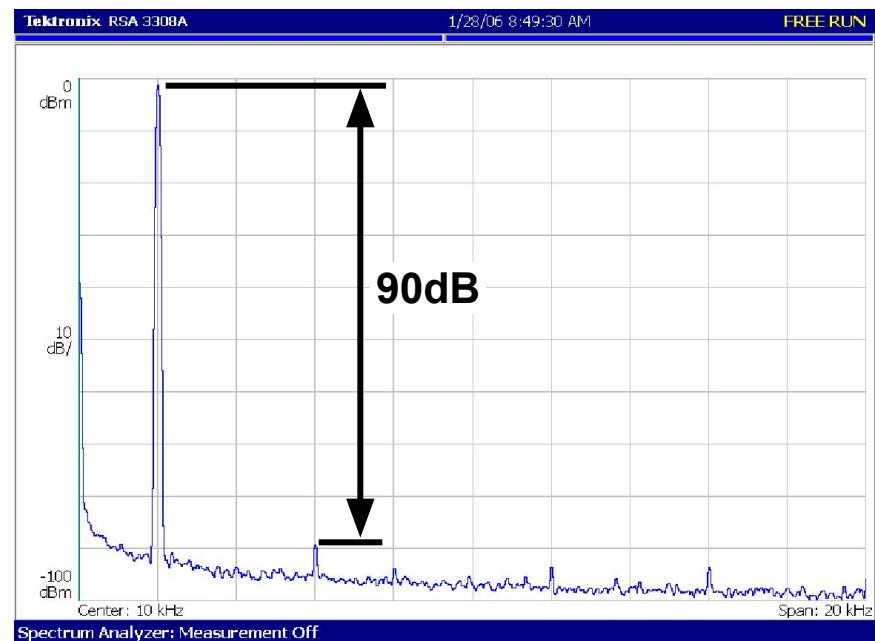
Measured Output Spectrum

Input amplitude = 0.6Vpp (differential)

0.6V Supply



0.8V Supply



Measured SNR

- Integrated from 1kHz
- Referred to 0.6Vpp input

