

```

1  library ieee;
2  use ieee.std_logic_1164.all;
3      --virara um component em meu_pacote_mux4x2.vhd
4  entity dem2x4 is
5
6      port(      aux3 : in std_logic_vector(1 downto 0);
7                aux4 : out std_logic_vector(3 downto 0)
8            );
9  end dem2x4;
10
11  architecture arq of dem2x4 is
12
13      begin
14          aux4 <= "0001" when aux3 = "00" else
15                  "0010" when aux3 = "01" else
16                  "0100" when aux3 = "10" else
17                  "1000" when aux3 = "11";
18      end arq;
19  end architecture arq;

```