

```

1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use ieee.numeric_std.all;
4  use work.meu_pacote_led.all;
5
6  entity somachaves is
7
8      port(    soma: inout std_logic_vector(11 downto 0);
9              chaves: in std_logic_vector(7 downto 0);
10             saida3: out integer range 0 to 15;
11             saida2: out integer range 0 to 15;
12             saida1: out integer range 0 to 15                );
13 end somachaves;
14
15 architecture arq of somachaves is
16
17     begin
18
19         soma <= to_bcd( chaves );
20         saida3 <= to_integer(unsigned( soma(11 downto 8) ));
21         saida2 <= to_integer(unsigned( soma(7  downto 4) ));
22         saida1 <= to_integer(unsigned( soma(3  downto 0) ));
23
24     end arq;
25
26

```