

```

1
2 library ieee;
3 use ieee.std_logic_1164.all;
4 use ieee.numeric_std.all;
5
6 entity decod_7_seg is
7
8     GENERIC (N : integer := 3);
9     port(
10         chaves: in std_logic_vector(3 downto 0);
11         anodos: out std_logic_vector(3 downto 0);
12         catodos: out std_logic_vector(0 to 7)
13     );
14 end decod_7_seg;
15
16 architecture arq of decod_7_seg is
17     begin
18
19         anodos <= not("1111");
20         --          0|aceso 1|apagado
21         catodos <=
22         not("11111100") when chaves = "0000" else -- 0
23         not("01100000") when chaves = "0001" else -- 1
24         not("11011010") when chaves = "0010" else -- 2
25         not("11110010") when chaves = "0011" else -- 3
26         not("01100110") when chaves = "0100" else -- 4
27         not("10110110") when chaves = "0101" else -- 5
28         not("10111110") when chaves = "0110" else -- 6
29         not("11100000") when chaves = "0111" else -- 7
30         not("11111110") when chaves = "1000" else -- 8
31         not("11110110") when chaves = "1001" else -- 9
32         not("11101110") when chaves = "1010" else -- A
33         not("00111110") when chaves = "1011" else -- b
34         not("10011100") when chaves = "1100" else -- C
35         not("01111010") when chaves = "1101" else -- d
36         not("10011110") when chaves = "1110" else -- E
37         not("10001110") when chaves = "1111"; -- F
38         --not("11100000"); -- F
39
40     end arq;
41

```