

```

1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3
4  package meu_pacote_led is
5
6      component ccto is
7          generic (N : integer);
8          port(    mclk, reset: in std_logic;
9                  clk: out std_logic      );
10 end component;
11
12 component ccto2 is
13     generic (N : integer);
14     port(    mclk, reset: in std_logic;
15             clk: out std_logic      );
16 end component;
17
18 component ccto3 is
19     generic (N : integer);
20     port(    mclk, reset: in std_logic;
21             clk: out std_logic      );
22 end component;
23
24 component ccto4 is
25     generic (N : integer);
26     port(    mclk, reset: in std_logic;
27             clk: out std_logic      );
28 end component;
29
30
31 component decod_7_seg is
32
33     GENERIC (N : integer := 3);
34     port(
35         chaves: in std_logic_vector(N-1 downto 0);
36         anodos: out std_logic_vector(N-1 downto 0);
37         catodos: out std_logic_vector(0 to 7)      );
38
39 end component;
40
41 end package;
42

```