```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use work.meu_pacote_led.all;

entity top is

    GENERIC (N : integer := 4);
    port(mclk, reset: in std_logic;
        anodos: out std_logic_vector(3 downto 0);
        catodos: out std_logic_vector(0 to 7)           );

end top;

architecture Behavioral of top is

    signal clk1, clk2, clk3, clk4:  std_logic;
    signal aux3 : std_logic_vector(3 downto 0);
    begin
        map1 : entity work.ccto(arq)
        generic map (N => N)
        port map( mclk, reset,  clk1 ); --in,in,out

        map2 : entity work.ccto2(arq)
        generic map (N => N)
        port map( mclk, reset,  clk2 ); --in,in,out

        map3 : entity work.ccto3(arq)
        generic map (N => N)
        port map( mclk, reset,  clk3 ); --in,in,out

        map4 : entity work.ccto4(arq)
        generic map (N => N)
        port map( mclk, reset,  clk4 ); --in,in,out

        aux3 <= clk4 & clk3 & clk2 & clk1 ;

        map5 : entity work.decod_7_seg(arq)
        port map(aux3, anodos, catodos);        --entrada,saida,saida


end Behavioral;
```