

```

1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3
4  package meu_pacote_led is
5
6      component ccto is
7          generic (N : integer);
8          port(    mclk, reset: in std_logic;
9                  clk: out std_logic      );
10 end component;
11
12 component ccto2 is
13     generic (N : integer);
14     port(    mclk, reset: in std_logic;
15             clk: out std_logic      );
16 end component;
17
18
19 component mux2x1 is
20     port(    seletor: in std_logic;
21             entrada1: in integer range 0 to 15;
22             entrada2: in integer range 0 to 15;
23             saida: out integer range 0 to 15      );
24 end component;
25
26 component dem2x4 is
27     port(    aux3 : in std_logic_vector(1 downto 0);
28             aux4 : out std_logic_vector(3 downto 0)      );
29 end component;
30
31 component decod_7_seg is
32
33     GENERIC (N : integer := 3);
34     port(
35         chaves: in std_logic_vector(3 downto 0);
36         chaves_display: in std_logic_vector(3 downto 0);
37         anodos: out std_logic_vector(3 downto 0);
38         catodos: out std_logic_vector(0 to 7)      );
39
40 end component;
41
42 end package;
43

```