```vhdl
library ieee;
use ieee.std_logic_1164.all;
    --virara umcomponent em meu_pacote_mux4x2.vhd


entity mux2x1 is

    port(   seletor: in std_logic;
            entrada1: in integer range 0 to 15;
            entrada2: in integer range 0 to 15;
            saida: out integer range 0 to 15            );
end mux2x1;

architecture arq of mux2x1 is

    begin

         saida <= entrada2 when seletor='1' else entrada1;

end arq;
```