```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use work.meu_pacote_led.all;

entity top is

    --GENERIC (N : integer := 10);
    port(   mclk, reset: in std_logic;
             clk1, clk2: out std_logic      );
end top;

architecture Behavioral of top is


    begin
        map1 : entity work.ccto(arq)
        port map( mclk, reset, clk1 );  --in,out

        map2 : entity work.ccto2(arq)
        port map( mclk, reset,  clk2  );    --in,out

end Behavioral;


```