```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity tb_ccto is
end tb_ccto;

architecture tb_arq of tb_ccto is
    signal mclk, reset, clk,clk2 : std_logic := '0';
    constant mclk_period : time := 100 ms;

begin
    uut: entity work.top( Behavioral )
    port map (mclk, reset, clk,clk2);

    process begin
        mclk <= '0'; wait for mclk_period/2;
        mclk <= '1'; wait for mclk_period/2;
    end process;
end;
```