

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3
4  package meu_pacote_led is
5
6      component ccto is
7          generic (N : integer);
8          port(    mclk, reset: in std_logic;
9                 clk: out std_logic      );
10 end component;
11
12 component ccto2 is
13     generic (N : integer);
14     port(    mclk, reset: in std_logic;
15            clk: out std_logic      );
16 end component;
17
18 component ccto3 is
19     generic (N : integer);
20     port(    mclk, reset: in std_logic;
21            clk: out std_logic      );
22 end component;
23
24 component ccto4 is
25     generic (N : integer);
26     port(    mclk, reset: in std_logic;
27            clk: out std_logic      );
28 end component;
29
30
31 end package;
32
```