

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity tb_ccto is
5  end tb_ccto;
6
7  architecture tb_arq of tb_ccto is
8      signal mclk, reset : std_logic := '0';
9      signal vetor_bit: std_logic_vector (3 downto 0) ;
10     constant mclk_period : time := 100 ms;
11
12 begin
13     uut: entity work.top( Behavioral )
14     port map (mclk, reset, vetor_bit);
15
16     process begin
17         mclk <= '0'; wait for mclk_period/2;
18         mclk <= '1'; wait for mclk_period/2;
19     end process;
20     reset <= '1', '0' after mclk_period/2;
21 end;
```