

```

1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity ccto2 is
5      generic (N : integer);
6      port(    mclk, reset: in std_logic;
7              clk: out std_logic          );
8  end entity;
9
10 architecture arq of ccto2 is
11
12     constant M: integer := 2*50_000_000 ;
13
14     begin
15
16         process(mclk, reset)
17             variable i: integer range 1 to M := 1;
18             variable v_clk: std_logic := '0';
19             begin
20                 if (reset = '1') then i := 1; v_clk := '0';
21                 elsif(mclk'event and mclk='1') then i := i + 1;
22                     if (i = M/N) then i := 1; v_clk := not(v_clk);
23                 end if;
24                 clk <= v_clk; end if;
25             end process;
26 end arq;

```