```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use work.meu_pacote_led.all;
    --CONTADOR DE 4 BITS
entity top is

    GENERIC (N : integer := 4);
    port(mclk, reset: in std_logic;
               clk1, clk2, clk3, clk4: out std_logic     );
end top;

architecture Behavioral of top is

    begin
        map1 : entity work.ccto(arq)
        generic map (N => N)
        port map( mclk, reset,  clk1 ); --in,in,out

        map2 : entity work.ccto2(arq)
        generic map (N => N)
        port map( mclk, reset,  clk2 ); --in,in,out

        map3 : entity work.ccto3(arq)
        generic map (N => N)
        port map( mclk, reset,  clk3 ); --in,in,out

        map4 : entity work.ccto4(arq)
        generic map (N => N)
        port map( mclk, reset,  clk4 ); --in,in,out

end Behavioral;


```