```
library ieee;
use ieee.std logic 1164.all;
entity ccto2 is
    generic (N : integer);
    port( mclk, reset: in std_logic;
                       clk: out std logic
                                              );
end entity;
architecture arq of ccto2 is
    constant M: integer := 2*50_000_000 ;
    begin
        process(mclk, reset)
            variable i: integer range 1 to M := 1;
            variable v_clk: std_logic := '0';
            if (reset = '1') then i := 1; v_clk := '0';
                elsif(mclk'event and mclk=\overline{1}) then i := i + 1;
                if (i = M/N) then i := 1; v_{clk} := not(v_{clk});
            end if;
            clk <= v clk; end if;</pre>
        end process;
end arg;
```