

```

1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity ccto2 is
5      generic (N : integer);
6      port(    mclk, reset: in std_logic;
7              clk: out std_logic
8          );
9  end entity;
10
11  architecture arq of ccto2 is
12      constant M: integer := 2*50_000_000 ;
13      begin
14
15          process(mclk, reset)
16              variable i: integer range 1 to M := 1;
17              variable v_clk: std_logic := '0';
18              begin
19                  if (reset = '1') then i := 1; v_clk := '0';
20                  elsif(mclk'event and mclk='1') then i := i + 1;
21                      if (i = M/N) then i := 1; v_clk := not(v_clk);
22                  end if;
23                  clk <= v_clk; end if;
24              end process;
25  end arq;

```