

```

1
2 library ieee;
3 use ieee.std_logic_1164.all;
4 use ieee.numeric_std.all;
5
6 entity decod_7_seg is
7
8     GENERIC (N : integer := 3);
9     port(
10         chaves: in std_logic_vector(3 downto 0);
11         chaves_display: in std_logic_vector(3 downto 0);
12         anodos: out std_logic_vector(3 downto 0);
13         catodos: out std_logic_vector(0 to 7)
14     );
15 end decod_7_seg;
16
17 architecture arq of decod_7_seg is
18     begin
19
20         anodos <= not( chaves_display );    -- 0|aceso 1|apagado
21
22         catodos <=
23         not("11111100") when chaves = "0000" else -- 0
24         not("01100000") when chaves = "0001" else -- 1
25         not("11011010") when chaves = "0010" else -- 2
26         not("11110010") when chaves = "0011" else -- 3
27         not("01100110") when chaves = "0100" else -- 4
28         not("10110110") when chaves = "0101" else -- 5
29         not("10111110") when chaves = "0110" else -- 6
30         not("11100000") when chaves = "0111" else -- 7
31         not("11111110") when chaves = "1000" else -- 8
32         not("11110110") when chaves = "1001" else -- 9
33         not("11101110") when chaves = "1010" else -- A
34         not("00111110") when chaves = "1011" else -- b
35         not("10011100") when chaves = "1100" else -- C
36         not("01111010") when chaves = "1101" else -- d
37         not("10011110") when chaves = "1110" else -- E
38         not("10001110") when chaves = "1111"; -- F
39         --not("11100000"); -- F
40
41     end arq;
42

```