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1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.numeric_std.all;
4  use ieee.std_logic_unsigned.all;
5
6  package meu_pacote_led is
7
8      component ccto is
9          generic (N : integer);
10         port( mclk, reset: in std_logic;
11              clk: out std_logic );
12     end component;
13
14     component ccto2 is
15         generic (N : integer);
16         port( mclk, reset: in std_logic;
17              clk: out std_logic );
18     end component;
19
20
21     component mux2x1 is
22         port( seletor: in std_logic;
23              entrada1: in integer range 0 to 15;
24              entrada2: in integer range 0 to 15;
25              saida: out integer range 0 to 15 );
26     end component;
27
28     component dem2x4 is
29         port( aux3 : in std_logic_vector(1 downto 0);
30              aux4 : out std_logic_vector(3 downto 0) );
31     end component;
32
33     component decod_7_seg is
34
35         GENERIC (N : integer := 3);
36         port(
37             chaves: in std_logic_vector(3 downto 0);
38             chaves_display: in std_logic_vector(3 downto 0);
39             anodos: out std_logic_vector(3 downto 0);
40             catodos: out std_logic_vector(0 to 7) );
41
42     end component;
43
44     component somachaves is
45
46         port( soma: inout std_logic_vector(11 downto 0);
47              chaves: in std_logic_vector(7 downto 0);
48              saida3: out integer range 0 to 15;
49              saida2: out integer range 0 to 15;
50              saida1: out integer range 0 to 15 );
51     end component;
52
53     component contador255 is
54
55         port( seletor, reset: in std_logic;
56              saida: out integer range 0 to 255 );
57     end component;
58
59     function to_bcd (bin : std_logic_vector(7 downto 0) ) return std_logic_vector;
60
61 end package;
62
63 package body meu_pacote_led is -- double dabble
64
65     function to_bcd ( bin : std_logic_vector(7 downto 0) ) return std_logic_vector is
66         variable i : integer:=0;
67         variable bcd : std_logic_vector(11 downto 0) := (others => '0');
68         variable bint : std_logic_vector(7 downto 0) := bin;
69

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70     begin
71         for i in 0 to 7 loop
72             bcd(11 downto 1) := bcd(10 downto 0);
73             bcd(0) := bint(7);
74             bint(7 downto 1) := bint(6 downto 0);
75             bint(0) := '0';
76
77             if(i < 7 and bcd(3 downto 0) > "0100") then
78                 bcd(3 downto 0) := bcd(3 downto 0) + "0011";
79             end if;
80
81             if(i < 7 and bcd(7 downto 4) > "0100") then
82                 bcd(7 downto 4) := bcd(7 downto 4) + "0011";
83             end if;
84
85             if(i < 7 and bcd(11 downto 8) > "0100") then
86                 bcd(11 downto 8) := bcd(11 downto 8) + "0011";
87             end if;
88
89         end loop;
90         return bcd;
91     end to_bcd;
92
93 end meu_pacote_led;
```