

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3      --virara umcomponent em meu_pacote_mux4x2.vhd
4
5
6  entity mux2x1 is
7
8      port(    seletor: in std_logic;
9              entrada1: in integer range 0 to 15;
10             entrada2: in integer range 0 to 15;
11             saida: out integer range 0 to 15          );
12 end mux2x1;
13
14 architecture arq of mux2x1 is
15
16     begin
17
18         saida <= entrada2 when seletor='1' else entrada1;
19
20 end arq;
```