```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;

package meu_pacote_led is

    component ccto is

            port(   mclk, reset: in std_logic;
                    clk: out std_logic      );

   end component;

    component ccto2 is

            port(   mclk, reset: in std_logic;
                      clk: out std_logic        );

    end component;

end package;

```