

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use work.meu_pacote_led.all;
4  --CONTADOR DE 4 BITS
5  entity top is
6
7      GENERIC (N : integer := 4);
8      port(mclk, reset: in std_logic;
9           clk1, clk2, clk3, clk4: out std_logic    );
10 end top;
11
12 architecture Behavioral of top is
13
14     begin
15         map1 : entity work.ccto(arq)
16             generic map (N => N)
17             port map( mclk, reset,  clk1 ); --in,in,out
18
19         map2 : entity work.ccto2(arq)
20             generic map (N => N)
21             port map( mclk, reset,  clk2 ); --in,in,out
22
23         map3 : entity work.ccto3(arq)
24             generic map (N => N)
25             port map( mclk, reset,  clk3 ); --in,in,out
26
27         map4 : entity work.ccto4(arq)
28             generic map (N => N)
29             port map( mclk, reset,  clk4 ); --in,in,out
30
31     end Behavioral;
32
33
```