```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;

package meu_pacote_led is

    component ccto is
            generic (N : integer);
            port(   mclk, reset: in std_logic;
                    clk: out std_logic      );
   end component;

    component ccto2 is
            generic (N : integer);
            port(   mclk, reset: in std_logic;
                    clk: out std_logic      );
   end component;

    component ccto3 is
            generic (N : integer);
        port(   mclk, reset: in std_logic;
                    clk: out std_logic      );
    end component;

    component ccto4 is
            generic (N : integer);
            port(   mclk, reset: in std_logic;
                    clk: out std_logic      );
    end component;


        component decod_7_seg is

             GENERIC (N : integer := 3);
             port(
             chaves: in std_logic_vector(N-1 downto 0);
             anodos: out std_logic_vector(N-1 downto 0);
             catodos: out std_logic_vector(0 to 7)          );

        end component;

end package;

```