

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.all;
3
4 package meu_pacote_led is
5
6     component ccto is
7
8         port(    mclk, reset: in std_logic;
9                 clk: out std_logic
10                );
11
12     end component;
13
14     component ccto2 is
15
16         port(    mclk, reset: in std_logic;
17                 clk: out std_logic
18                );
19
20     end component;
21
22 end package;
```