```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity ccto0 is
    port(   mclk, reset: in std_logic;
                    clk: out std_logic        );
end entity;

architecture arq of ccto0 is
    -- troca-se o M e o tempo de simulacao somente para ver a forma de onda,
    50_000_000 = 1Hz na basys
    constant M: integer := 50_000_000 ; --50_000_000; /2 1HZ na Basys, 100_000_000; /2
    0.5HZ

    begin

        process(mclk, reset)
            variable i: integer range 1 to M := 1;
            variable v_clk: std_logic := '0';
            begin
            if (reset = '1') then i := 1; v_clk := '0';
                elsif(mclk'event and mclk='1') then i := i + 1;
                if (i = M/4) then i := 1; v_clk := not(v_clk);      --/2 = 1Hz
            end if;
            clk <= v_clk; end if;
        end process;
end arq;
```